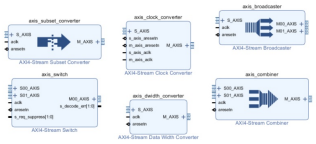

Xilinx AXI4-Stream Integrated Logic Analyzer Guide

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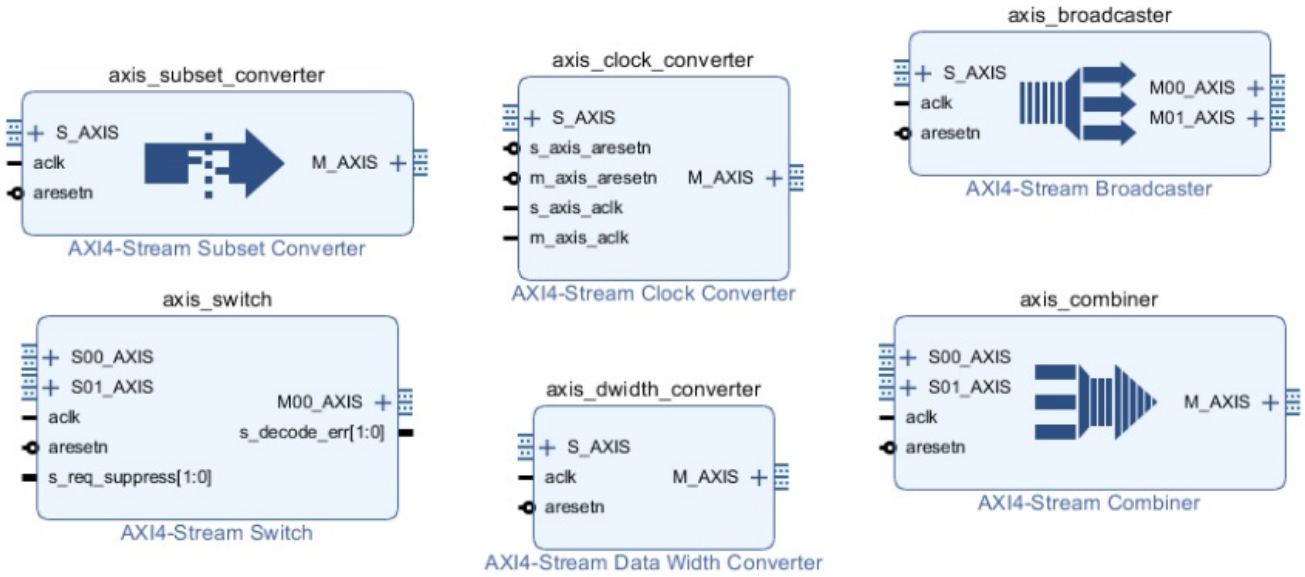
Xilinx AXI4-Stream Integrated Logic Analyzer Guide



Introduction

The Integrated Logic Analyzer (ILA) with AXI4-Stream Interface core is a customizable logic analyzer IP that can be used to monitor the internal signals and interfaces of a design. The ILA core includes many advanced features of modern logic analyzers, including boolean trigger equations and edge transition triggers. The core also offers interface debugging and monitoring capability along with protocol checking for memory-mapped AXI and AXI4-Stream. Because the ILA core is synchronous to the design being monitored, all design clock constraints that are applied to your design are also applied to the components of the ILA core. To debug interfaces within a design, ILA IP needs to be added to a block design in the Vivado® IP integrator. Similarly, AXI4/AXI4-Stream protocol checking option can be enabled for ILA IP in the IP integrator. Protocol violations can be then displayed in the waveform viewer of the Vivado logic analyzer.

Features

- User-selectable number of probe ports and probe width.
- User-selectable storage targets such as block RAM and UltraRAM
- Multiple probe ports can be combined into a single trigger condition.
- User-selectable AXI slots to debug AXI interfaces in a design.
- Configurable options for AXI interfaces including interface types and trace sample depth.
- Data and trigger property for probes.
- A number of comparators and the width for each probe and individual ports within interfaces.
- Input/output cross-triggering interfaces.
- Configurable pipelining for input probes.
- AXI4-MM and AXI4-Stream protocol checking.

For more information about the ILA core, see the Vivado Design Suite User Guide: Programming and Debugging (UG908).

IP Facts

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family[1]	Versal™ ACAP
Supported User Interfaces	IEEE Standard 1149.1 – JTAG
Provided with Core	
Design Files	RTL
Example Design	Verilog
Test Bench	Not Provided
Constraints File	Xilinx® Design Constraints (XDC)
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the **Xilinx Design Tools: Release Notes Guide**.
Synthesis	Vivado Synthesis
Support	
All Vivado IP Change Logs	Master Vivado IP Change Logs: **72775**
Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado® IP catalog.
2. For the supported versions of the tools, see the **Xilinx Design Tools: Release Notes Guide**.

Overview

Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. This document covers the following design processes:

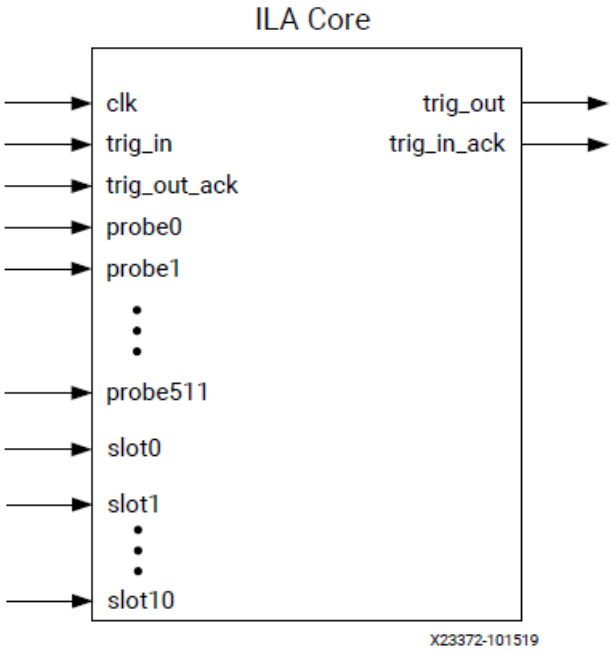
- Hardware, IP, and Platform Development: Creating the PL IP blocks for the hardware platform, creating PL kernels, subsystem functional simulation, and evaluating the Vivado® timing, resource use, and power closure. Also involves developing the hardware platform for system integration. Topics in this document that apply to this design process include:
- Port Descriptions
- Clocking and Resets
- Customizing and Generating the Core

Core Overview
Signals and interfaces in the FPGA design are connected to an ILA probe and slot inputs. These signals and interfaces, attached to the probe and slot inputs respectively, are sampled at design speeds and stored using on-chip block RAM. Signals and interfaces in the Versal™ ACAP design are connected to the ILA probe and slot inputs. These attached signals and interfaces are sampled at design speeds using the core clock input and stored in on-chip block RAM memories. The core parameters specify the following:

- A number of probes (up to 512) and probe width (1 to 1024).
- A number of slots and interface options.
- Trace sample depth.
- Data and/or trigger property for probes.
- Number of comparators for each probe.

Communication with the ILA core is conducted using an instance of the AXI Debug Hub that connects to the Control, Interface, and Processing System (CIPS) IP core.

Figure 1: **ILA Core**



After the design is loaded into the Versal ACAP, use the Vivado® logic analyzer software to set up a trigger event for the ILA measurement. After the trigger occurs, the sample buffer is filled and uploaded into the Vivado logic analyzer. You can view this data using the waveform window. The probe sample and trigger functionality is implemented in the programmable logic region. On-chip block RAM or UltraRAM memory based on the storage target you have selected during customization which stores the data until it is uploaded by the software. No user input or output is required to trigger events, capture data, or to communicate with the ILA core. ILA core is capable of monitoring interface-level signals, it can convey transaction-level information such as the outstanding transactions for AXI4 interfaces.

ILA Probe Trigger Comparator
Each probe input is connected to a trigger comparator that is capable of performing various operations. At run time the comparator can be set to perform = or != comparisons. This includes matching level patterns, such as X0XX101. It also includes detecting edge transitions such as rising edge (R), falling edge (F), either edge (B), or no transition (N). The trigger comparator can perform more complex comparisons, including >, <, ≥, and ≤.

IMPORTANT! The comparator is set at run time through the Vivado® logic analyzer.

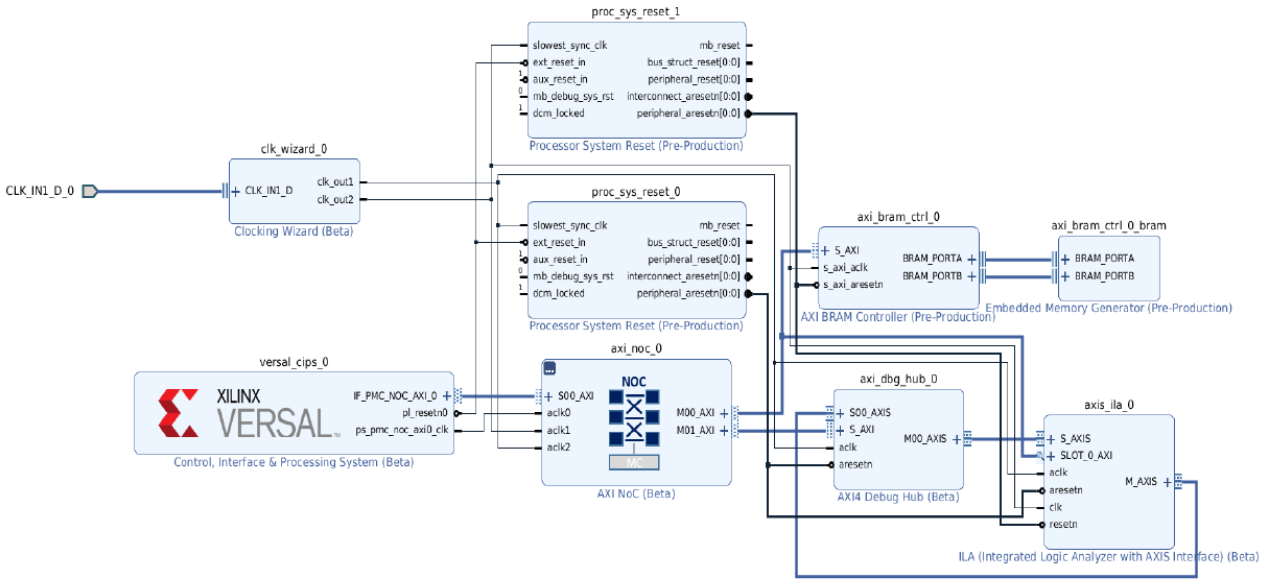
ILA Trigger Condition

The trigger condition is the result of a Boolean “AND” or “OR” calculation of each of the ILA probe trigger comparator results. Using the Vivado® logic analyzer, you select whether to “AND” probe trigger comparators probes or “OR” them. The “AND” setting causes a trigger event when all of the ILA probe comparisons are satisfied. The “OR” setting causes a trigger event when any of the ILA probe comparisons are satisfied. The trigger condition is the trigger event used for the ILA trace measurement.

Applications

The ILA core is designed to be used in an application that requires verification or debugging using Vivado®. The following figure shows CIPS IP core writes and reads from the AXI block RAM controller through the AXI Network on Chip (NoC). The ILA core is connected to the interface net between the AXI NoC and AXI block RAM controller to monitor the AXI4 transaction in the hardware manager.

Figure 2: **AXI Interface Debugging Use Case**



Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado® Design Suite under the terms of the Xilinx End User License.

Note: To verify that you need a license, check the License column of the IP Catalog. Included means that a license is included with the Vivado® Design Suite; Purchase means that you have to purchase a license to use the core. Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Port Descriptions

The following tables provide details about the ILA ports and parameters.

ILA Ports

Table 1: **ILA Ports**

Port Name	I/O	Description
clk	I	Design clock that clocks all trigger and storage logic.
probe<n>[<m> – 1:0]	I	Probe port input. The probe port number <n> is in the range from 0 to 511. The probe port width (denoted by <m>) is in the range of 1 to 1024. You must declare this port as a vector. For a 1-bit port, use probe<n>[0:0].
trig_out	O	The trig_out port can be generated either from the trigger condition or from an external trig_in port. There is a run time control from the Logic Analyzer to switch between trigger condition and trig_in to dri ve trig_out.
trig_in	I	Input trigger port used in process based system for Embedded Cro ss Trigger. Can be connected to another ILA to create cascading Tr igger.
slot_<p>_<intf_name>	I	Slot interface. The type of the interface <intf_name> is created dynamically based on the slot_<p>_<intf_name> interface type parameter. The individual ports within the interfaces are available for monitoring in t he hardware manager.
trig_out_ack	I	An acknowledgment to trig_out.
trig_in_ack	O	An acknowledgment to trig_in.
resetn	I	ILA Input Type when set to ‘Interface Monitor’, this port should be th e same reset signal that is synchronous to the design logic that is a ttached to the Slot_<p>_<intf_name> ports of the ILA core.
S_AXIS	I/O	Optional port. Used for manual connection with AXI Debug Hub core when ‘Enabl e AXI4- Stream Interface for Manul Connection to AXI Debug Hub’ i s selected in Advanced Options.
M_AXIS	I/O	Optional port. Used for manual connection with AXI Debug Hub core when ‘Enabl e AXI4- Stream Interface for Manual Connection to AXI Debug Hub’ is selected in ‘Advanced Options’.

Table 1: **ILA Ports** *(cont'd)*		
Port Name	**I/O**	**Description**
aresetn	I	Optional port. Used for manual connection with AXI Debug Hub core when 'Enable AXI4- Stream Interface for Manual Connection to AXI Debug Hub' is selected in 'Advanced Options'. This port should be synchronous with reset port of AXI Debug Hub.
aclk	I	Optional port. Used for manual connection with AXI Debug Hub core when 'Enable AXI4- Stream Interface for Manual Connection to AXI Debug Hub' is selected in 'Advanced Options'. This port should be synchronous with clock port of AXI Debug Hub.

ILA Parameters

Table 2: **ILA Parameters**

Parameter	Allowable Values	Default Values	Description
Component_Name	String with A–Z, 0–9, and _ (underscore)	ila_0	Name of instantiated component.
C_NUM_OF_PROBES	1–512	1	Number of ILA probe ports.
C_MEMORY_TYPE	0, 1	0	Storage target for the data captured. 0 corresponds to block RAM and 1 corresponds to Ultra RAM.
C_DATA_DEPTH	1,024, 2,048, 4,096, 8,192, 16,384, 32,768, 65,536, 131,072	1,024	Probe storage buffer depth. This number represents the maximum number of samples that can be stored at run time for each probe input.
C_PROBE<n>_WIDTH	1–1024	1	Width of probe port <n>. Where <n> is the probe port having a value from 0 to 1,023.
C_TRIGOUT_EN	True/False	FALSE	Enables the trig out functionality. Ports trig_out and trig_out_ack are used.
C_TRIGIN_EN	True/False	FALSE	Enables the trig in functionality. Ports trig_in and trig_in_ack are used.
C_INPUT_PIPE_STAGES	0–6	0	Add extra flops to the probe ports. One parameter applies to all of the probe ports.
ALL_PROBE_SAME_MU	True/False	TRUE	This forces the same compare value units (match units) to all of the probes.
C_PROBE<n>_MU_CNT	1–16	1	Number of Compare Value (Match) units per probe. This is valid only if ALL_PROBE_SAME_MU is FALSE.
C_PROBE<n>_TYPE	DATA and TRIGGER, TRIGGER, DATA	DATA and TRIGGER	To choose a selected probe for specifying trigger condition or for data storage purpose or for both.
C_ADV_TRIGGER	True/False	FALSE	Enables the advance trigger option. This enables trigger state machine and you can write your own trigger sequence in Vivado Logic Analyzer.

Table 2: **ILA Parameters** *(cont'd)*			
Parameter	**Allowable Values**	**Default Values**	**Description**
C_NUM_MONITOR_SLOTS	1-11	1	Number of Interface Slots.

Notes:

1. The maximum number of compare value (match) units is limited to 1,024. For the basic trigger (C_ADV_TRIGGER = FALSE), each probe has one compare value unit (as in the earlier version). But for the advance trigger option (C_ADV_TRIGGER = TRUE), this means the individual probes can still have possible selection of number of compare values units from one to four. But all compare value units should not exceed more than 1,024. This means, if you need four compare units per probe then you are allowed to use only 256 probes.

Designing with the Core

This section includes guidelines and additional information to facilitate designing with the core.

Clocking

The clk input port is the clock used by the ILA core to register the probe values. For best results, it should be the same clock signal that is synchronous to the design logic that is attached to the probe ports of the ILA core. When connecting manually with AXI Debug Hub, the aclk signal should be synchronous to AXI Debug Hub clock input port.

Resets

When you set an ILA Input Type to Interface Monitor, reset port should be the same reset signal that is synchronous to the design logic whose interface is attached to slot_<p>_<intf_name> port of the ILA core. For manual connection with an AXI Debug Hub core, present port should be synchronous with the reset port of an AXI Debug Hub core.

Design Flow Steps

This section describes customizing and generating the core, constraining the core, and the simulation, synthesis, and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994)
- Vivado Design Suite User Guide: Designing with IP (UG896)
- Vivado Design Suite User Guide: Getting Started (UG910)
- Vivado Design Suite User Guide: Logic Simulation (UG900)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado® Design Suite. If you are customizing and generating the core in the Vivado IP integrator, see the Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994) for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the validate_bd_design command in the Tcl console. You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.

2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click the menu.

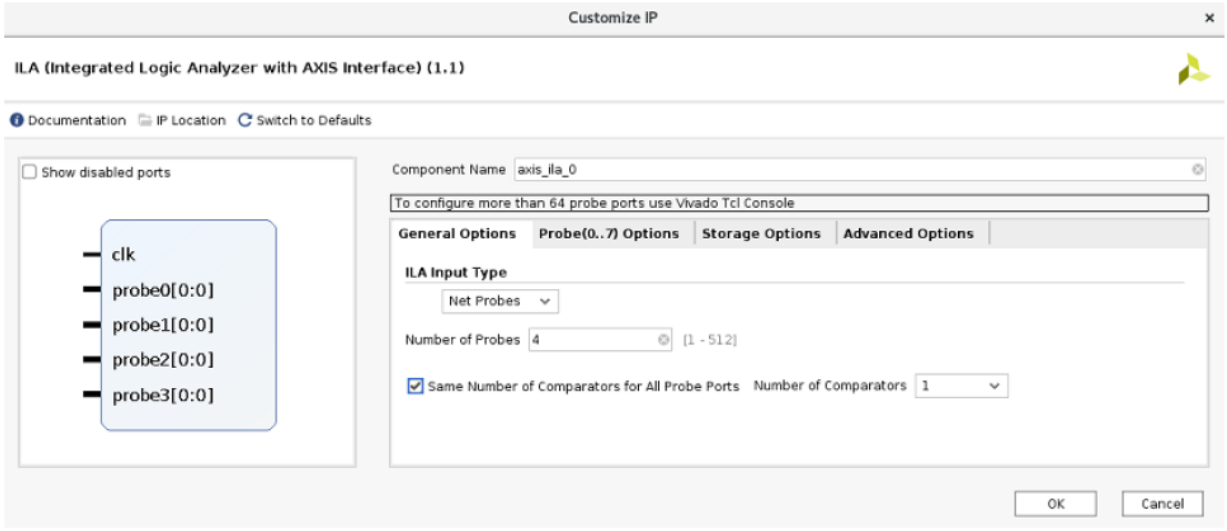
For details, see the Vivado Design Suite User Guide: Designing with IP (UG896) and the Vivado Design Suite User Guide: Getting Started (UG910). Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

To access the core, perform the following:

1. Open a project by selecting File then Open Project or create a new project by selecting File then New Project in Vivado.
2. Open the IP catalog and navigate to any of the taxonomies.
3. Double-click ILA to bring up the core name Vivado IDE.

General Options Panel
The following figure shows the General Options tab in the Native setting that allows you to specify the options:

Figure 3: **General Options Panel – Native Probes Type**



The following figure shows the General Options tab in the AXI setting that allows you to specify the options:

Figure 4: **General Options Panel – Interface Monitor Type**

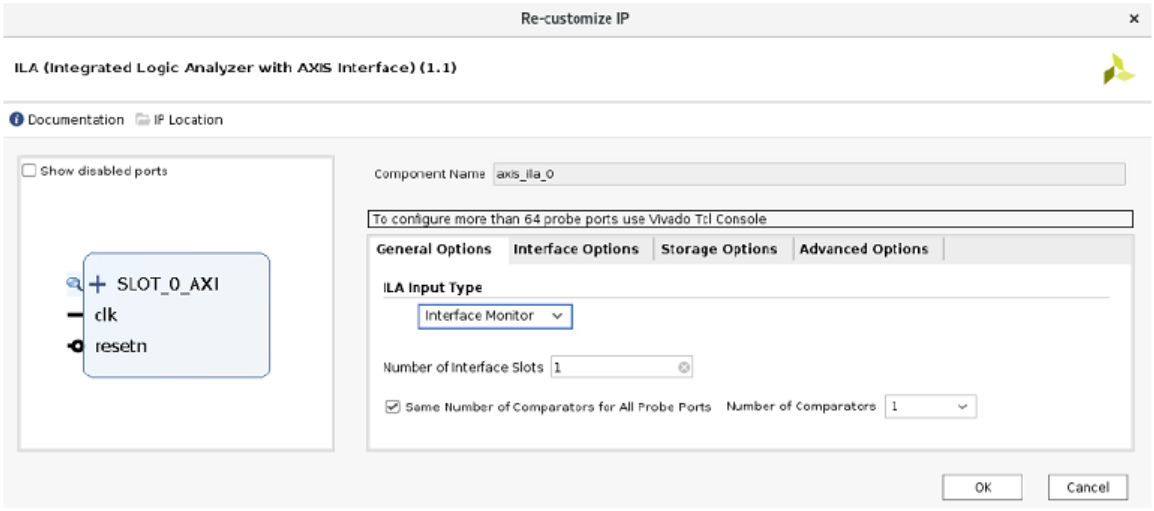
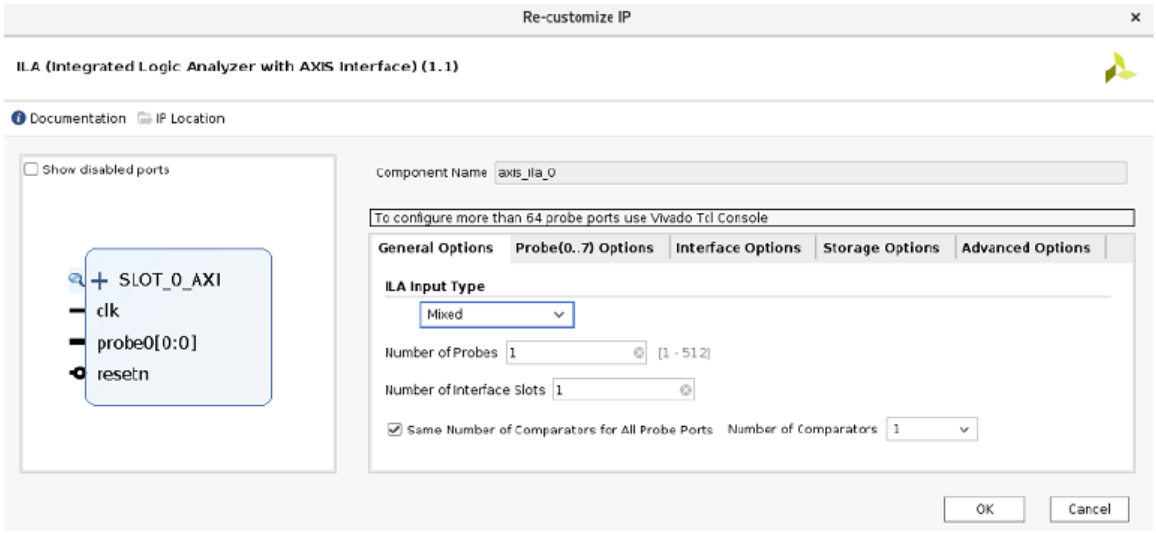


Figure 5: **General Options Panel – Mixed Type**

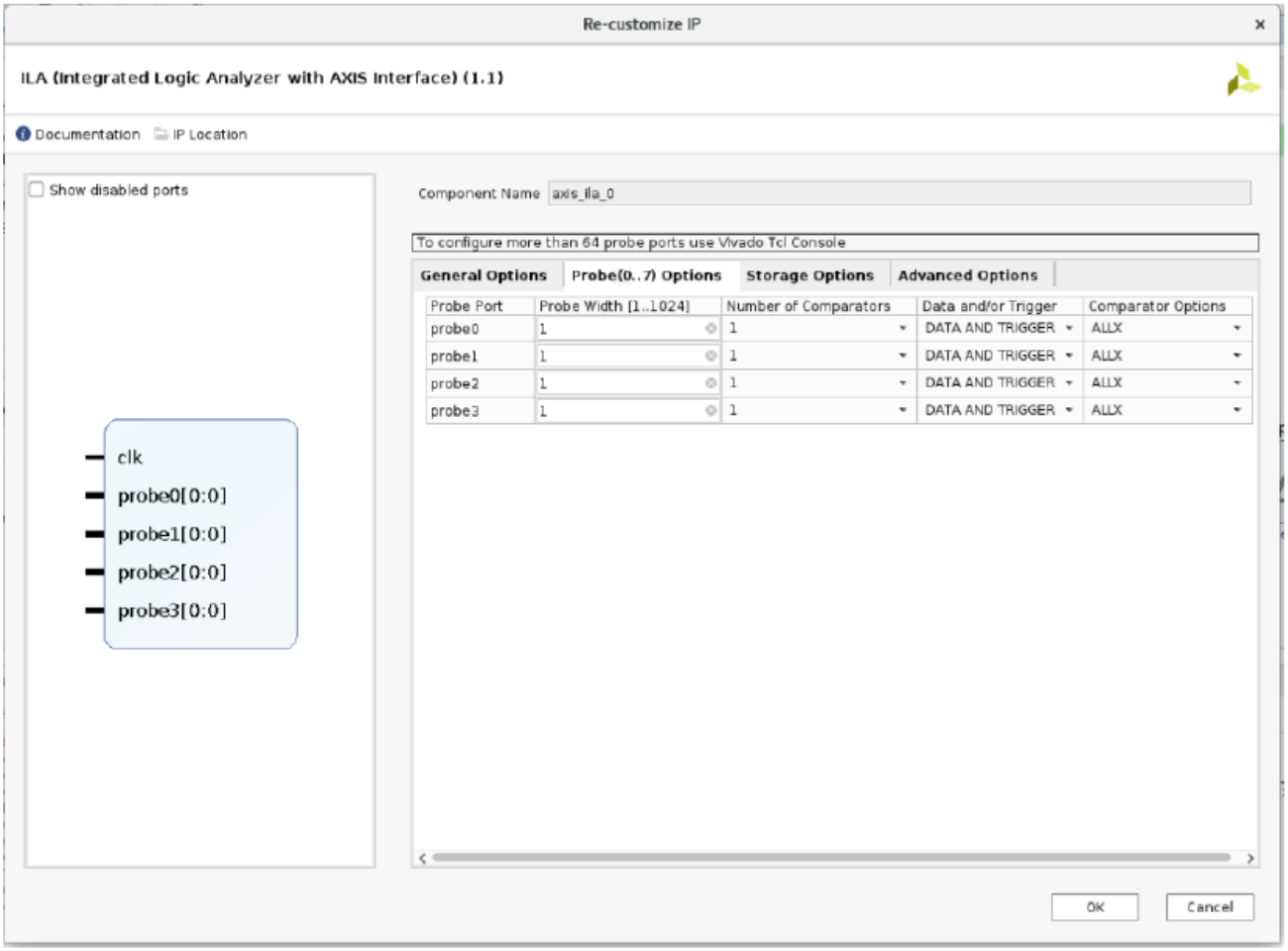


- Component Name: Use this text field to provide a unique module name for the ILA core.
- ILA Input Type: This option specifies which type of interface or signal ILA should be debugging. Currently, the values for this parameter are “Native Probes”, “Interface Monitor” and “Mixed.”
- Number of Probes: Use this text field to select the number of probe ports on the ILA core. The valid range used in the Vivado® IDE is 1 to 64. If you need more than 64 probe ports, you need to use the Tcl command flow to generate the ILA core.
- A number of Interface Slots (only available in Interface Monitor type and Mixed type): This option allows you to select the number of AXI interface slots that need to be connected to the ILA.
- Same Number of Comparators for All Probe Ports: The number of comparators per probe can be configured on this panel. The same number of comparators for all probes can be enabled by selecting.

Probe Port Panels

The following figure shows the Probe Ports tab that allows you to specify settings:

Figure 6: **Probe Ports Panel**

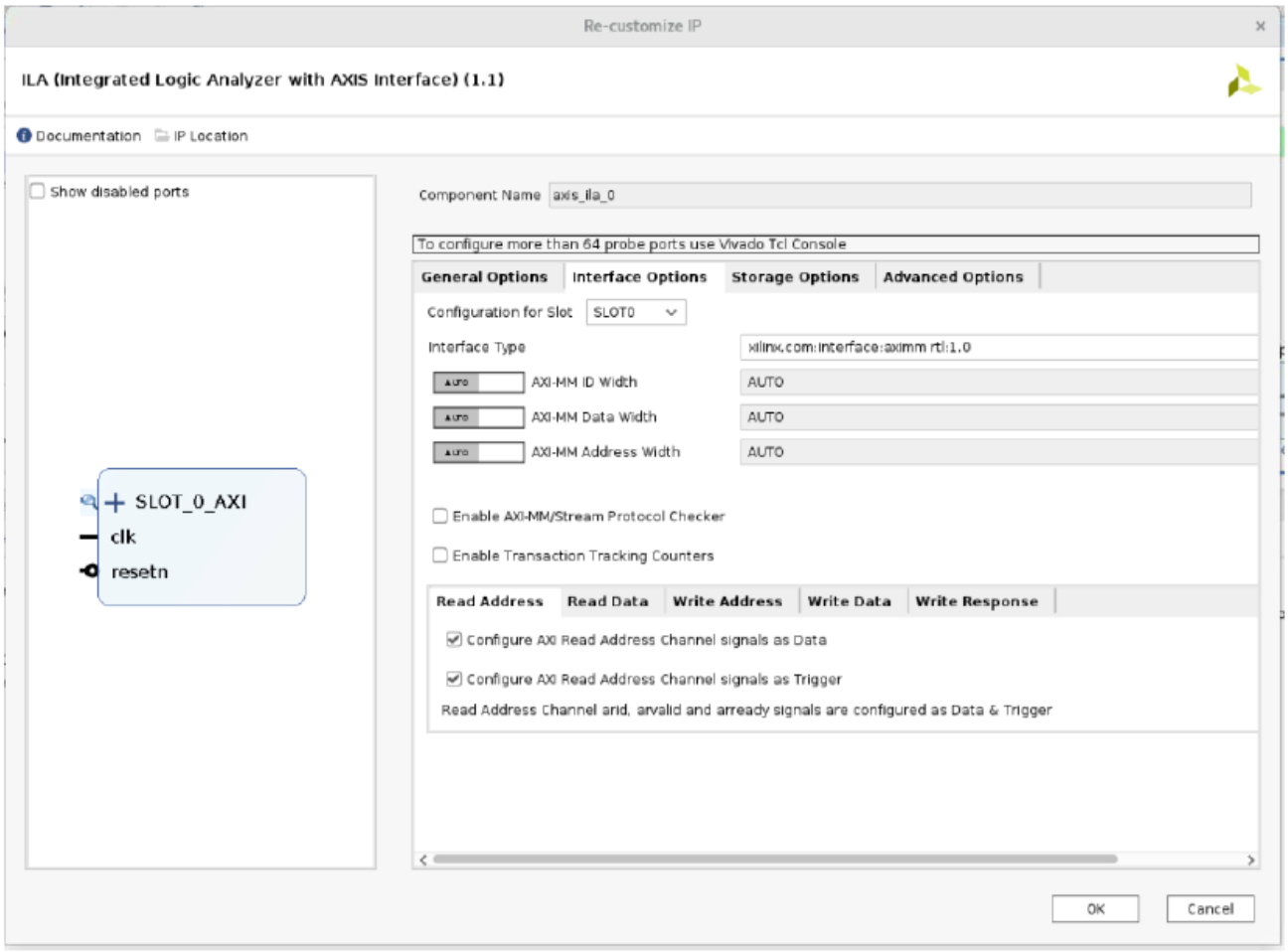


- Probe Port Panel: Width of each Probe Port can be configured in Probe Port Panels. Each Probe Port Panel has up to seven ports.
- Probe Width: Width of each Probe Port can be mentioned. The valid range is 1 to 1024.
- Number of Comparators: This option is enabled only when “Same Number of Comparators for All Probe Ports” option is disabled. A comparator for each probe in the range 1 to 16 can be set.
- Data and/or Trigger: Probe type for each probe can be set using this option. The valid options are DATA_and_TRIGGER, DATA and TRIGGER.
- Comparator Options: The type of operation or comparison for each probe can be set using this option.

Interface Options

The following figure shows the Interface Options tab when Interface Monitor or Mixed type is selected for ILA input type:

Figure 7: **Interface Options Tab**



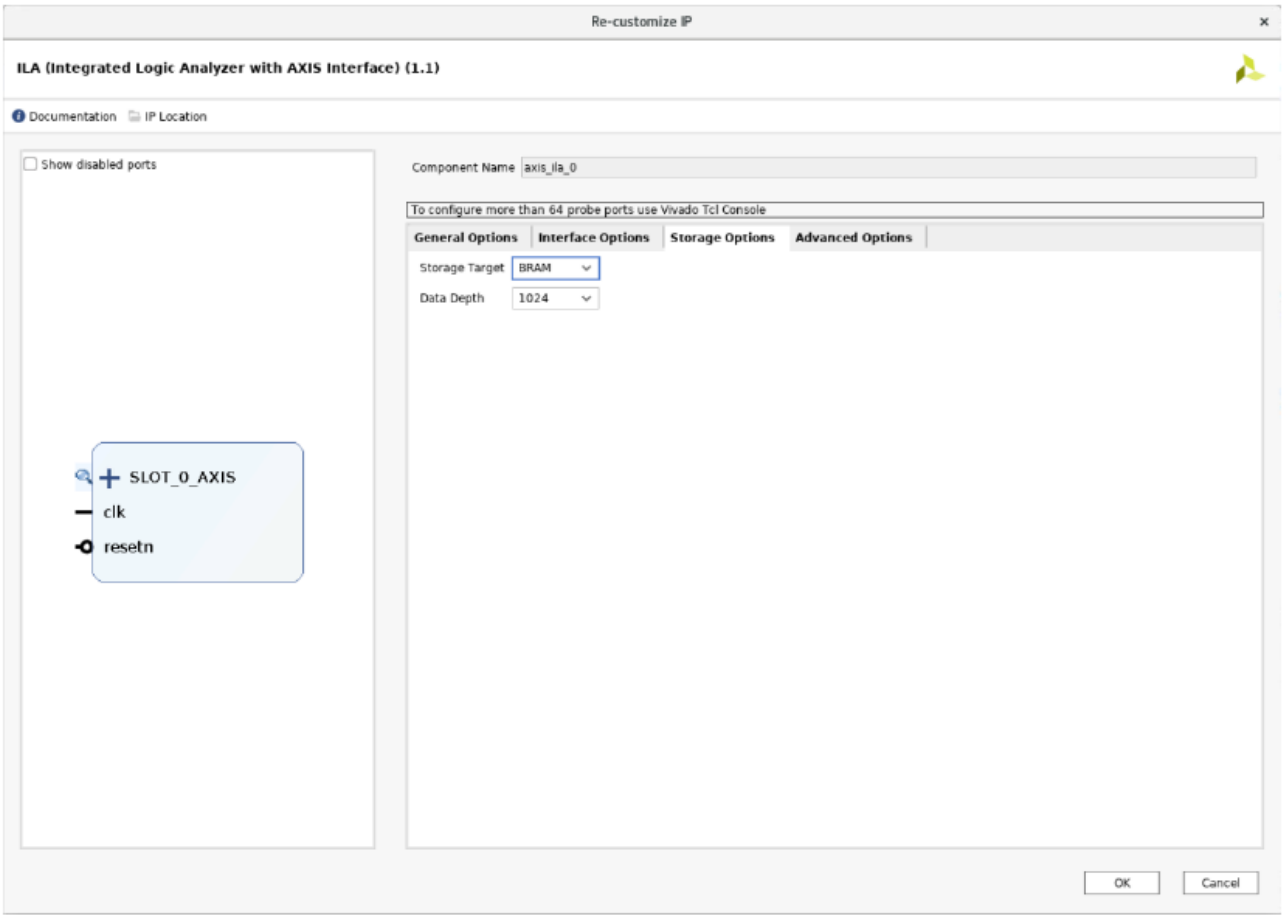
- Interface Type: Vendor, Library, Name, and Version (VLNV) of the interface to be monitored by the ILA core.
- AXI-MM ID Width: Selects the ID width of the AXI interface when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- AXI-MM Data Width: Selects the parameters corresponding to slot_Selects the Data width of the AXI interface when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- AXI-MM Address Width: Selects the Address width of the AXI interface when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Enable AXI-MM/Stream Protocol Checker: Enables AXI4-MM or AXI4-Stream protocol checker for slot <p> when the slot_<p> interface type is configured as AXI-MM or AXI4-Stream, where <p> is the slot number.
- Enable Transaction Tracking Counters: Enables AXI4-MM transaction tracking capability.
- Number of Outstanding Read Transactions: Specifies the number of outstanding Read transactions per ID. The value should be equal to or greater than the number of outstanding Read transactions for that connection.
- Number of Outstanding Write Transactions: Specifies the number of outstanding Write transactions per ID. The value should be equal to or greater than the number of outstanding Write transactions for that connection.
- Monitor APC Status signals: Enable monitoring of APC status signals for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Configure AXI read address channel as Data: Select read address channel signals for data storage purpose for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Configure AXI read address channel as Trigger: Select read address channel signals for specifying trigger condition for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.

- Configure AXI read data channel as Data: Select read data channel signals for data storage purposes for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Configure AXI read data channel as Trigger: Select read data channel signals for specifying trigger conditions for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Configure AXI write address channel as Data: Select write address channel signals for data storage purpose for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Configure AXI write address channel as Trigger: Select write address channel signals for specifying trigger conditions for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Configure AXI write data channel as Data: Select write data channel signals for data storage purpose for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Configure AXI write data channel as Trigger: Select write data channel signals for specifying trigger condition for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Configure AXI write response channel as Data: Select write response channel signals for data storage purposes for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- Configure AXI write response channel as Trigger: Select write response channel signals for specifying trigger condition for slot <p> when the slot_<p> interface type is configured as AXI-MM, where <p> is the slot number.
- AXI-Stream Tdata Width: Selects the Tdata width of the AXI-Stream interface when the slot_<p> interface type is configured as AXI-Stream, where <p> is the slot number.
- AXI-Stream TID Width: Selects the TID width of the AXI-Stream interface when the slot_<p> interface type is configured as AXI-Stream, where <p> is the slot number.
- AXI-Stream TUSER Width: Selects the TUSER width of the AXI-Stream interface when the slot_<p> interface type is configured as AXI-Stream, where <p> is the slot number.
- AXI-Stream TDEST Width: Selects the TDEST width of the AXI-Stream interface when the slot_<p> interface type is configured as AXI-Stream, where <p> is the slot number.
- Configure AXIS Signals as Data: Select AXI4-Stream signals for data storage purpose for slot <p> when the slot_<p> interface type is configured as AXI-Stream where <p> is the slot number.
- Configure AXIS Signals as Trigger: Select AXI4-Stream signals for specifying trigger condition for slot <p> when the slot_<p> interface type is configured as AXI-Stream, where <p> is the slot number.
- Configure Slot as Data and/or Trigger: Selects non-AXI slot signals for specifying trigger condition or for data storage purpose or for both for slot <p> when the slot_<p> interface type is configured as non-AXI, where <p> is the slot number.

Storage Options

The following figure shows the Storage Options tab that allows you to select the storage target type and depth of the memory to be used:

Figure 8: **Storage Options Tab**

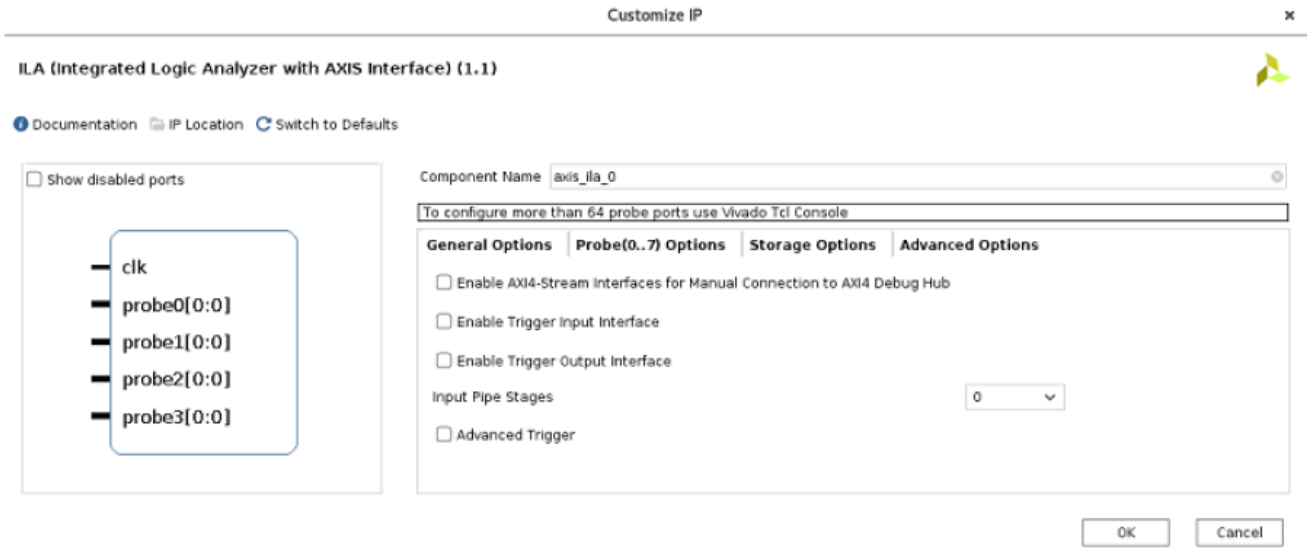


- Storage Target: This parameter is used to select the storage target type from the drop-down menu.
- Data Depth: This parameter is used to select a suitable sample depth from the drop-down menu.

Advanced Options

The following figure shows the Advanced Options tab:

Figure 9: **Advanced Options Tab**



- Enable AXI4-Stream Interface for Manual Connection to AXI Debug Hub: When enabled, this option gives an

AXIS interface for the IP to connect to AXI Debug Hub.

- Enable Trigger Input Interface: Check this option to enable an optional trigger input port.
- Enable Trigger Output Interface: Check this option to enable an optional trigger output port.
- Input Pipe Stages: Select the number of registers you want to add for the probe to improve implementation results. This parameter applies to all probes.
- Advanced Trigger: Check to enable the state machine-based trigger sequencing.

Output Generation

For details, see the Vivado Design Suite User Guide: Designing with IP (UG896).

Constraining the Core

Required Constraints

The ILA core includes an XDC file that contains appropriate false path constraints to prevent the over-constraining of clock domain crossing synchronization paths. It is also expected that the clock signal connected to the clk input port of the ILA core is properly constrained in your design.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

- **Clock Frequencies**

  This section is not applicable for this IP core.
- **Clock Management**

  This section is not applicable for this IP core.
- **Clock Placement**

  This section is not applicable for this IP core.
- **Banking**

  This section is not applicable for this IP core.
- **Transceiver Placement**

  This section is not applicable for this IP core.
- **I/O Standard and Placement**

  This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third-party tools, see the Vivado Design Suite User Guide: Logic Simulation (UG900).

Synthesis and Implementation

For details about synthesis and implementation, see the Vivado Design Suite User Guide: Designing with IP (UG896).

Debugging

This appendix includes details about resources available on the Xilinx® Support website and debugging tools. If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT! IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.

Finding Help on Xilinx.com

To help in the design and debug process when using the core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support. The Xilinx Community Forums are also available where members can learn, participate, share, and ask questions about Xilinx solutions.

Documentation
This product guide is the main document associated with the core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records
Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available. Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Technical Support
Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Additional Resources and Legal Notices

Xilinx Resources
For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- • From the Vivado® IDE, select Help → Documentation and Tutorials.
  • On Windows, select Start → All Programs → Xilinx Design Tools → DocNav.
  • At the Linux command prompt, enter docnav.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the Design Hubs View tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References
These documents provide supplemental material useful with this guide:

1. Vivado Design Suite User Guide: Programming and Debugging (UG908)
2. Vivado Design Suite User Guide: Designing with IP (UG896)
3. Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994)
4. Vivado Design Suite User Guide: Getting Started (UG910)
5. Vivado Design Suite User Guide: Logic Simulation (UG900)
6. Vivado Design Suite User Guide: Implementation (UG904)
7. ISE to Vivado Design Suite Migration Guide (UG911)
8. AXI Protocol Checker LogiCORE IP Product Guide (PG101)
9. AXI4-Stream Protocol Checker LogiCORE IP Product Guide (PG145)

Revision History
The following table shows the revision history for this document.

Section	Revision Summary
11/23/2020 Version 1.1	
Initial release.	N/A

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PG357 (v1.1) November 23, 2020, ILA with AXI4-Stream Interface v1.1