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Walfront ESP32 WiFi and Bluetooth Internet of Things Module

Walfront ESP32 WiFi and Bluetooth Internet of Things Module User Manual

Contents

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Walfront ESP32 WiFi and Bluetooth Internet of Things Module

Product Information

- **Module:** ESP32
- **Features:** WiFi-BT-BLE MCU module

Pin Definitions

Pin Description

Name	No.	Type	Function

Strapping Pins

Pin	Default	Function

Functional Description

- **CPU and Internal Memory**

  The ESP32 module has a dual-core processor and internal memory for system operations.

- **External Flash and SRAM**

  The ESP32 supports external QSPI flash and SRAM, providing additional storage and encryption capabilities.

- **Crystal Oscillators**

  The module utilizes a 40-MHz crystal oscillator for timing and synchronization.

- **RTC and Low-Power Management**

  Advanced power-management technologies enable the ESP32 to optimize power consumption based on usage.

FAQ

- **Q: What are the default strapping pins for ESP32?**

  A: The default strapping pins for ESP32 are MTDI, GPIO0, GPIO2, MTDO, and GPIO5.

- **Q: What is the power supply voltage range for ESP32?**

  A: The power supply voltage range for ESP32 is 3.0V to 3.6V.

About This Document
This document provides the specifications for the ESP32 module.

Overview

ESP32 is a powerful, generic WiFi-BT-BLE MCU module that targets a wide variety of applications, ranging from low-power sensor networks to the most demanding tasks, such as voice encoding, music streaming and MP3 decoding.
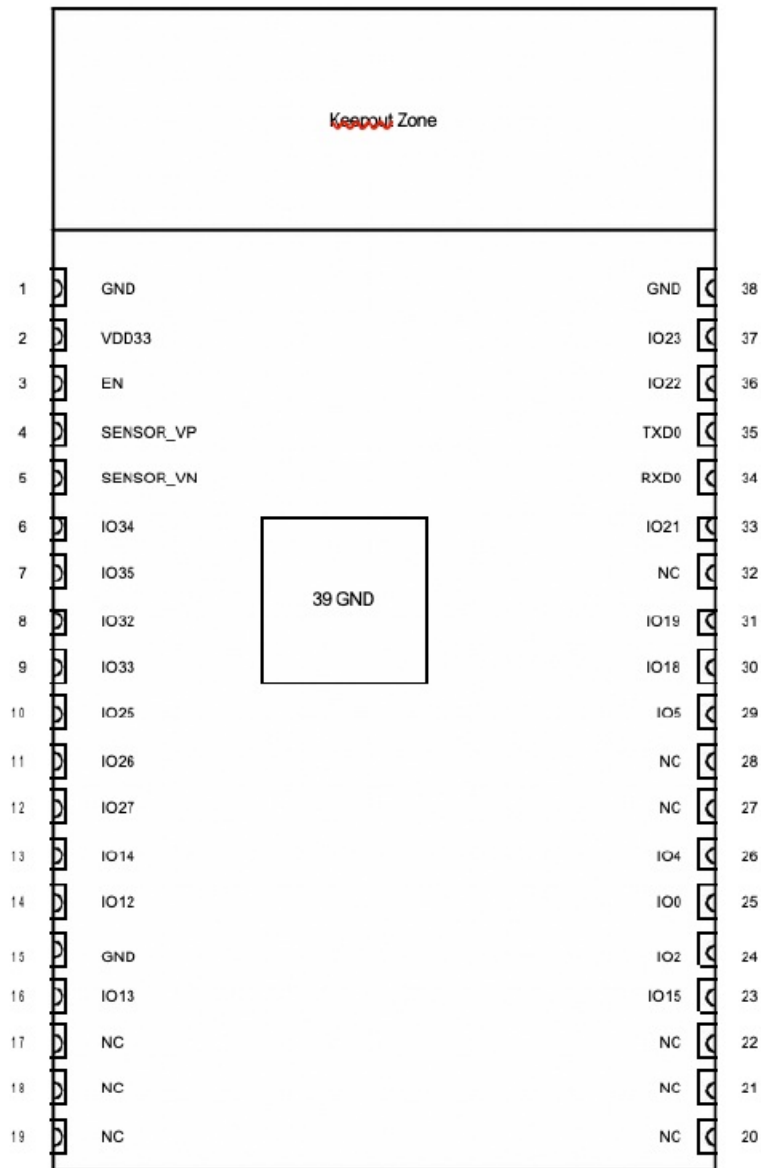
Pin Definitions

Pin Layout

Figure 1: Pin Layout of ESP32 (Top View)

Pin Description

ESP32 has 38 pins. See pin definitions in Table 1.

Table 1: Pin Definitions

Name	No.	Type	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	I	Module-enable signal. Active high.
SENSOR_VP	4	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_VN	5	I	GPIO39, ADC1_CH3, RTC_GPIO3
IO34	6	I	GPIO34, ADC1_CH6, RTC_GPIO4
IO35	7	I	GPIO35, ADC1_CH7, RTC_GPIO5

IO32	8	I/O	GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
IO33	9	I/O	GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
IO25	10	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	11	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	12	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
IO14	13	I/O	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
IO12	14	I/O	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
GND	15	P	Ground
IO13	16	I/O	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
NC	17	–	–
NC	18	–	–
NC	19	–	–
NC	20	–	–
NC	21	–	–
NC	22	–	–
IO15	23	I/O	GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	24	I/O	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	25	I/O	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	26	I/O	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
NC1	27	–	–

NC2	28	–	–
IO5	29	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
IO18	30	I/O	GPIO18, VSPICLK, HS1_DATA7

IO19	31	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
NC	32	–	–
IO21	33	I/O	GPIO21, VSPIHD, EMAC_TX_EN
RXD0	34	I/O	GPIO3, U0RXD, CLK_OUT2
TXD0	35	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO22	36	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
IO23	37	I/O	GPIO23, VSPID, HS1_STROBE
GND	38	P	Ground

Notice:
GPIO6 to GPIO11 are connected to the SPI flash integrated on the module and are not connected out.

Strapping Pins
ESP32 has five strapping pins:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

The software can read the values of these five bits from the register "GPIO_STRAPPING". During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings. Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins. To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32. After reset release, the strapping pins work as normal-function pins. Refer to Table 2 for a detailed boot-mode configuration by strapping pins.

Table 2: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)			
Pin	Default	3.3 V	1.8 V
MTDI	Pull-down	0	1

Booting Mode				
Pin	Default	SPI Boot		Download Boot
GPIO 0	Pull-up	1		0
GPIO 2	Pull-down	Don't-care		0
Enabling/Disabling Debugging Log Print over U0TXD During Booting				
Pin	Default	U0TXD Active		U0TXD Silent
MTDO	Pull-up	1		0
Timing of SDIO Slave				
Pin	Default	Falling-edge Sampling Falling-edge Output	Falling-edge Sampling Rising-edge Output	Rising-edge Sampling Falling-edge Output	Rising-edge Sampling Rising-edge Output
MTDO	Pull-up	0	0	1	1
GPIO 5	Pull-up	0	1	0	1

Note:

- Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave" after booting.
- The internal pull-up resistor (R9) for MTDI is not populated in the module, as the flash and SRAM in ESP32 only support a power voltage of 3.3 V (output by VDD_SDIO)

Functional Description

This chapter describes the modules and functions integrated into ESP32.

CPU and Internal Memory
ESP32 contains two low-power Xtensa® 32-bit LX6 microprocessors. The internal memory includes:

- 448 KB of ROM for booting and core functions.
- 520 KB of on-chip SRAM for data and instructions.
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash-encryption and chip-ID.

External Flash and SRAM
ESP32 supports multiple external QSPI flash and SRAM chips. ESP32 also supports hardware encryption/decryption based on AES to pro-tect developers' programs and data in Flash.

ESP32 can access the external QSPI flash and SRAM through high-speed caches.

- The external flash can be mapped into CPU instruction memory space and read-only memory space simultaneously.
  - When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU.
  - When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads are supported.
- External SRAM can be mapped into CPU data memory space. Up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads and writes are supported.

ESP32 integrates an 8 MB SPI flash and an 8 MB PSRAM for more memory space.

Crystal Oscillators
The module uses a 40-MHz crystal oscillator.

RTC and Low-Power Management
With the use of advanced power-management technologies, ESP32 can switch between different power modes.

Electrical Characteristics

Absolute Maximum Ratings
Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only and do not refer to the functional operation of the device that should follow the recommended operating conditions.

Table 3: Absolute Maximum Ratings

1. The module worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to the ground. Please note that pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

Recommended Operating Conditions
Table 4: Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I $V DD$	Currently delivered by the external power supply	0.5	–	–	A
T	Operating temperature	–40	–	65	°C

DC Characteristics (3.3 V, 25 °C)

Table 5: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
C_{IN}	Pin capacitance		–	2	–	pF
V_{IH}	High-level input voltage		0.75×VDD1	–	VDD1+0.3	V
V_{IL}	Low-level input voltage		–0.3	–	0.25×VDD1	V
I_{IH}	High-level input current		–	–	50	nA
I_{IL}	Low-level input current		–	–	50	nA
V_{OH}	High-level output voltage		0.8×VDD1	–	–	V
V_{OL}	Low-level output voltage		–	–	0.1×VDD1	V
I_{OH}	High-level source current (V_{DD1} = 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain 1 ; 2	–	40	–	mA
		VDD3P3_RTC power domain 1 ; 2	–	40	–	mA
		VDD_SDIO power domain 1 ; 3	–	20	–	mA

I *OL*	Low-level sink current (VDD1 = 3.3 V, V*OL* = 0.495 V, output drive strength set to the maximum)	–	28	–	mA
R *P U*	Resistance of internal pull-up resistor	–	45	–	kΩ
R *P D*	Resistance of internal pull-down resistor	–	45	–	kΩ
V *IL_nRST*	Low-level input voltage of CHIP_PU to power off the chip	–	–	0.6	V

Notes:

1. VDD is the I/O voltage for a particular power domain of pins.
2. For the VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, VOH>=2.64 V, as the number of current-source pins increases.
3. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

Wi-Fi Radio
Table 6: Wi-Fi Radio Characteristics

Parameter	Condition	Min	Typical	Max	Unit
Operating frequency range *note* 1	–	2412	–	2462	MHz
TX power *note*2	802.11b:26.62dBm;802.11g:25.91dBm 802.11n20:25.89dBm;802.11n40:26.51dBm				dBm
Sensitivity	11b, 1 Mbps	–	–98	–	dBm
	11b, 11 Mbps	–	–89	–	dBm
	11g, 6 Mbps	–	–92	–	dBm
	11g, 54 Mbps	–	–74	–	dBm
	11n, HT20, MCS0	–	–91	–	dBm
	11n, HT20, MCS7	–	–71	–	dBm
	11n, HT40, MCS0	–	–89	–	dBm
	11n, HT40, MCS7	–	–69	–	dBm
Adjacent channel rejection	11g, 6 Mbps	–	31	–	dB
	11g, 54 Mbps	–	14	–	dB
	11n, HT20, MCS0	–	31	–	dB
	11n, HT20, MCS7	–	13	–	dB

1. The device should operate in the frequency range allocated by regional regulatory authorities. The target operating frequency range is configurable by software.
2. For the modules that use IPEX antennas, the output impedance is 50 Ω. For other modules without IPEX antennas, users do not need to be concerned about the output impedance.
3. Target TX power is configurable based on device or certification requirements.

Bluetooth/BLE

Radio 4.5.1 Receiver
Table 7: Receiver Characteristics – Bluetooth/BLE

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	–	–	–97	–	dBm
Maximum received signal @30.8% PER	–	0	–	–	dBm
Co-channel C/I	–	–	+10	–	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	–	–5	–	dB
	F = F0 – 1 MHz	–	–5	–	dB
	F = F0 + 2 MHz	–	–25	–	dB
	F = F0 – 2 MHz	–	–35	–	dB
	F = F0 + 3 MHz	–	–25	–	dB
	F = F0 – 3 MHz	–	–45	–	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	–	–	dBm
	2000 MHz ~ 2400 MHz	–27	–	–	dBm
	2500 MHz ~ 3000 MHz	–27	–	–	dBm
	3000 MHz ~ 12.5 GHz	–10	–	–	dBm
Intermodulation	–	–	–36	–	dBm

Transmitter

Table 8: Transmitter Characteristics – Bluetooth/BLE

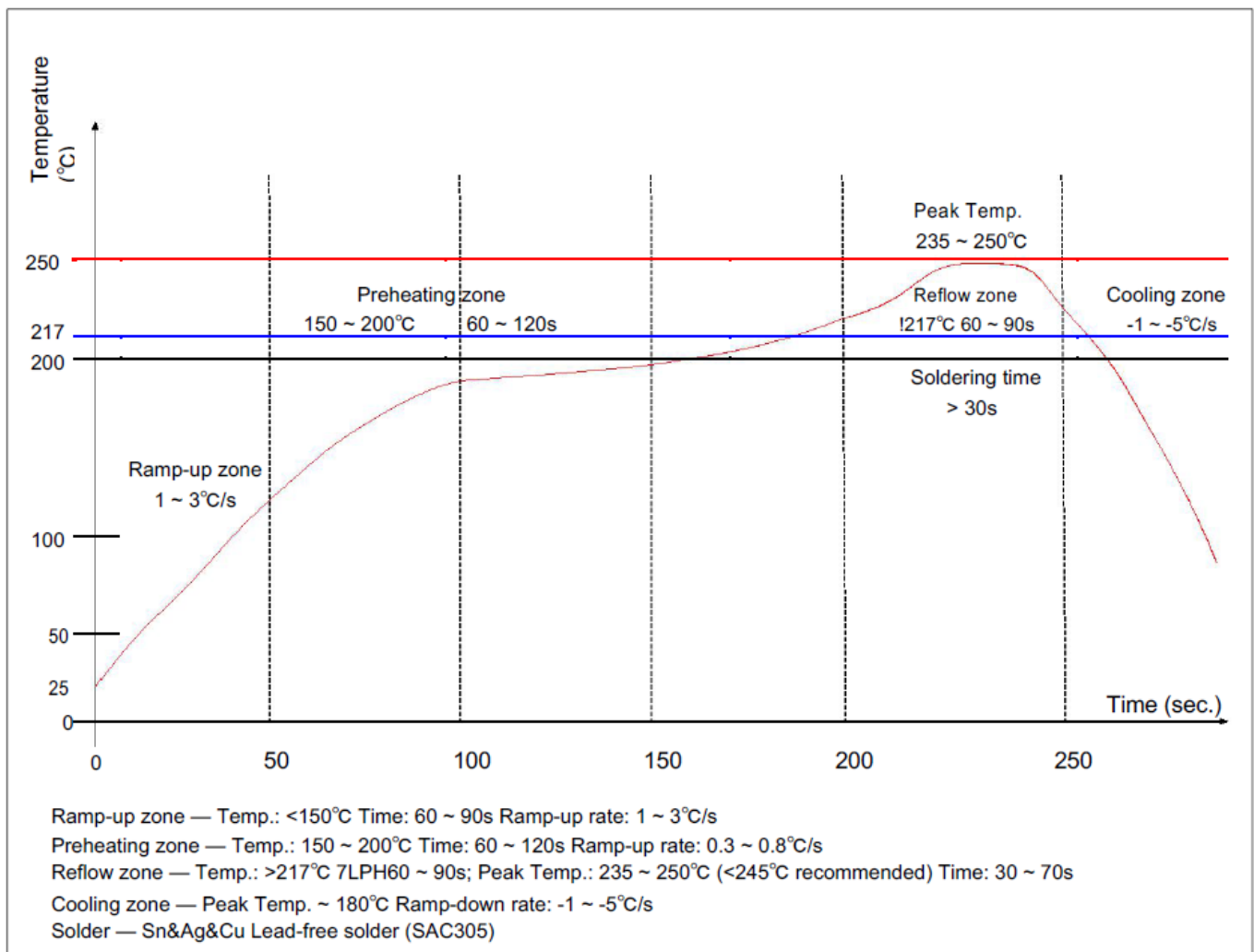| Parameter	Conditions	Min	Typ	Max	Unit
RF frequency	–	2402	–	2480	dBm
Gain control step	–	–	–	–	dBm
RF power	BLE:6.80dBm;BT:8.51dBm				dBm
Adjacent channel transmits power	F = F0 ± 2 MHz	–	–52	–	dBm
	F = F0 ± 3 MHz	–	–58	–	dBm
	F = F0 ± > 3 MHz	–	–60	–	dBm
Δ f1avg	–	–	–	265	kHz
Δ f2 max	–	247	–	–	kHz
Δ f2avg/Δ f1avg	–	–	–0.92	–	–
ICFT	–	–	–10	–	kHz
Drift rate	–	–	0.7	–	kHz/50 s
Drift	–	–	2	–	kHz

Reflow Profile

Figure 2: Reflow Profile

- **Ramp-up zone — Temp.:** <150°C Time: 60 ~ 90s Ramp-up rate: 1 ~ 3°C/s
- **Preheating zone — Temp.:** 150 ~ 200°C Time: 60 ~ 120s Ramp-up rate: 0.3 ~ 0.8°C/s
- **Reflow zone — Temp.:** >217°C 7LPH60 ~ 90s; Peak Temp.: 235 ~ 250°C (<245°C recommended) Time: 30 ~ 70s
- **Cooling zone — Peak Temp.** ~ 180°C Ramp-down rate: -1 ~ -5°C/s
- **Solder — Sn&Ag&Cu** Lead-free solder (SAC305)

OEM Guidance

1. **Applicable FCC rules**

   This module is granted by Single Modular Approval. It complies with the requirements of FCC part 15C, section 15.247 rules.

2. **The specific operational use conditions**

   This module can be used in IoT devices. The input voltage to the module is nominally 3.3V-3.6 V DC. The operational ambient temperature of the module is –40 °C ~ 65 °C. Only the embedded PCB antenna is allowed. Any other external antenna is prohibited.

3. Limited module procedures

   N/A

4. Trace antenna design

N/A

5. **RF exposure considerations**

The equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator and your body. If the equipment is built into a host as a portable usage, an additional RF exposure evaluation may be required as specified by 2.1093.

6. **Antenna**

    1. **Antenna type:** PCB antenna Peak gain: 3.40dBi
    2. Omni antenna with IPEX connector Peak gain2.33dBi

7. **Label and compliance information**

An exterior label on OEM's end product can use wording such as the following: "Contains Transmitter Module FCC ID: 2BFGS-ESP32WROVERE" or "Contains FCC ID: 2BFGS-ESP32WROVERE."

8. **Information on test modes and additional testing requirements**

    - The modular transmitter has been fully tested by the module grantee on the required number of channels, modulation types, and modes, it should not be necessary for the host installer to re-test all the available transmitter modes or settings. It is recommended that the host product manufacturer, installing the modular transmitter, perform some investigative measurements to confirm that the resulting composite system does not exceed the spurious emissions limits or band edge limits (e.g., where a different antenna may be causing additional emissions).

    - The testing should check for emissions that may occur due to the intermixing of emissions with the other transmitters, digital circuitry, or due to the physical properties of the host product (enclosure). This investigation is especially important when integrating multiple modular transmitters where the certification is based on testing each of them in a stand-alone configuration. It is important to note that host product manufacturers should not assume that because the modular transmitter is certified they do not have any responsibility for final product compliance.

    - If the investigation indicates a compliance concern the host product manufacturer is obligated to mitigate the issue. Host products using a modular transmitter are subject to all the applicable individual technical rules as well as to the general conditions of operation in Sections 15.5, 15.15, and 15.29 to not cause interference. The operator of the host product will be obligated to stop operating the device until the interference has been corrected.

9. Additional testing, Part 15 Subpart B disclaimer The final host/module combination needs to be evaluated against the FCC Part 15B criteria for unintentional radiators to be properly authorized for operation as a Part 15 digital device.

The host integrator installing this module into their product must ensure that the final composite product complies with the FCC requirements by a technical assessment or evaluation of the FCC rules, including the transmitter operation and should refer to the guidance in KDB 996369. For host products with certified modular transmitters, the frequency range of investigation of the composite system is specified by rule in Sections 15.33(a)(1) through (a)(3), or the range applicable to the digital device, as shown in Section 15.33(b)(1), whichever is the higher frequency range of investigation When testing the host product, all the transmitters must be operating. The transmitters can be enabled by using publicly-available drivers and turned on, so the transmitters are active. In certain conditions, it might be appropriate to use a technology-specific call box (test set) where accessory 50 devices or drivers are not available. When testing for emissions from the unintentional radiator, the transmitter shall be placed in the receive mode or idle mode, if possible. If receive mode only is not possible then, the radio shall be passive (preferred) and/or active scanning. In these cases, this would need to enable activity on the communication BUS (i.e., PCIe, SDIO, USB) to ensure the unintentional radiator circuitry is enabled. Testing laboratories may need to add attenuation or filters depending on the signal strength of any active beacons (if

applicable) from the enabled radio(s). See ANSI C63.4, ANSI C63.10 and ANSI C63.26 for further general testing details.

The product under test is set into a link/association with a partnering device, as per the normal intended use of the product. To ease testing, the product under test is set to transmit at a high-duty cycle, such as by sending a file or streaming some media content.

FCC Warning:
Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation

Documents / Resources

ESP32 User Manual	**Walfront ESP32 WiFi and Bluetooth Internet of Things Module** [pdf] User Manual ESP32, ESP32 WiFi and Bluetooth Internet of Things Module, WiFi and Bluetooth Internet of Things Module, Bluetooth Internet of Things Module, Internet of Things Module, Things Module, Module

References

- **User Manual**