VISHAY SUM70042E-GE3 Discrete Semiconductor User Guide

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Contents

VISHAY SUM70042E-GE3 Discrete Semiconductor

Product Information

Specifications

- Brand: Vishay Siliconix
- Type: N-Channel MOSFET
- Drain-Source Voltage (VDS): 100V
- RDS(on) max. at VGS = 10V: 0.0040 ohms
- RDS(on) max. at VGS = 7.5V: 0.0045 ohms
- Gate Charge (Qg): 84nC
- Continuous Drain Current (ID): 150A
- Package Type: TO-263

Features
For detailed features, please refer to www.vishay.com/doc?99912.

Applications
This N-Channel MOSFET is commonly used in applications requiring high power switching.

Ordering Information
Package Lead (Pb)-free and halogen-free TO-263 SUM70042E-GE3

Thermal Resistance Ratings

- Junction-to-Ambient: 40°C/W
- Junction-to-Case: 0.55°C/W

Operating Conditions

Operating Junction and Storage Temperature Range: -55 to +175°C

Product Usage Instructions

Installation

1. Ensure proper grounding before installation.
2. Mount the MOSFET securely on a suitable PCB using appropriate insulation materials.
3. Connect the drain, gate, and source terminals correctly as per the circuit design.

Operation

1. Apply the recommended gate voltage for the desired operation.
2. Avoid exceeding the maximum rated drain-source voltage during operation.
3. Monitor the thermal conditions to prevent overheating.

Maintenance

1. Regularly inspect the MOSFET for any physical damage.
2. Ensure proper ventilation for heat dissipation.

Disposal
Dispose of the MOSFET according to local regulations for electronic waste disposal.

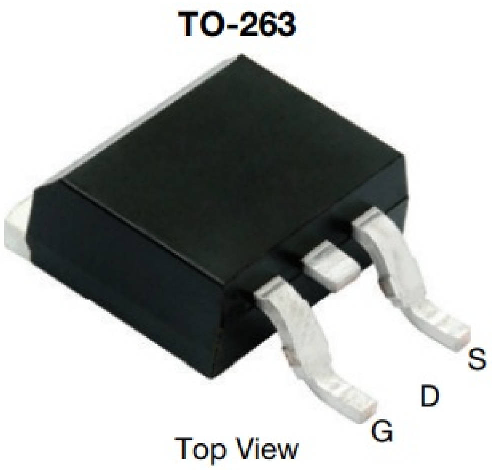
FAQs

Q: What is the maximum drain-source voltage for this MOSFET?
A: The maximum drain-source voltage is 100V.

Q: What is the maximum continuous drain current supported?
A: The MOSFET supports a maximum continuous drain current of 150A.

N-Channel 100 V (D-S) MOSFET

OVERVIEW



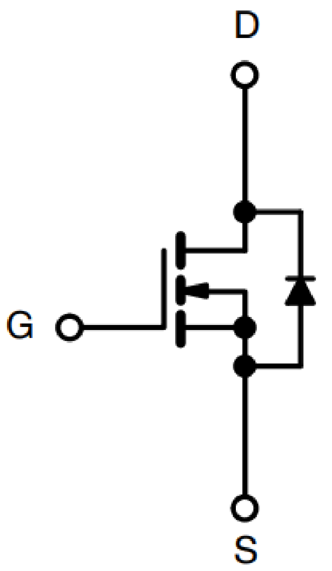
FEATURED

- TrenchFET® power MOSFET
- Maximum 175 °C junction temperature
- Very low Qgd reduces power loss from passing through Vplateau

- 100 % Rg and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Switching power supply
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management
- OR-ing / e-fuse



N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	100
$R_{DS(on)}$ max. (W) at V_{GS} = 10 V	0.0040
$R_{DS(on)}$ max. (W) at V_{GS} = 7.5 V	0.0045
Q_g typ. (nC)	84
I_D (A)	150 d
Configuration	Single

ORDERING INFORMATION

Package	TO-263
Lead (Pb)-free and halogen-free	SUM70042E-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		VDS	100	V
Gate-source voltage		VGS	± 20	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	150 d	A
	T_C = 70 °C		139	
Pulsed drain current (t = 100 μs)		IDM	200	
Avalanche current		IAS	50	
Single avalanche energy a	L = 0.1 mH	EAS	125	mJ
Maximum power dissipation a	T_C = 25 °C	P_D	278 b	W
	T_C = 125 °C		178 b	
Operating junction and storage temperature range		TJ, Tstg	-55 to +175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient (PCB mount) c	RthJA	40	°C/W
Junction-to-case (drain)	RthJC	0.55	

Notes

- Duty cycle ≤ 1 %
- See SOA curve for voltage derating
- When mounted on 1″ square PCB (FR4 material)
- Package limited

SPECIFICATIONS

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	VDS	V_{GS} = 0 V, I_D = 10 mA	100	–	–	V
Gate threshold voltage	VGS(th)	V_{DS} = V_{GS}, I_D = 250 μA	2	–	4	
Gate-body leakage	IGSS	V_{DS} = 0 V, V_{GS} = ± 20 V	–	–	± 250	nA
		V_{DS} = 100 V, V_{GS} = 0 V	–	–	1	

Zero gate voltage drain current	IDSS	V_{DS} = 100 V, V_{GS} = 0 V, T_J = 125 °C	–	–	150	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 175 °C	–	–	5	mA
On-state drain current a	ID(on)	V_{DS} ³ 10 V, V_{GS} = 10 V	50	–	–	A
Drain-source on-state resistance a	RDS(on)	V_{GS} = 10 V, I_D = 20 A	–	0.0033	0.0040	W
		V_{GS} = 7.5 V, I_D = 15 A	–	0.0036	0.0045	
Forward transconductance a	gfs	V_{DS} = 15 V, I_D = 15 A	–	60	–	S
Dynamic b						
Input capacitance	Ciss	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	–	6490	–	pF
Output capacitance	Coss		–	570	–	
Reverse transfer capacitance	Crss		–	20	–	
Total gate charge c	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 20 A	–	84	110	nC
Gate-source charge c	Qgs		–	33.5	–	
Gate-drain charge c	Qgd		–	9.5	–	
Gate resistance	R_g	f = 1 MHz	0.26	1.3	2.6	W
Turn-on delay time c	td(on)	V_{DD} = 50 V, R_L = 5 W I_D @ 10 A, V_{GEN} = 10 V, R_g = 1 W	–	25	50	ns
Rise time c	t_r		–	18	36	
Turn-off delay time c	td(off)		–	45	90	
Fall time c	t_f		–	14	28	
Drain-Source Body Diode Ratings and Characteristics b (T_C = 25 °C)						
Pulsed current (t = 100 µs)	ISM		–	–	200	A
Forward voltage a	VSD	I_F = 10 A, V_{GS} = 0 V	–	0.8	1.5	V
Reverse recovery time	trr	I_F = 10 A, di/dt = 100 A/µs	–	58	116	ns
Peak reverse recovery charge	IRM(REC)		–	3.9	5.9	A
Reverse recovery charge	Qrr		–	126	189	µC
Reverse recovery fall time	t_a		–	42	–	ns
Reverse recovery rise time	t_b		–	16	–	

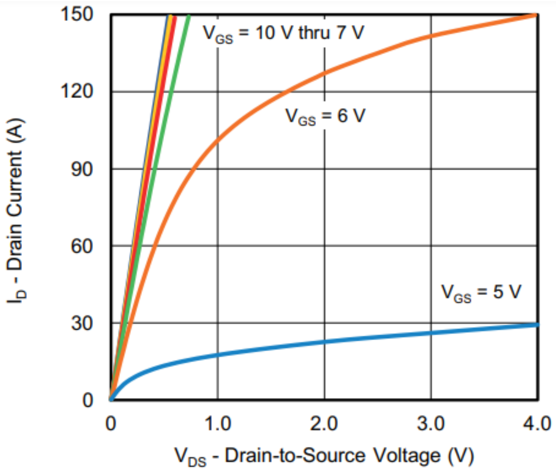
Notes

- Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

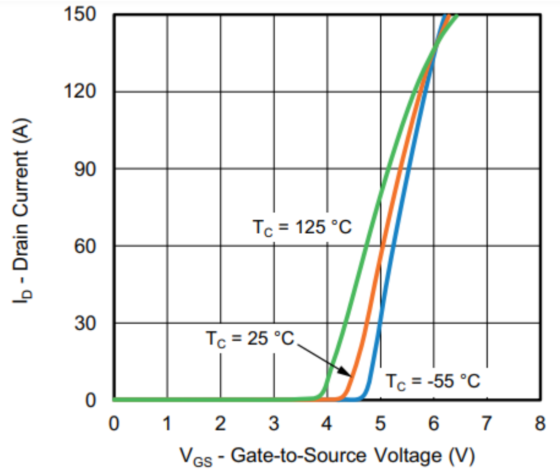
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS

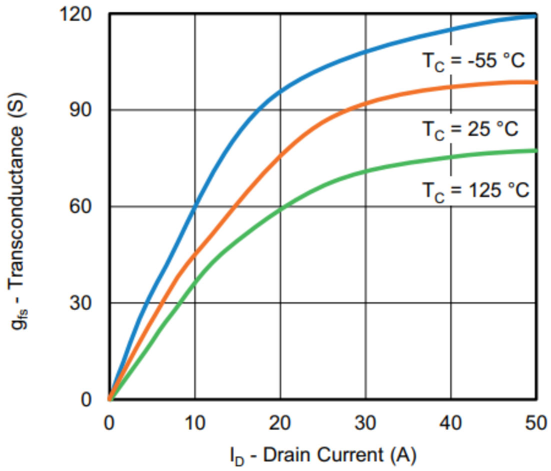
(TA = 25 °C, unless otherwise noted)



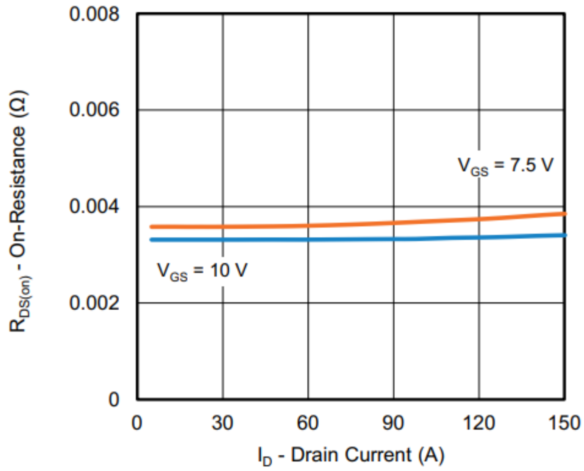
Output Characteristics



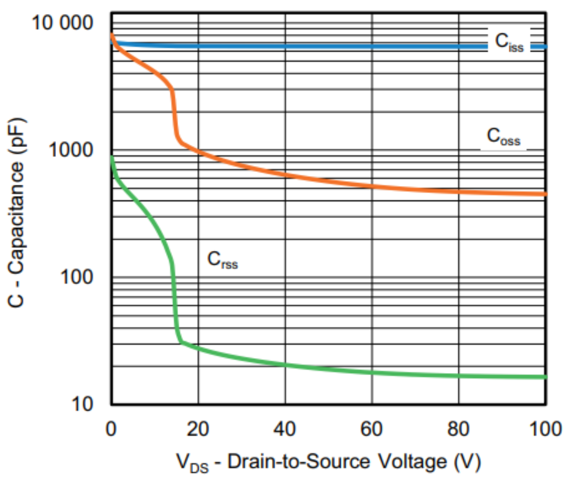
Transfer Characteristics



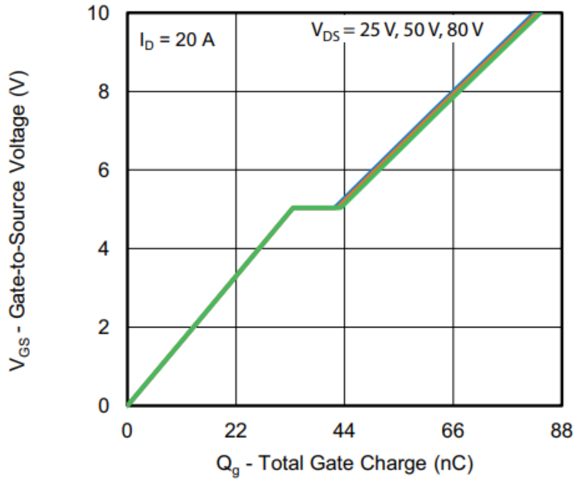
Transconductance



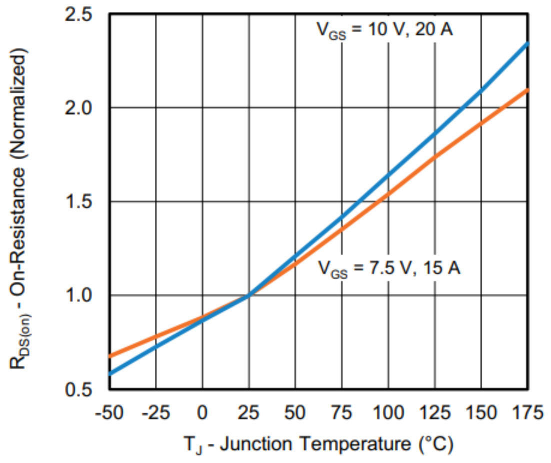
On-Resistance vs. Drain Current



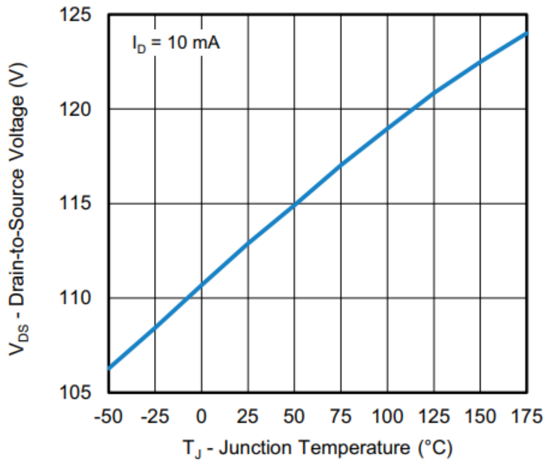
Capacitance



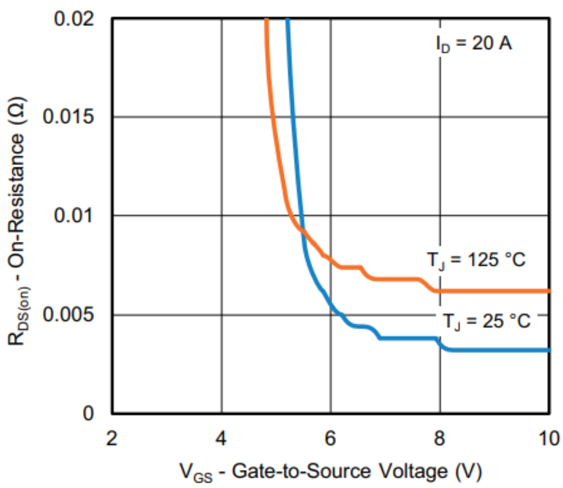
Gate Charge



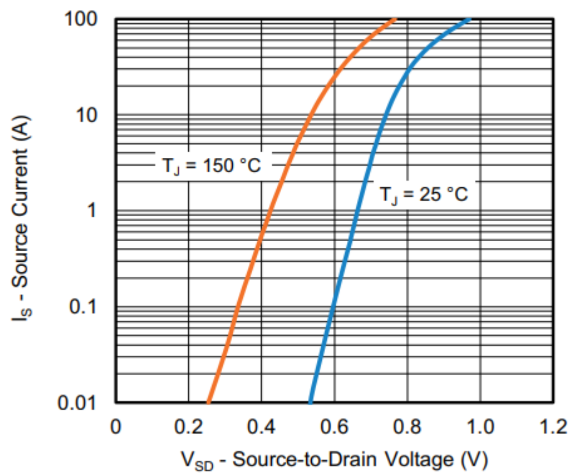
On-Resistance vs. Junction Temperature



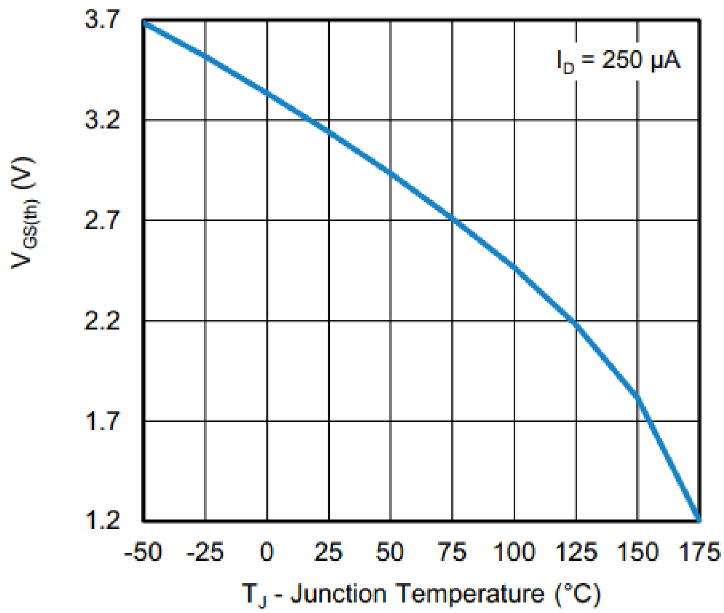
Drain Source Breakdown vs. Junction Temperature



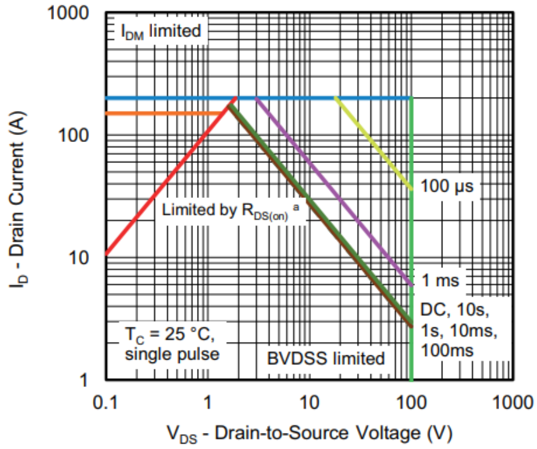
On-Resistance vs. Gate-to-Source Voltage



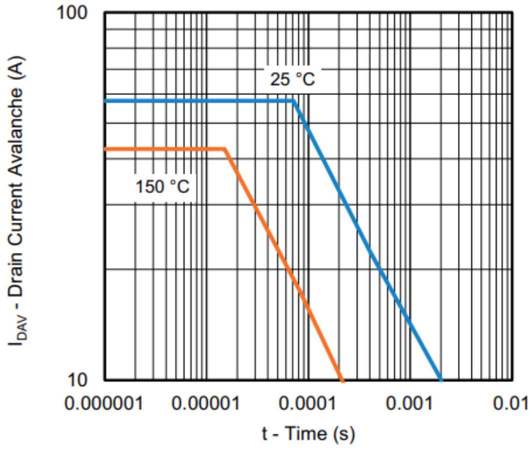
Source Drain Diode Forward Voltage



Threshold Voltage



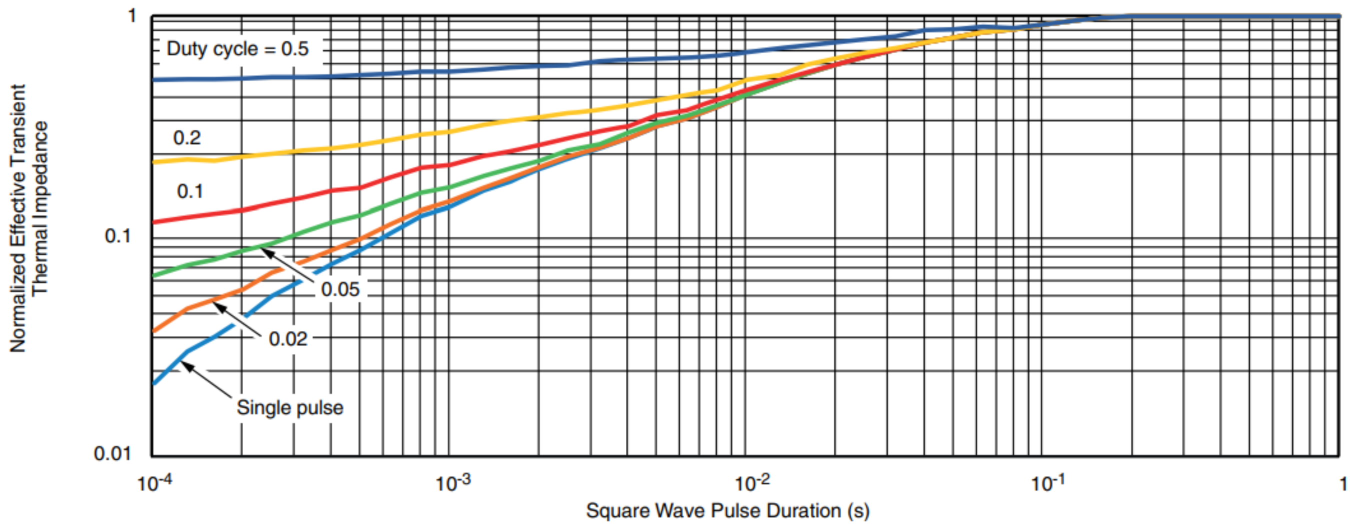
Safe Operating Area



Single Pulse Avalanche Current Capability vs. Time

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Case

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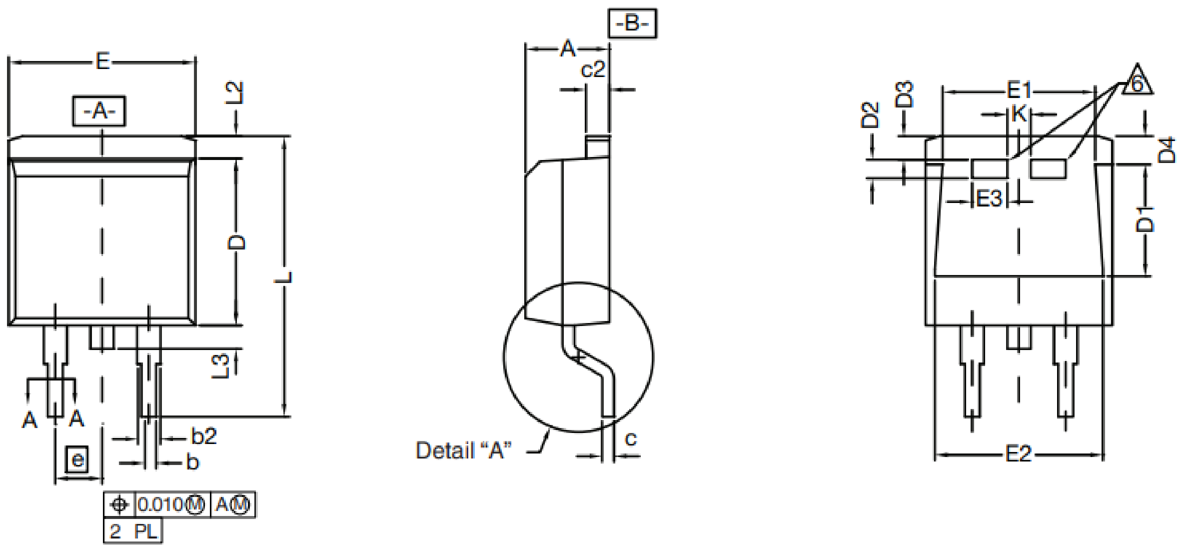
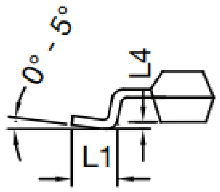
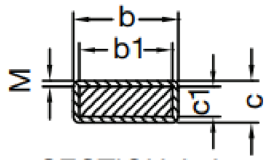
TO-263 (D2PAK): 3-LEAD





DETAIL A (ROTATED 90°)



SECTION A-A

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	–	6.223	–
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		–	0.002	–	0.050
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843					

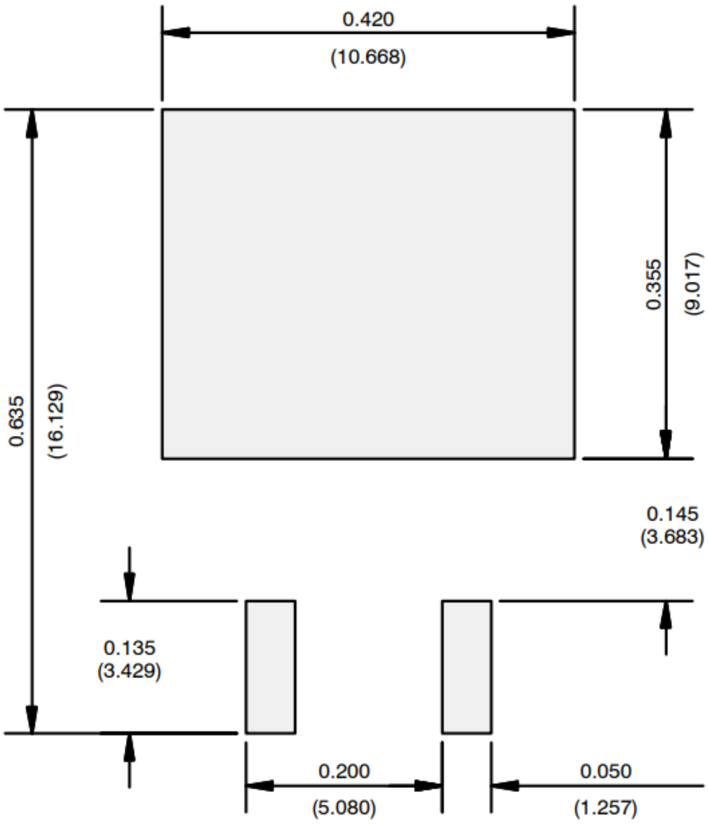
Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.

3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

RECOMMENDED

RECOMMENDED MINIMUM PADS FOR D2PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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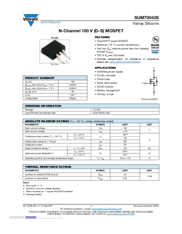	VISHAY SUM70042E-GE3 Discrete Semiconductor [pdf] User Guide SUM70042E-GE3 Discrete Semiconductor, SUM70042E-GE3, Discrete Semiconductor, Semiconductor

References

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