VISHAY SUM70040E Power Mosfet N Channel User Guide

Contents

VISHAY SUM70040E Power Mosfet N Channel

Product Specifications

- **Brand:** Vishay Siliconix
- **Type:** N-Channel MOSFET
- **Drain-Source Voltage (VDS):** 100V
- **RDS(on) Max:** 0.0040 at VGS = 10V, 0.0046 at VGS = 7.5V
- **ID (A):** 120A
- **Gate Charge (Qg):** 76
- **Package Type:** TO-263

Product Usage Instructions

Features

- Lead (Pb)-free and halogen-free
- For compliance definitions, refer to **www.vishay.com/doc?99912**

Applications

Designed for N-Channel MOSFET applications.

Thermal Resistance Ratings

- Junction-to-Ambient (PCB Mount): 40°C/W
- Junction-to-Case (Drain): 0.4°C/W

Frequently Asked Questions (FAQ)

- **What is the maximum Drain-Source Voltage for this MOSFET?**
  The maximum Drain-Source Voltage is 100V.
- **What is the Gate Charge for this MOSFET?**
  The Gate Charge is 76.
- **What is the maximum Drain Current supported by this MOSFET?**

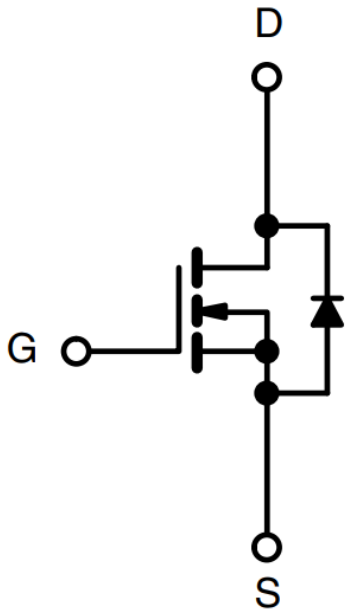
The maximum Drain Current is 120A.

FEATURES

- ThunderFET® power MOSFET
- Maximum 175 °C junction temperature
- 100 % Rg and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Power supply
  Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management
- OR-ing



N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (W) MAX.	I_D (A) d	Q_g (TYP.)
100	0.0040 at V_{GS} = 10 V	120	76
	0.0046 at V_{GS} = 7.5 V	120	

ABSOLUTE MAXIMUM RATINGS (TC = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		VDS	100	V
Gate-Source Voltage		VGS	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	120 d	A
	T_C = 70 °C		120 d	
Pulsed Drain Current (t = 100 µs)		IDM	480	
Avalanche Current		IAS	73	
Single Avalanche Energy a	L = 0.1 mH	EAS	266	mJ
Maximum Power Dissipation a	T_C = 25 °C	P_D	375 b	W
	T_C = 125 °C		125 b	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient (PCB Mount) c	RthJA	40	°C/W
Junction-to-Case (Drain)	RthJC	0.4	

Notes

- Duty cycle 1 %.
- See SOA curve for voltage derating.
- When mounted on 1″ square PCB (FR4 material).
- Package limited.

SPECIFICATIONS (TJ = 25 °C, unless otherwise noted)

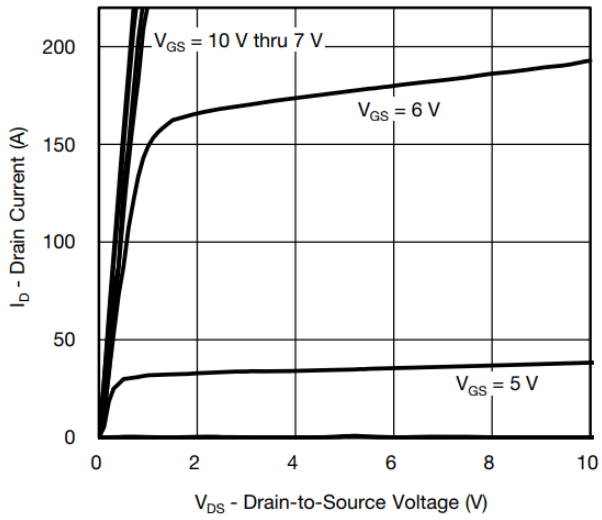
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	VDS	V_{GS} = 0 V, I_D = 250 µA	100	–	–	V
Gate Threshold Voltage	VGS(th)	V_{DS} = V_{GS}, I_D = 250 µA	2.5	–	4	
Gate-Body Leakage	IGSS	V_{DS} = 0 V, V_{GS} = ± 20 V	–	–	± 250	nA
Zero Gate Voltage Drain Current	IDSS	V_{DS} = 100 V, V_{GS} = 0 V	–	–	1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 125 °C	–	–	150	
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 175 °C	–	–	5	mA
On-State Drain Current a	ID(on)	V_{DS} ³ 10 V, V_{GS} = 10 V	120	–	–	A
Drain-Source On-State Resistance a	RDS(on)	V_{GS} = 10 V, I_D = 20 A	–	0.0032	0.0040	W
		V_{GS} = 7.5 V, I_D = 15 A	–	0.0035	0.0046	
Forward Transconductance a	gfs	V_{DS} = 15 V, I_D = 20 A	–	82	–	S
Dynamic b						
Input Capacitance	Ciss	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	–	5100	–	pF
Output Capacitance	Coss		–	2025	–	
Reverse Transfer Capacitance	Crss		–	165	–	
Total Gate Charge c	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 20 A	–	76	120	nC
Gate-Source Charge c	Qgs		–	23	–	
Gate-Drain Charge c	Qgd		–	17	–	
Gate Resistance	R_g	f = 1 MHz	0.6	3.3	6.6	W
Turn-On Delay Time c	td(on)	V_{DD} = 50 V, R_L = 5 W I_D @ 10 A, V_{GEN} = 10 V, R_g = 1 W	–	15	30	ns
Rise Time c	t_r		–	22	40	
Turn-Off Delay Time c	td(off)		–	55	100	
Fall Time c	t_f		–	15	30	
Drain-Source Body Diode Ratings and Characteristics b (T_C = 25 °C)						
Pulsed Current	ISM		–	–	480	A
Forward Voltage a	VSD	I_F = 10 A, V_{GS} = 0 V	–	0.8	1.5	V

Notes

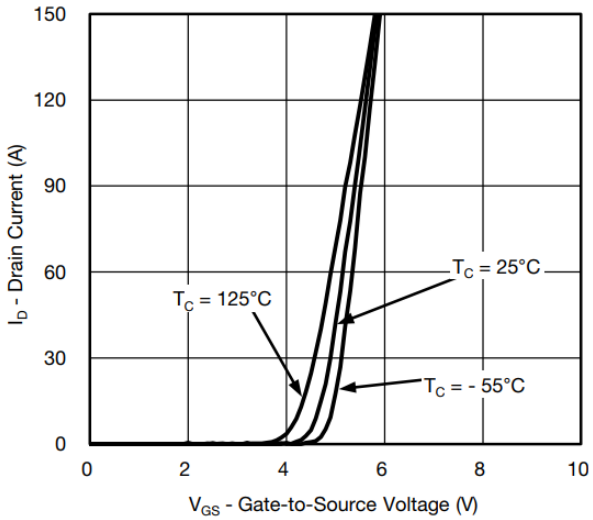
- Pulse test; pulse width 300 µs, duty cycle 2 %.

- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

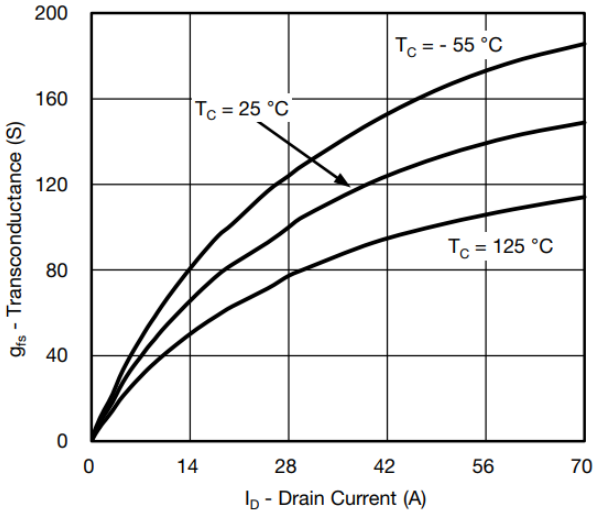
TYPICAL CHARACTERISTICS (TA = 25 °C, unless otherwise noted)



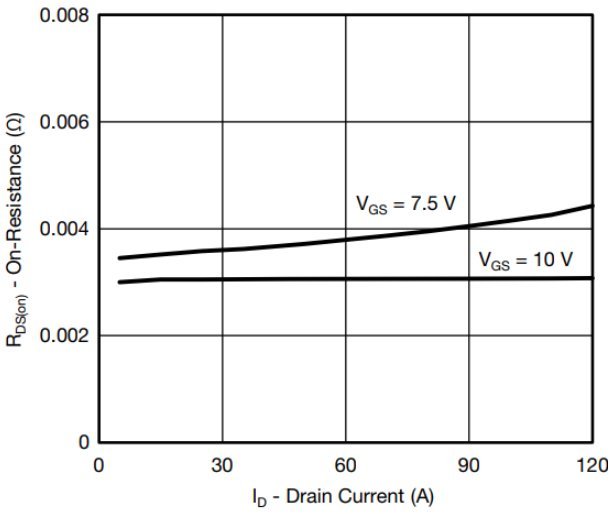
Output Characteristics



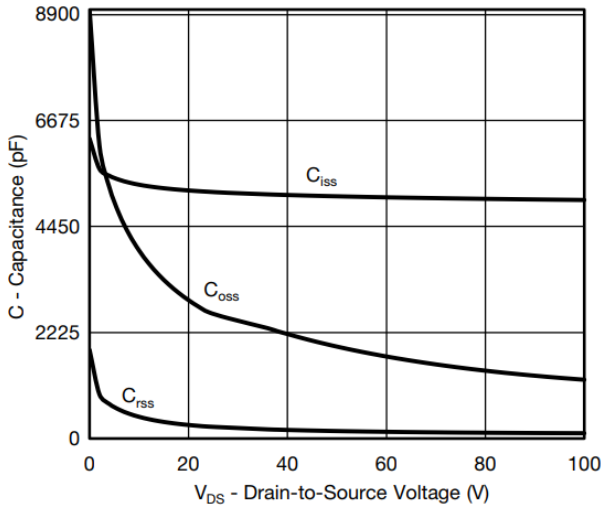
Transfer Characteristics



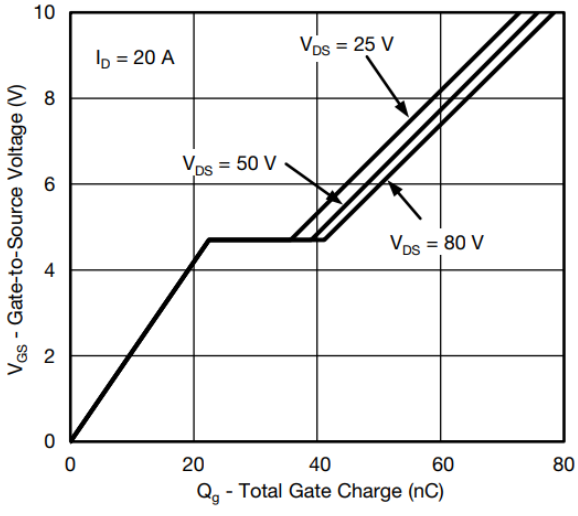
Transconductance



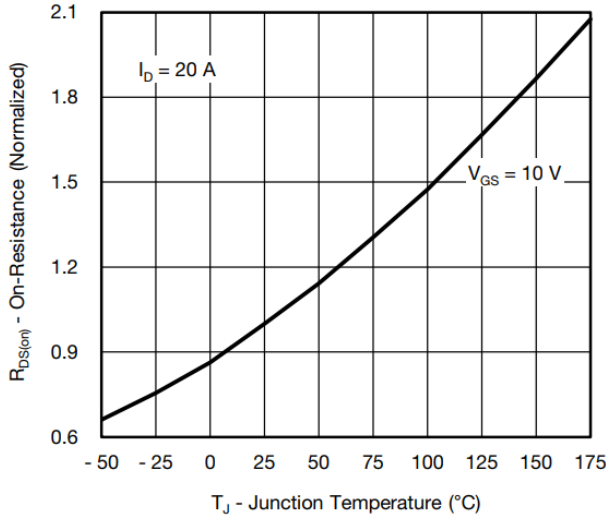
On-Resistance vs. Drain Current



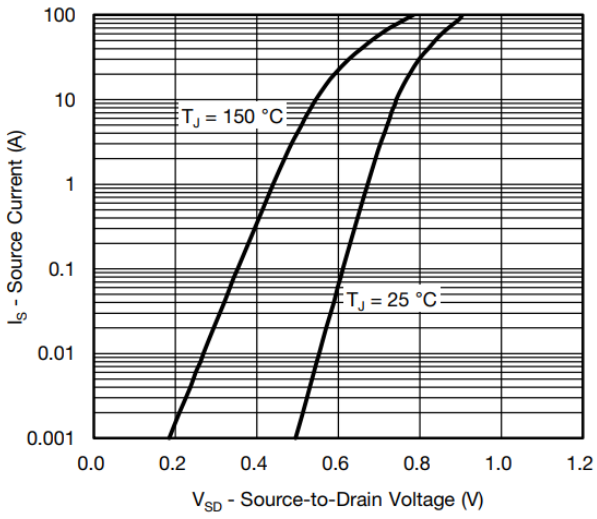
Capacitance



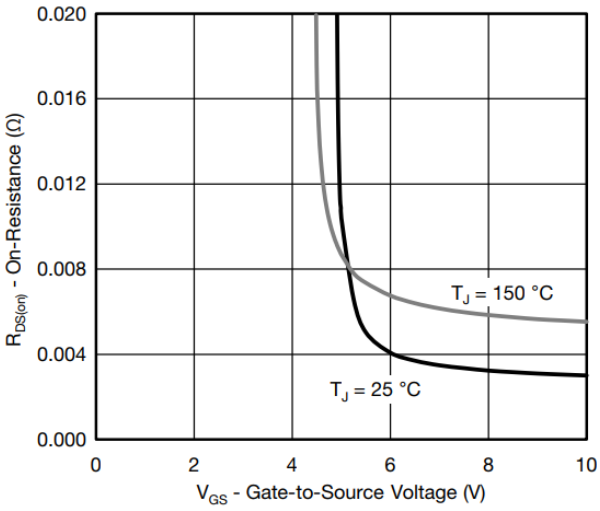
Gate Charge



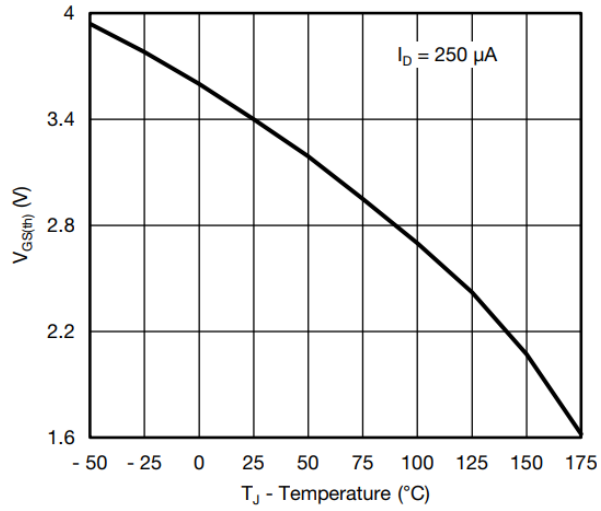
On-Resistance vs. Junction Temperature



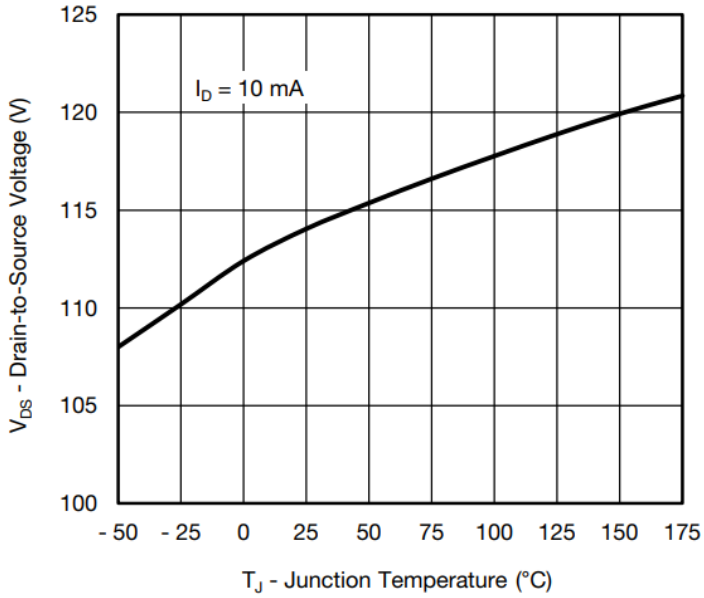
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

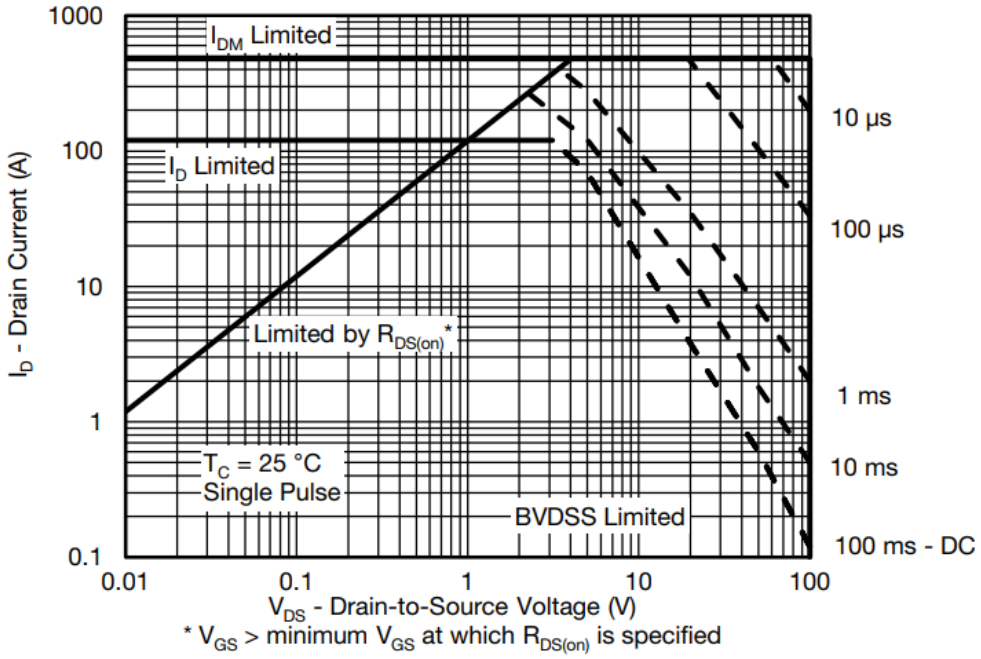


Threshold Voltage

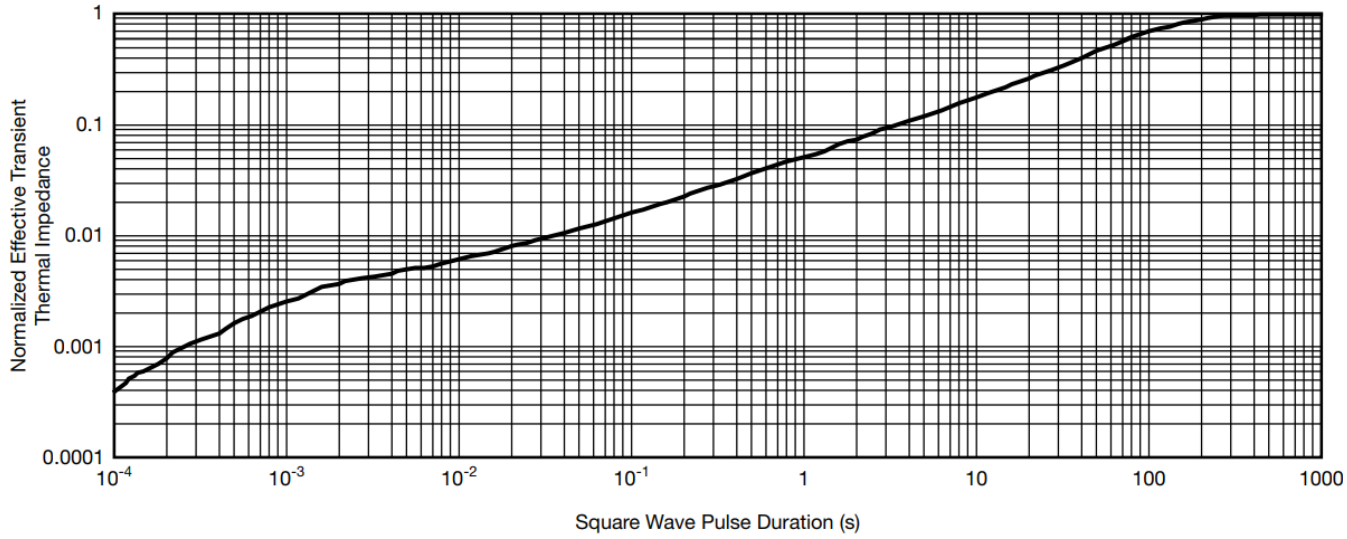


Drain Source Breakdown vs. Junction Temperature

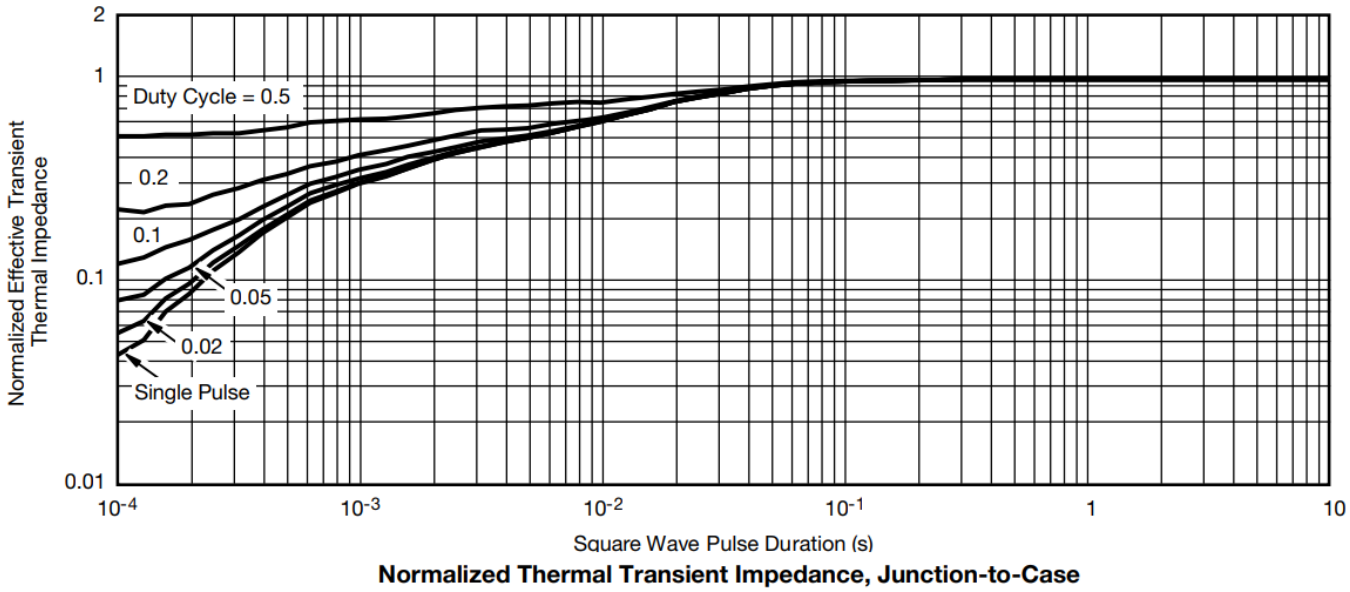
THERMAL RATINGS (TA = 25 °C, unless otherwise noted)



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

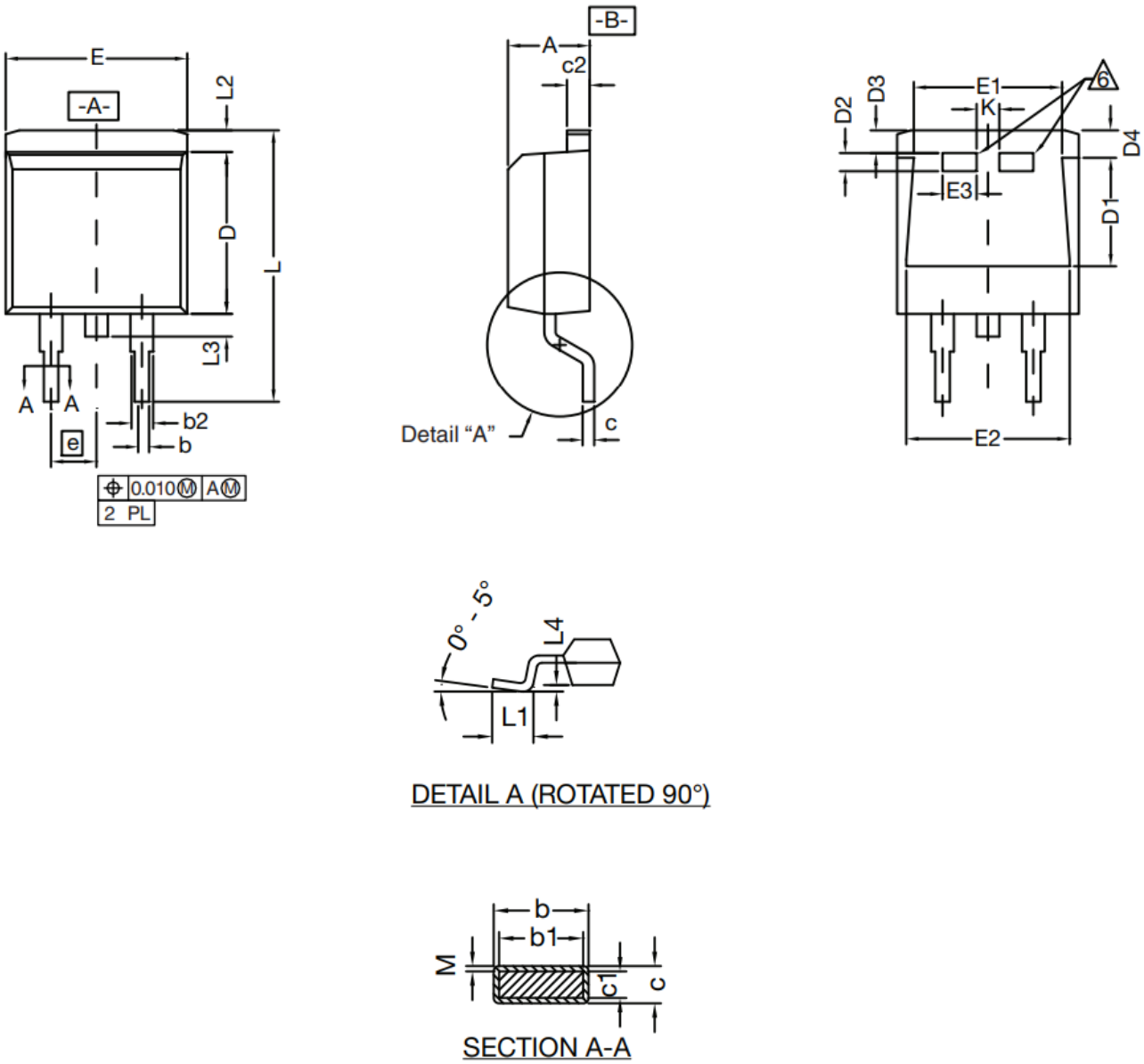
The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction to Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction to Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board – FR4, size 1″ x 1″ x 0.062″, double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Package Information

TO-263 (D2PAK): 3-LEAD

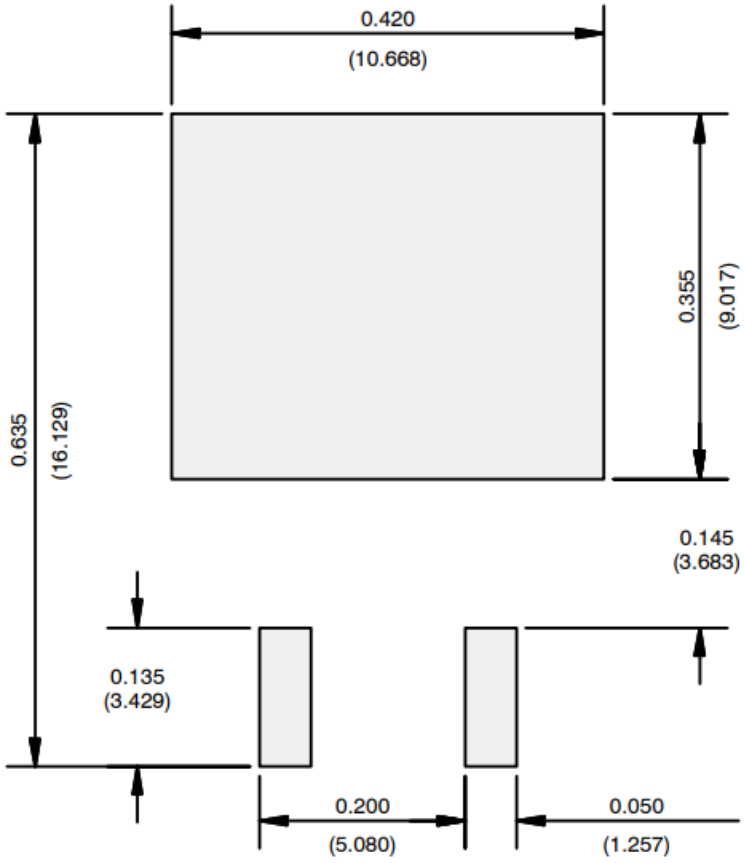


DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	–	6.223	–
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		–	0.002	–	0.050
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843					

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D2PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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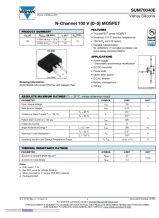	[VISHAY SUM70040E Power Mosfet N Channel](#) [pdf] User Guide SUM70040E Power Mosfet N Channel, SUM70040E, Power Mosfet N Channel, Mosfet N Chan nel, N Channel

References

- Vishay Intertechnology: Passives & Discrete Semiconductors
- vishay.com/doc?91000
- vishay.com/doc?99912
- SUM70040E MOSFETs | Vishay
- User Manual