SUM70030E N-Channel MOSFET

VISHAY SUM70030E N-Channel MOSFET Owner's Manual

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VISHAY SUM70030E N-Channel MOSFET

FEATURES

- TrenchFET® power MOSFET
- Maximum 175 °C junction temperature
- Very low Qgd reduces power loss from passing through Vplateau
- 100 % Rg and UIS tested
- Material categorization: for definitions of compliance please see **www.vishay.com/doc?99912**

APPLICATIONS

- Power supply
  Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management
- OR-ing / e-fuse

PRODUCT SUMMARY

V_{DS} (V)	100
$R_{DS(on)}$ max. (W) at V_{GS} = 10 V	0.00288
$R_{DS(on)}$ max. (W) at V_{GS} = 7.5 V	0.00348
Q_g typ. (nC)	142.4
I_D (A)	150 d
Configuration	Single

ORDERING INFORMATION

Package	TO-263
Lead (Pb)-free and halogen-free	SUM70030E-GE3

ABSOLUTE MAXIMUM RATINGS (TC = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		VDS	100	V
Gate-source voltage		VGS	± 20	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	150 d	A
	T_C = 70 °C		150 d	
Pulsed drain current (t = 100 µs)		IDM	500	
Avalanche current		IAS	60	
Single avalanche energy a	L = 0.1 mH	EAS	180	mJ
Maximum power dissipation a	T_C = 25 °C	P_D	375 b	W
	T_C = 125 °C		125 b	
Operating junction and storage temperature range		TJ, Tstg	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient (PCB mount) c	RthJA	40	°C/W
Junction-to-case (drain)	RthJC	0.4	

Notes

- Duty cycle 1 %
- See SOA curve for voltage derating
- When mounted on 1″ square PCB (FR4 material)
- Package limited

SPECIFICATIONS (TJ = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	VDS	V_{GS} = 0 V, I_D = 250 µA	100	–	–	

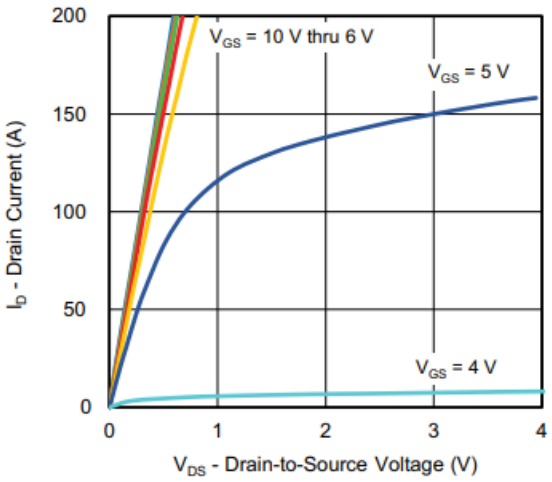
Gate threshold voltage	VGS(th)	V_{DS} = V_{GS}, I_D = 250 µA	2	–	4	V
Gate-body leakage	IGSS	V_{DS} = 0 V, V_{GS} = ± 20 V	–	–	± 250	nA
Zero gate voltage drain current	IDSS	V_{DS} = 100 V, V_{GS} = 0 V	–	–	1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 125 °C	–	–	150	
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 175 °C	–	–	5	mA
On-state drain current a	ID(on)	V_{DS} ³ 10 V, V_{GS} = 10 V	120	–	–	A
Drain-source on-state resistance a	RDS(on)	V_{GS} = 10 V, I_D = 30 A	–	0.00240	0.00288	W
		V_{GS} = 7.5 V, I_D = 20 A	–	0.00290	0.00348	
Forward transconductance a	gfs	V_{DS} = 15 V, I_D = 30 A	–	110	–	S
Dynamic b						
Input capacitance	Ciss	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	–	10 870	–	pF
Output capacitance	Coss		–	820	–	
Reverse transfer capacitance	Crss		–	40	–	
Total gate charge c	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 20 A	–	142.4	214	nC
Gate-source charge c	Qgs		–	46.8	–	
Gate-drain charge c	Qgd		–	18.5	–	
Output charge	Qoss	V_{DS} = 50 V, V_{GS} = 0 V	–	138	207	
Gate resistance	R_g	f = 1 MHz	0.34	1.7	3.4	W
Turn-on delay time c	td(on)	V_{DD} = 50 V, R_L = 3 W I_D @ 10 A, V_{GEN} = 10 V, R_g = 1 W	–	30	60	ns
Rise time c	t_r		–	13	26	
Turn-off delay time c	td(off)		–	50	100	
Fall time c	t_f		–	15	30	
Drain-Source Body Diode Ratings and Characteristics b (T_C = 25 °C)						
Pulsed current (t = 100 µs)	ISM		–	–	250	A
Forward voltage a	VSD	I_F = 10 A, V_{GS} = 0 V	–	0.8	1.5	V
Reverse recovery time	trr	I_F = 34 A, di/dt = 100 A/µs	–	76	150	ns
Peak reverse recovery charge	IRM(REC)		–	4.6	5.6	A
Reverse recovery charge	Qrr		–	0.205	0.24	µC
Reverse recovery fall time	t_a		–	52	–	ns

Reverse recovery rise time	t_b		–	24	–	

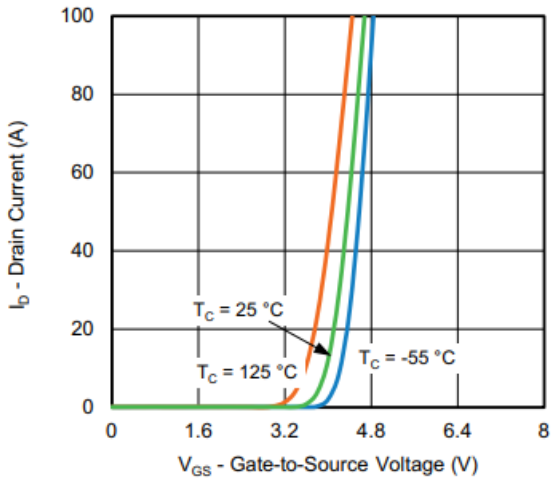
Notes

- Pulse test; pulse width 300 µs, duty cycle 2 %
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

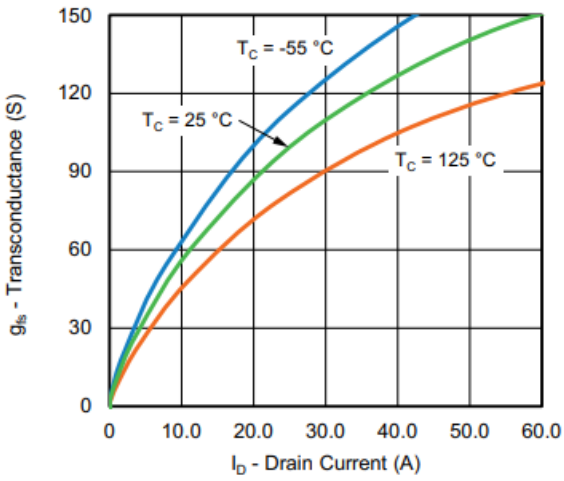
TYPICAL CHARACTERISTICS (TA = 25 °C, unless otherwise noted)



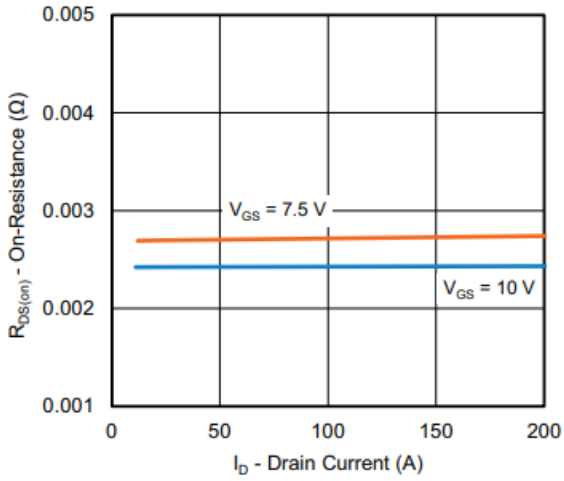
Output Characteristics



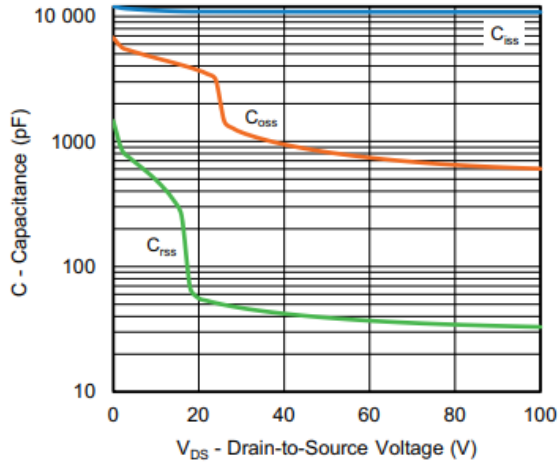
Transfer Characteristics



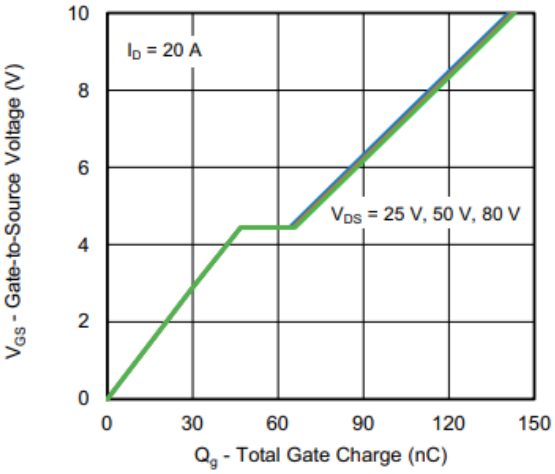
Transconductance



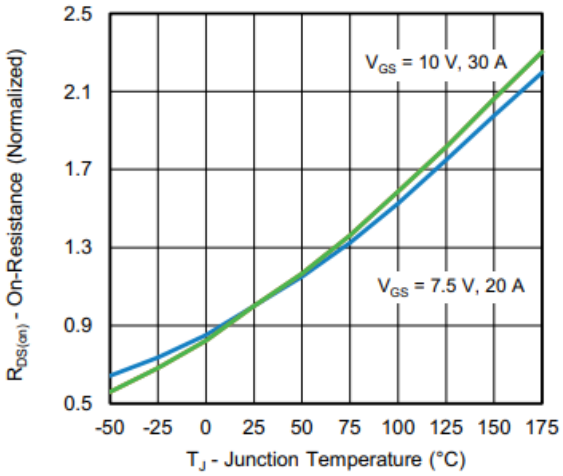
On-Resistance vs. Drain Current



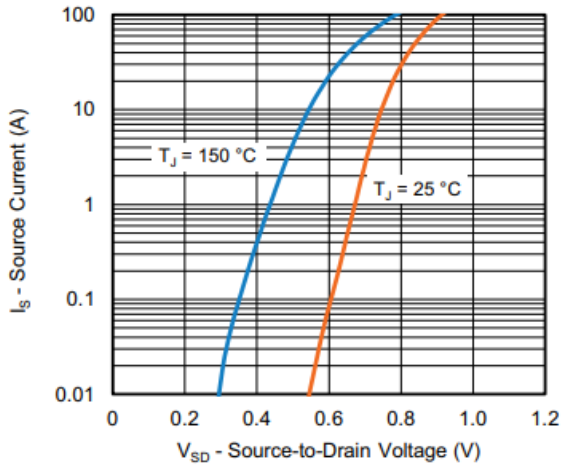
Capacitance



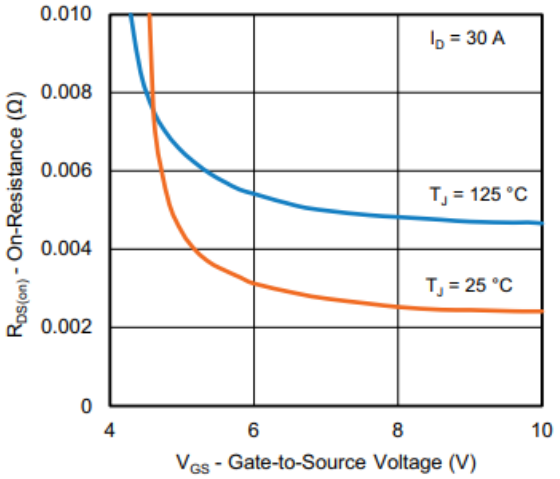
Gate Charge



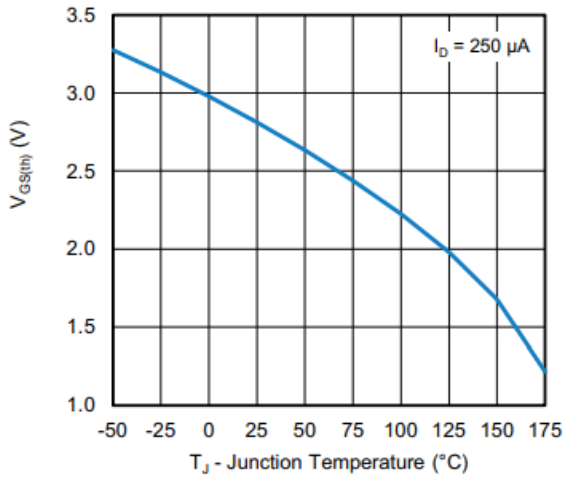
On-Resistance vs. Junction Temperature



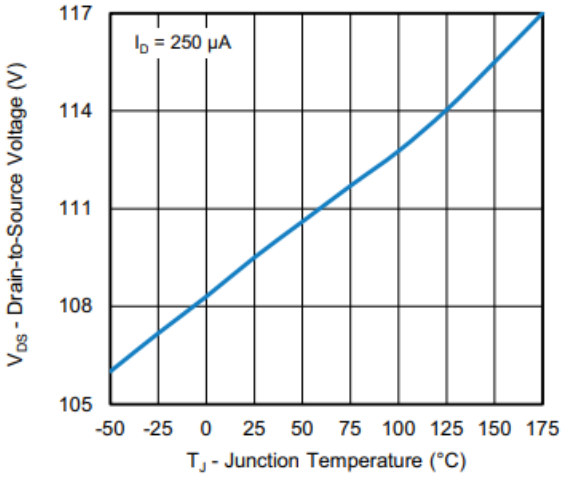
Source Drain Diode Forward Voltage



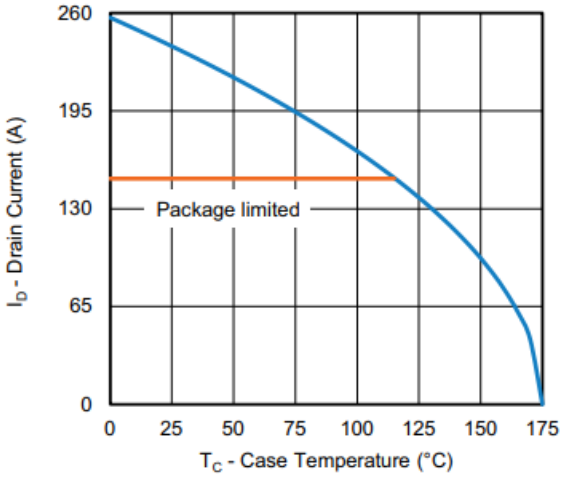
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

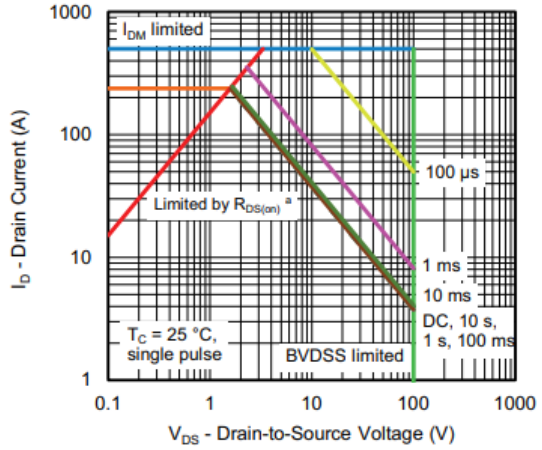


Drain Source Breakdown vs. Junction Temperature

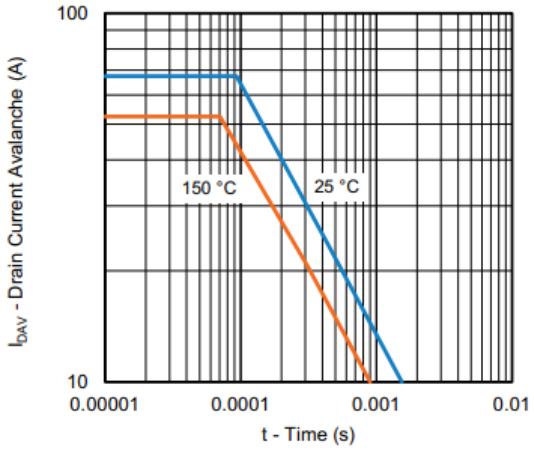


Current De-rating

THERMAL RATINGS (TA = 25 °C, unless otherwise noted)



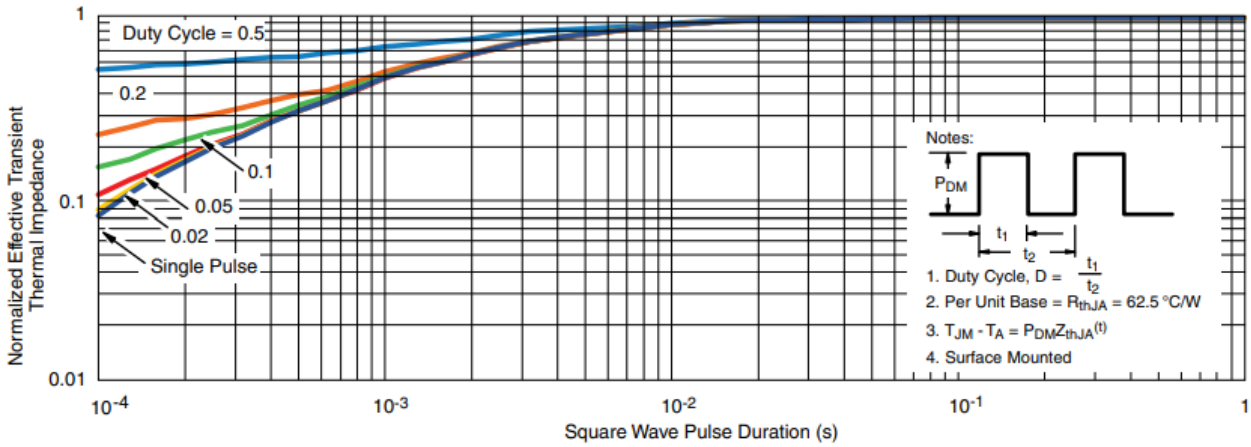
Safe Operating Area



Single Pulse Avalanche Current Capability vs. Time

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Case

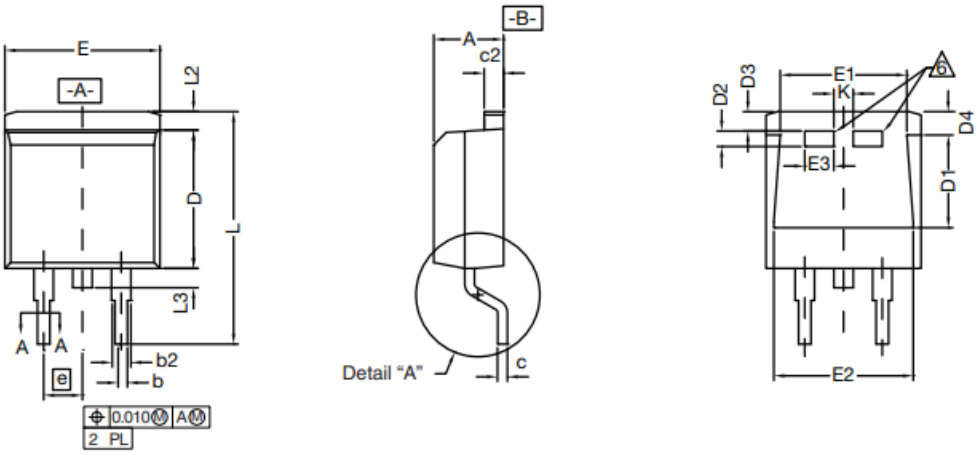
Note

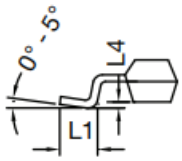
The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction to Ambient (25 °C)

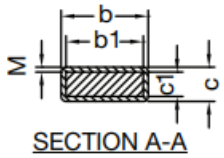
- Normalized Transient Thermal Impedance Junction to Case (25 °C) is a general guideline only to enable the user to get a “ballpark” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics developed from empirical measurements. The latter is valid for the part mounted on printed circuit board – FR4, size 1″ x 1″ x 0.062″, double-sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

TO-263 (D2PAK): 3-LEAD





DETAIL A (ROTATED 90°)



SECTION A-A

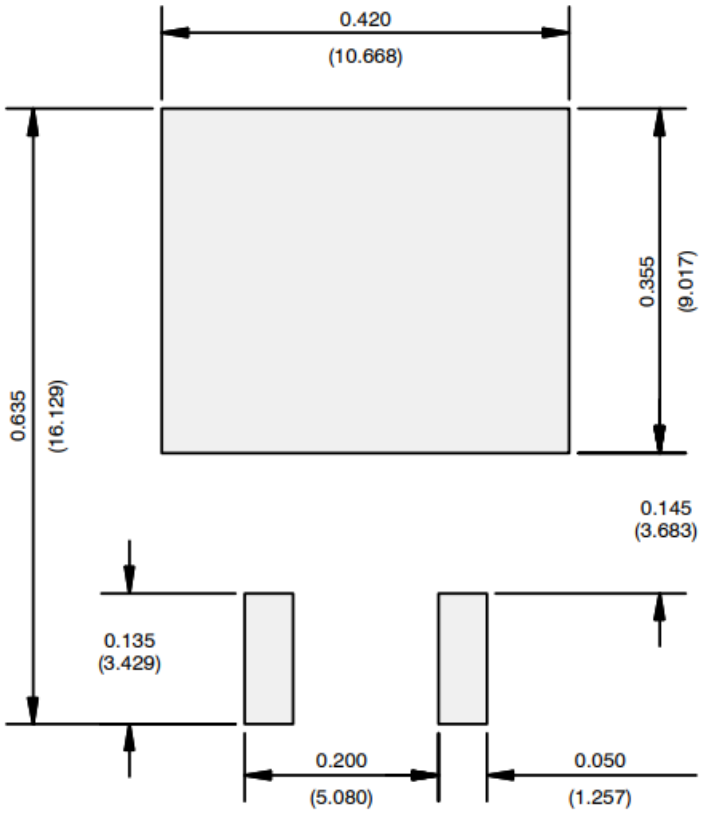
DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	–	6.223	–
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		–	0.002	–	0.050
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843					

Notes

1. Plane B includes the maximum features of the heat sink tab and plastic.
2. No more than 25 % of L1 can fall above the seating plane by max. 8 mils.

3. Pin-to-pin coplanarity max. 4 mils.
4. The thin lead is for SUB, and SYB.
   Thick lead is for SUM, SYM, and SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D2PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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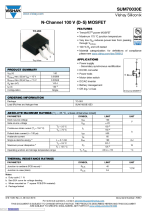
Documents / Resources

	VISHAY SUM70030E N-Channel MOSFET [pdf] Owner's Manual SUM70030E, SUM70030E-GE3, SUM70030E N-Channel MOSFET, SUM70030E, N-Channel MOSFET, MOSFET

References

- Vishay Intertechnology: Passives & Discrete Semiconductors
- User Manual