

VISHAY SiHS90N65E Power MOSFET Instruction Manual

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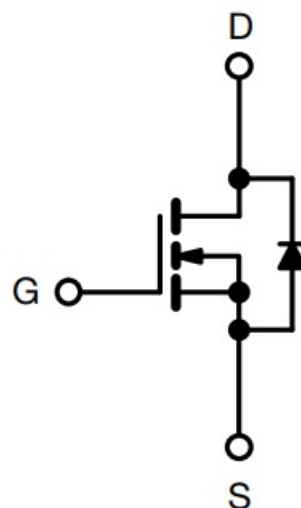
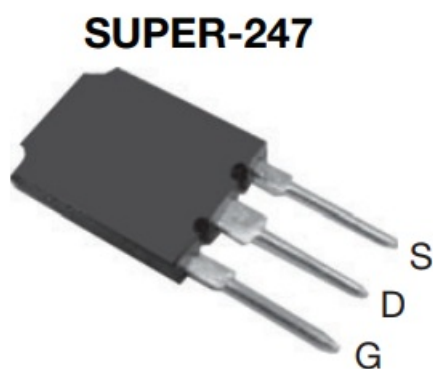
VISHAY SiHS90N65E Power MOSFET



FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS



N-Channel MOSFET

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ (W) typ. at 25 °C	$V_{GS} = 10\text{ V}$	0.025
Q_g (nC) max.	591	
Q_{gs} (nC)	84	
Q_{gd} (nC)	160	
Configuration	Single	

INFORMATION

ORDERING INFORMATION	
Package	Super-247
Lead (Pb)-free	SiHS90N65E-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			VDS	650	V
Gate-source voltage			VGS	± 30	
Continuous drain current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	I _D	87	A
		T _C = 100 °C		55	
Pulsed drain current a			IDM	323	
Linear derating factor				5	W/°C
Single pulse avalanche energy b			EAS	1930	mJ
Maximum power dissipation			P _D	625	W
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Drain-source voltage slope	T _J = 125 °C		dV/dt	41	V/ns
Reverse diode dV/dt d		4.1			
Soldering recommendations (peak temperature) c	for 10 s			300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- VDD = 140 V, starting $T_J = 25\text{ }^{\circ}\text{C}$, L = 28.2 mH, $R_g = 25\text{ }\Omega$, IAS = 11.7 A
- 1.6 mm from case
- $ISD \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	RthJA	—	40	$^{\circ}\text{C}/\text{W}$
Maximum junction-to-case (drain)	RthJC	—	0.2	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	VDS	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	—	—	V

V _{DS} temperature coefficient	DV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		–	0.83	–	V/°C
Gate threshold voltage (N)	V _{GS} (th)	V _{DS} = V _{GS} , I _D = 250 μA		2.0	–	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		–	–	± 10 0	nA
		V _{GS} = ± 30 V		–	–	± 1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V		–	–	1	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		–	–	25	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 45 A	–	0.025	0.029	W
Forward transconductance a	g _{fs}	V _{DS} = 30 V, I _D = 45 A		–	32	–	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 300 kHz		–	11826	–	pF
Output capacitance	C _{oss}			–	528	–	
Reverse transfer capacitance	C _{rss}			–	9	–	
Effective output capacitance, energy related a	Co(er)	V _{GS} = 0 V, V _{DS} = 0 V to 520 V		–	384	–	
Effective output capacitance, time related b	Co(tr)			–	1502	–	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 45 A, V _{DS} = 520 V	–	394	591	nC
Gate-source charge	Q _{gs}			–	84	–	
Gate-drain charge	Q _{gd}			–	160	–	
Turn-on delay time	t _{d(on)}	V _{DD} = 520 V, I _D = 45 A, V _{GS} = 10 V, R _g = 9.1 W		–	85	128	ns
Rise time	t _r			–	152	228	
Turn-off delay time	t _{d(off)}			–	323	485	
Fall time	t _f			–	267	401	
Gate input resistance	R _g	f = 1 MHz, open drain		0.6	1.2	2.4	W
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol D showing the integral reverse p – n junction diode S		–	–	87	A
Pulsed diode forward current	I _{SM}			–	–	323	

Diode forward voltage	VSD	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 45\text{ A}$, $V_{GS} = 0\text{ V}$	–	0.9	1.2	V
Reverse recovery time	trr	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 45\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$	–	971	1942	ns
Reverse recovery charge	Qrr		–	26	52	μC
Reverse recovery current	IRRM		–	42	–	A

Notes

- $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
- $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

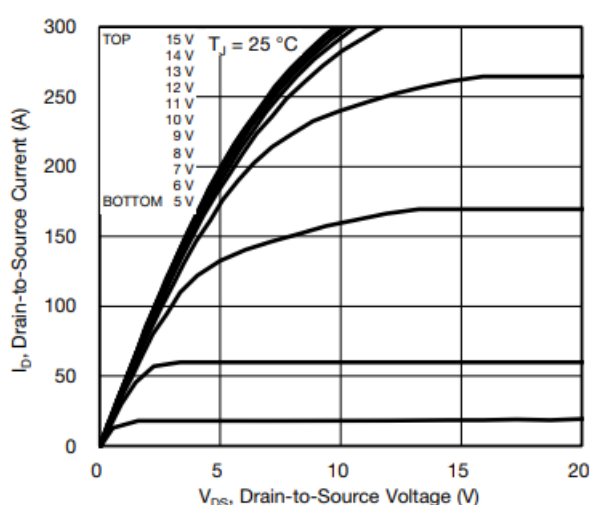


Fig. 1 - Typical Output Characteristics

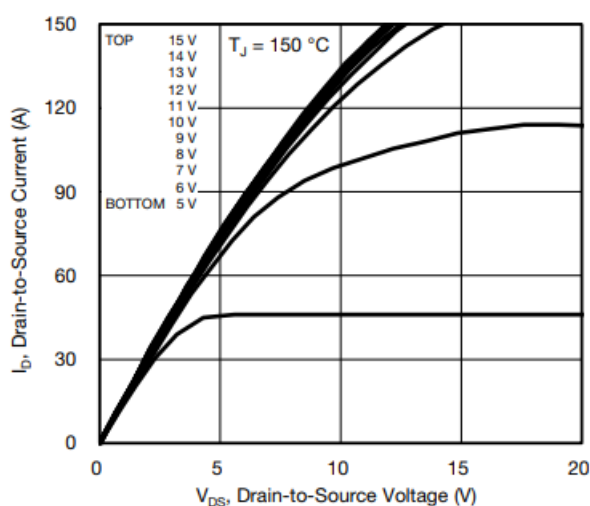


Fig. 2 - Typical Output Characteristics

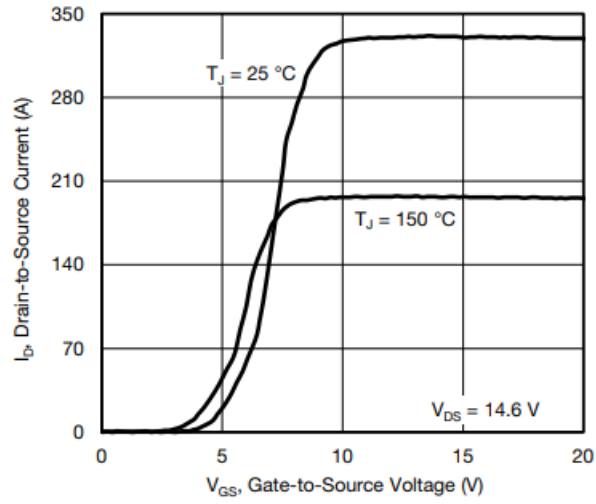


Fig. 3 - Typical Transfer Characteristics

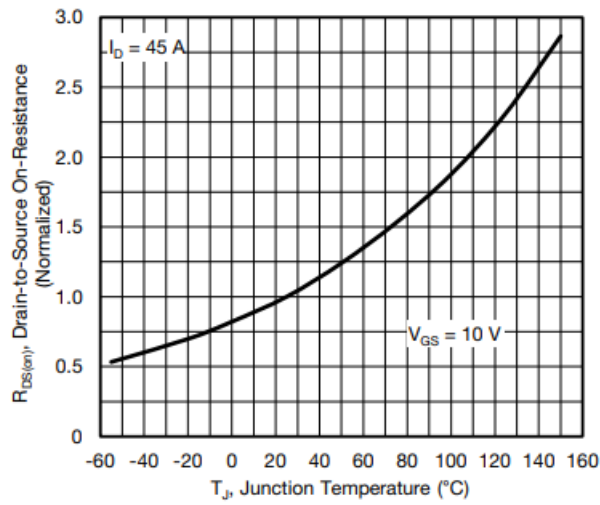


Fig. 4 - Normalized On-Resistance vs. Temperature

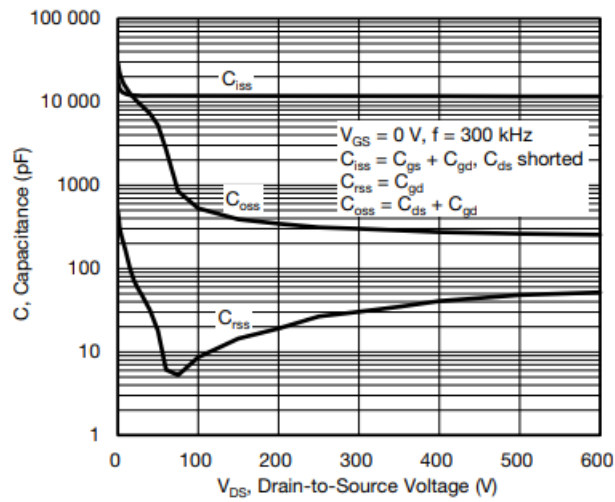


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

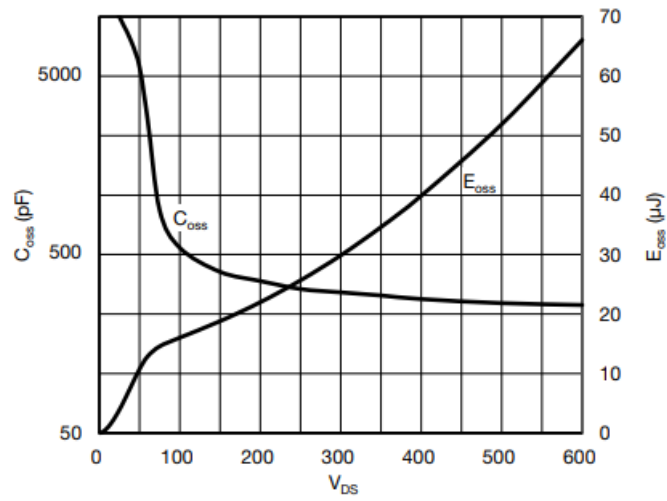


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

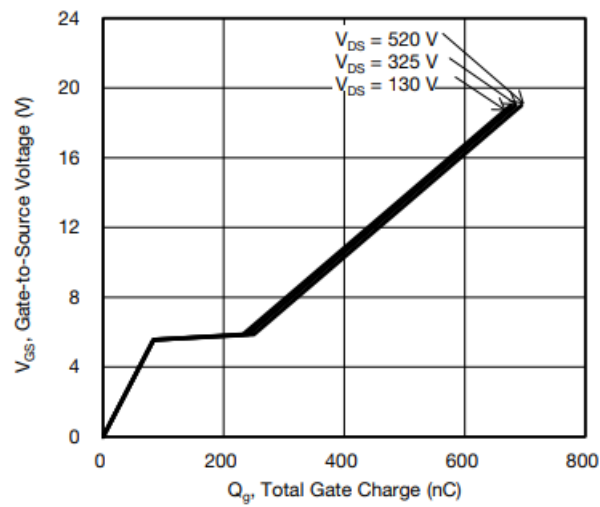


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

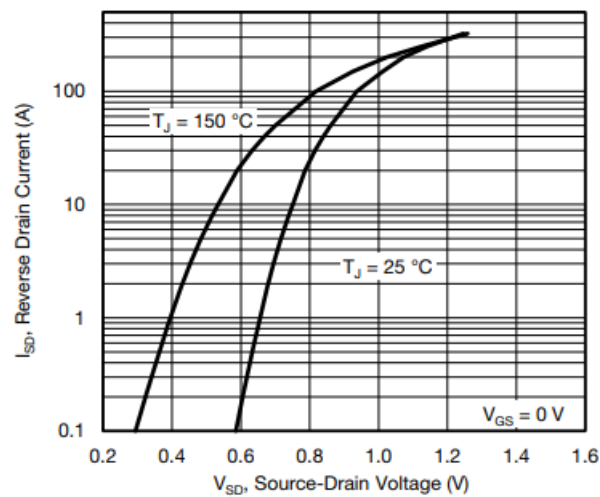


Fig. 8 - Typical Source-Drain Diode Forward Voltage

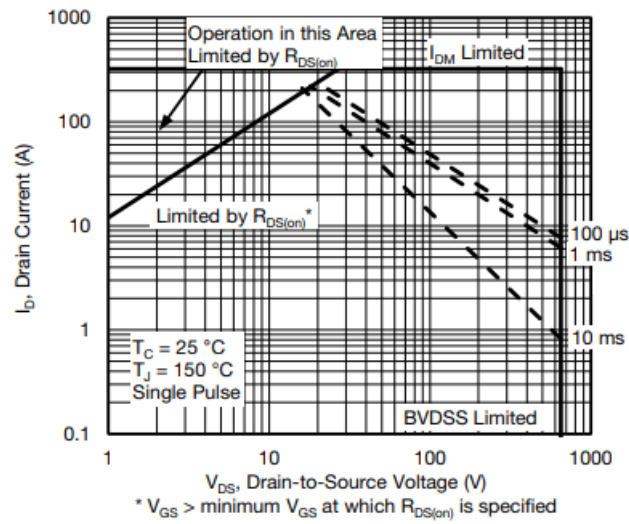


Fig. 9 - Maximum Safe Operating Area

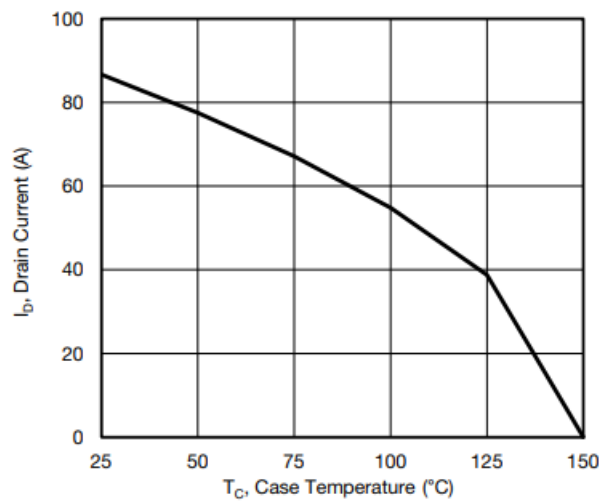


Fig. 10 - Maximum Drain Current vs. Case Temperature

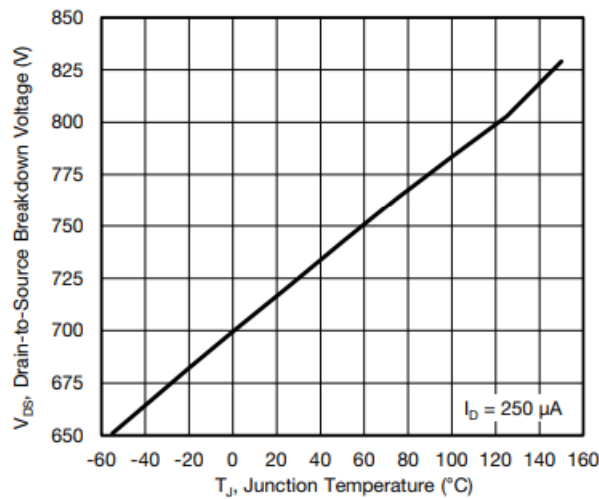


Fig. 11 - Temperature vs. Drain-to-Source Voltage

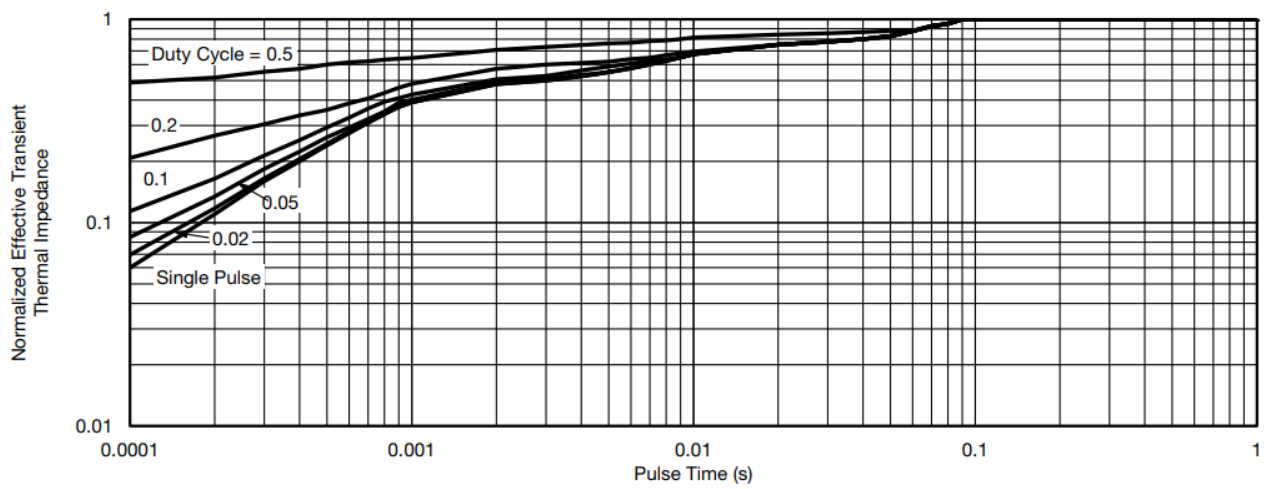


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

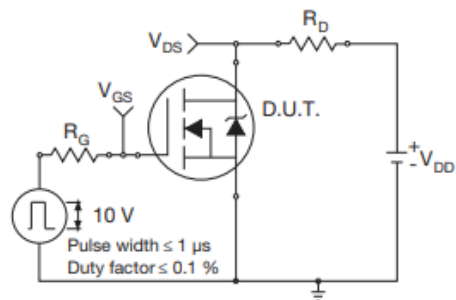


Fig. 13 - Switching Time Test Circuit

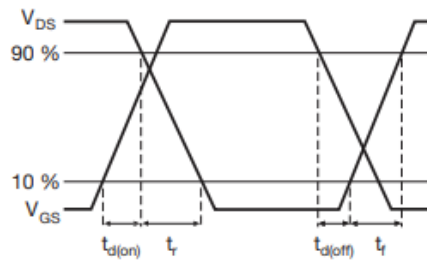


Fig. 14 - Switching Time Waveforms

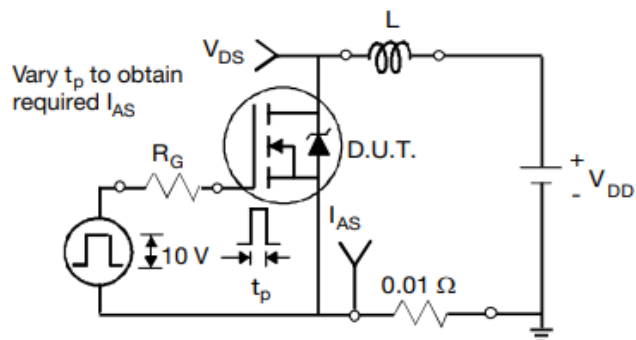


Fig. 15 - Unclamped Inductive Test Circuit

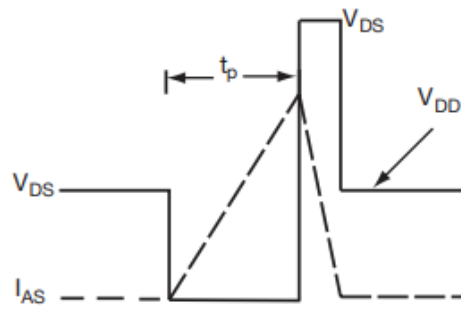


Fig. 16 - Unclamped Inductive Waveforms

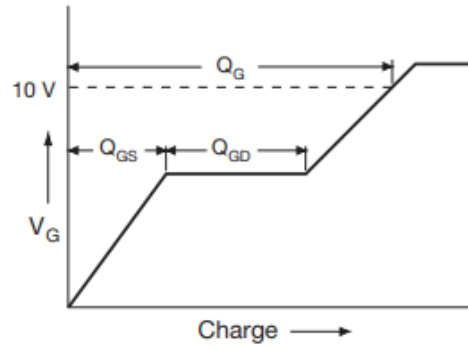


Fig. 17 - Basic Gate Charge Waveform

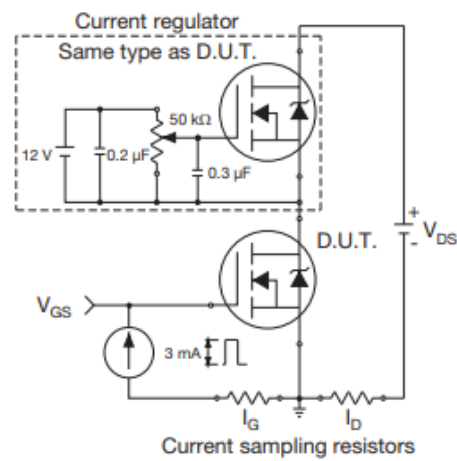
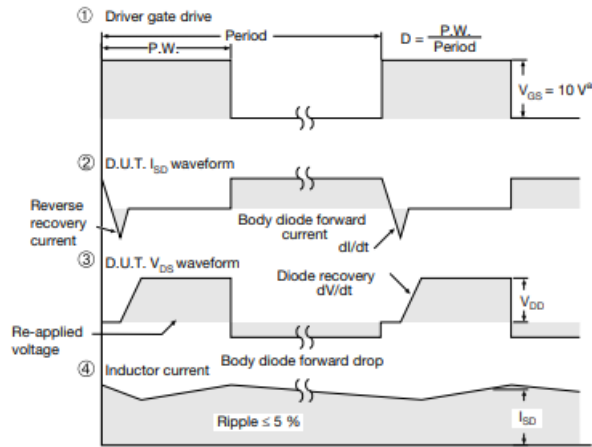
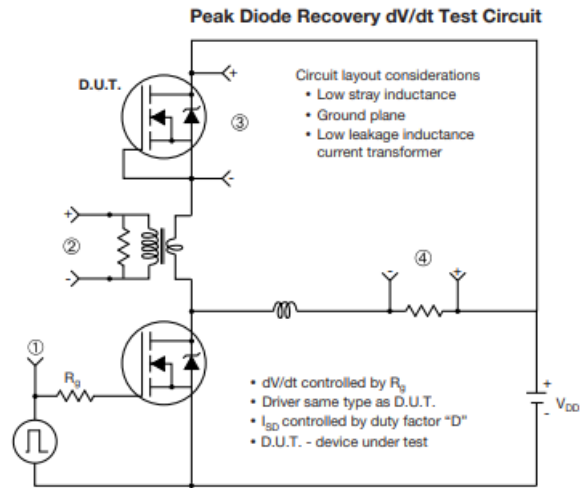


Fig. 18 - Gate Charge Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

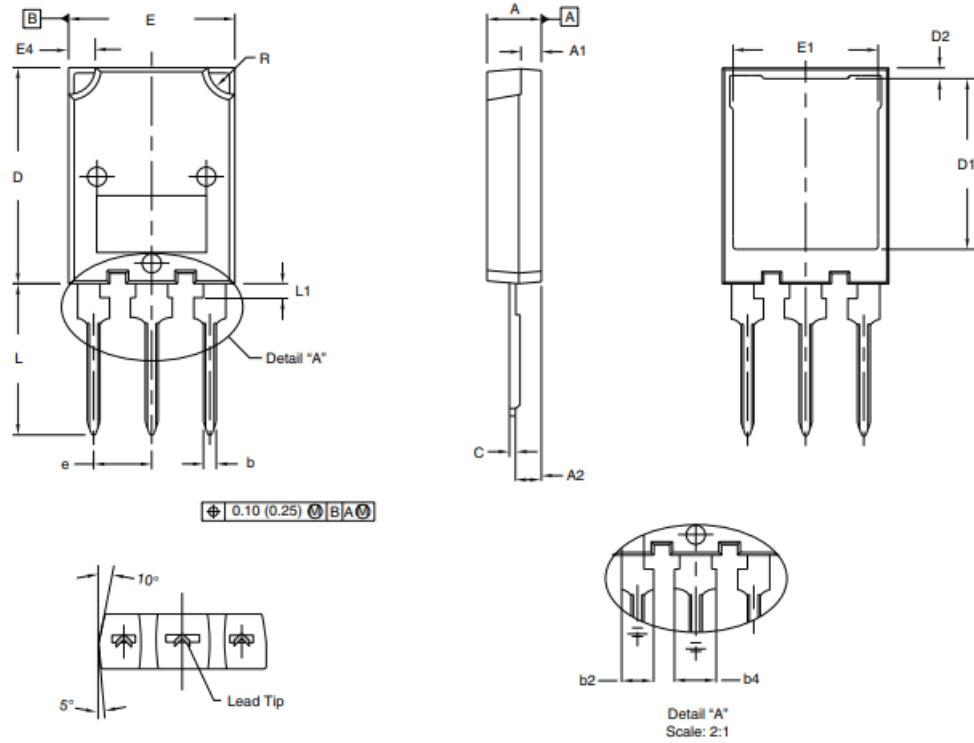
Fig. 19 - For N-Channel

TO-274AA (High Voltage)

VERSION 1: FACILITY CODE = Y

TO-274AA (High Voltage)

VERSION 1: FACILITY CODE = Y



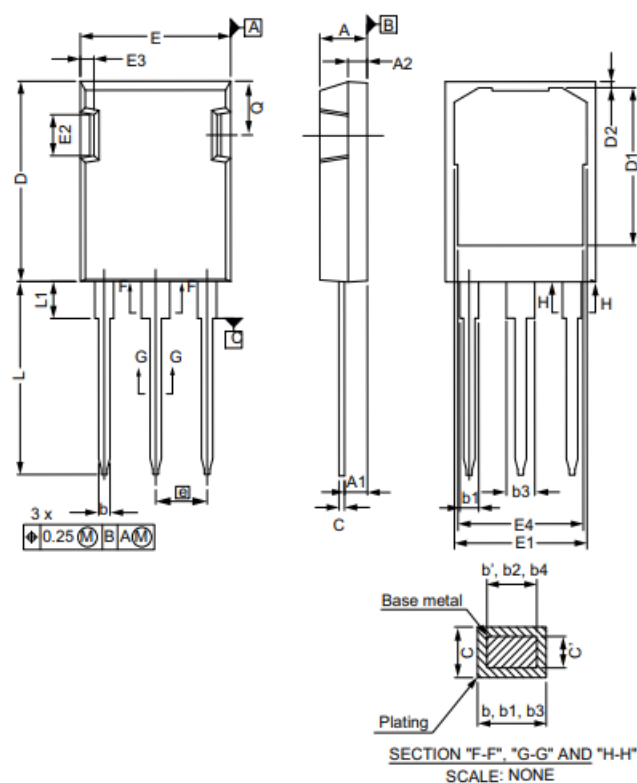
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c (1)	0.38	0.89	0.015	0.035
D	19.80	20.80	0.780	0.819

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA
 - (1) Dimension measured at tip of lead

VERSION 2: FACILITY CODE = N



MILLIMETERS			MILLIMETERS		
DIM.	MIN.	MAX.	DIM.	MIN.	MAX.
A	4.83	5.21	D1	16.25	17.65
A1	2.29	2.54	D2	0.50	0.80
A2	1.91	2.16	E	15.75	16.13
b'	1.07	1.28	E1	13.10	14.15
b	1.07	1.33	E2	3.68	5.10
b1	1.91	2.41	E3	1.00	1.90
b2	1.91	2.16	E4	12.38	13.43
b3	2.87	3.38	e	5.44 BSC	
b4	2.87	3.13	N	3	
c'	0.55	0.65	L	19.81	20.32
c	0.55	0.68	L1	3.70	4.00
D	20.80	21.10	Q	5.49	6.00
ECN: E20-0538-Rev. C, 19-Oct-2020 DWG: 5975					

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Outline conforms to JEDEC® outline to TO-274AD
- Dimensions are measured in mm, angles are in degree
- Metal surfaces are tin plated, except area of cut

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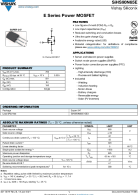
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Documents / Resources

	<p>VISHAY SiHS90N65E Power MOSFET [pdf] Instruction Manual SiHS90N65E Power MOSFET, SiHS90N65E, Power MOSFET, MOSFET</p>
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References

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