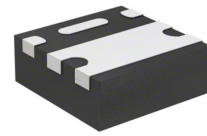




SIA416DJ Siliconix Discrete  
Semiconductor



# VISHAY SIA416DJ Siliconix Discrete Semiconductor Owner's Manual

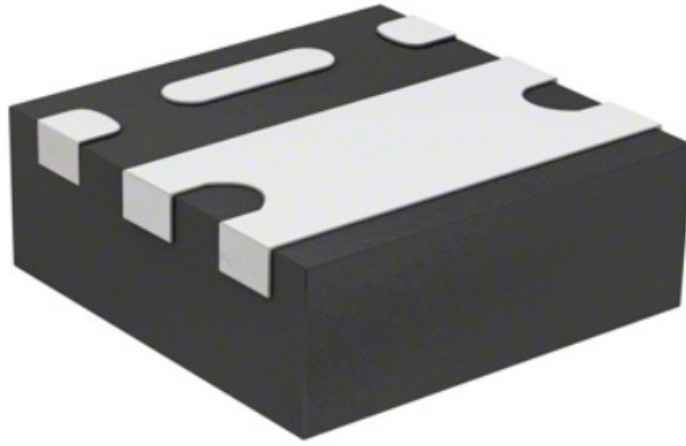
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**VISHAY SIA416DJ Siliconix Discrete Semiconductor**



### Specifications:

- Manufacturer: Vishay Siliconix
- Product Name: SiA416DJ
- Channel Type: N-Channel
- Maximum Drain-Source Voltage (VDS): 100V
- Maximum On-State Resistance (RDS(on)): 0.083 ohms at VGS = 10V, 0.130 ohms at VGS = 4.5V
- Continuous Drain Current (ID): 11.3A
- Total Gate Charge (Qg): 3.5nC
- Package Type: PowerPAK SC-70-6L-Single
- Lead-free and Halogen-free

### Product Usage Instructions

#### Features and Parameters:

- Maximum Drain-Source Voltage (VDS): 100V
- Continuous Drain Current (ID): 11.3A
- Total Gate Charge (Qg): 3.5nC
- Maximum Power Dissipation: 12W
- Operating Temperature Range: -55°C to 150°C
- Soldering Peak Temperature: 260°C

#### Static Parameters:

- Drain-Source Breakdown Voltage: 100V
- Gate-Source Threshold Voltage: 3V
- Zero Gate Voltage Drain Current: 10nA
- On-State Drain Current: 9A
- Drain-Source On-State Resistance: 0.083 ohms at VGS = 10V, 0.130 ohms at VGS = 4.5V

#### Dynamic Parameters:

- Total Gate Charge: 3.5nC

- Input Capacitance: 295pF
- Output Capacitance: 92pF
- Reverse Transfer Capacitance: 16pF
- Turn-On Delay Time: 25ns
- Rise Time: 50ns
- Turn-Off Delay Time: 100ns
- Fall Time: 200ns

**Frequently Asked Questions (FAQ):**

**1. Q: What is the maximum operating temperature range for the SiA416DJ MOSFET?**

A: The MOSFET can operate within a temperature range of -55°C to 150°C.

**2. Q: Does the SiA416DJ MOSFET come with lead and halogen-free options?**

A: Yes, the ordering information includes lead (Pb)-free and Halogen-free options.

**3. Q: What is the maximum drain-source voltage supported by the SiA416DJ MOSFET?**

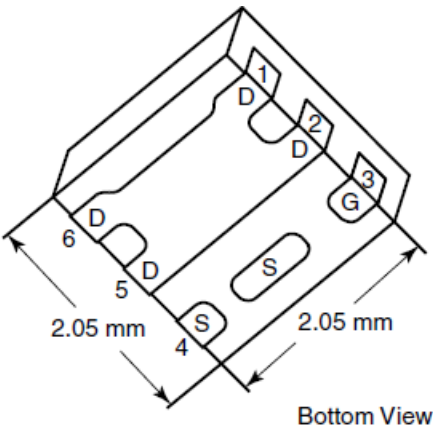
A: The MOSFET supports a maximum drain-source voltage of 100V.

**4. Q: What is the total gate charge for the SiA416DJ MOSFET?**

A: The total gate charge is specified to be 3.5nC.

PRODUCT SUMMARY			
VDS (V)	RDS(on) (W) Max.	ID (A) <sup>a</sup>	Qg (Typ.)
100	0.083 at VGS = 10 V	11.3	3.5 nC
	0.130 at VGS = 4.5 V	9	

**PowerPAK SC-70-6L-Single**



**Ordering Information:**  
 SiA416DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

**FEATURES**

- TrenchFET® Power MOSFET
- 100 % Rg and UIS Tested

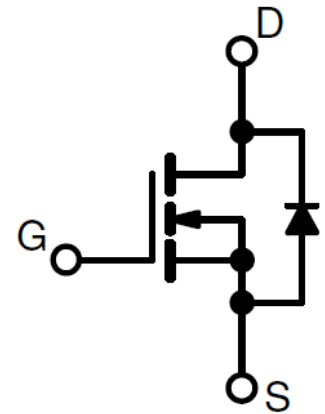
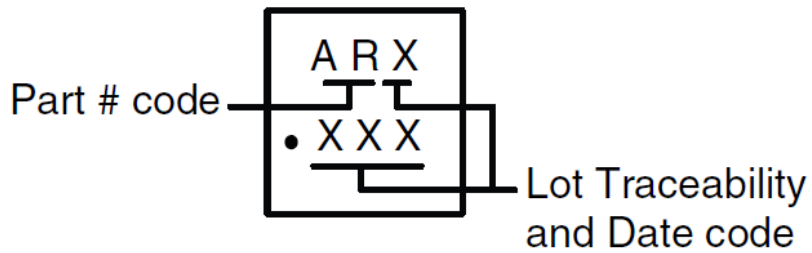
- **Material categorization:**

For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

## APPLICATIONS

- DC/DC Converters
- Full-Bridge Converters
- For Power Bricks and POL Power

### Marking Code



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		VDS	100	V
Gate-Source Voltage		VGS	± 20	
Continuous Drain Current (TJ = 150 °C)	TC = 25 °C	ID	11.3	A
	TC = 70 °C		9	
	TA = 25 °C		4.8b, c	
	TA = 70 °C		3.9b, c	
Pulsed Drain Current (t = 300 µs)		IDM	15	
Continuous Source-Drain Diode Current	TC = 25 °C	IS	12	
	TA = 25 °C		2.9b, c	
Single Pulse Avalanche Current	L = 0.1 mH	IAS	3	mJ
Single Pulse Avalanche Energy		EAS	0.45	
Maximum Power Dissipation	TC = 25 °C	PD	19	W
	TC = 70 °C		12	
	TA = 25 °C		3.5b, c	
	TA = 70 °C		2.2b, c	
Operating Junction and Storage Temperature Range		TJ, Tstg	– 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	RthJA	28	36	°C/W
Maximum Junction-to-Case (Drain)	Steady State	RthJC	5.3	6.5	

#### Notes:

- Based on TC = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
V <sub>DS</sub> Temperature Coefficient	DV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		54		mV/°C
V <sub>GS</sub> (th) Temperature Coefficient	DV <sub>GS</sub> (t <sub>h</sub> )/T <sub>J</sub>			− 4.4		
Gate-Source Threshold Voltage	V <sub>GS</sub> (th)	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.6		3	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D</sub> (on)	V <sub>DS</sub> <sup>3</sup> 5 V, V <sub>GS</sub> = 10 V	10			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS</sub> (on)	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.2 A		0.068	0.083	W
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.6 A		0.092	0.130	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.2 A		8		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 M Hz		295		pF
Output Capacitance	C <sub>oss</sub>			92		
Reverse Transfer Capacitance	C <sub>rss</sub>			16		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.8 A		6.5	10	nC
				3.5	5.3	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.8 A		1.2		
Gate-Drain Charge	Q <sub>gd</sub>			1.9		
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		7.6		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.4	1.8	3.6	W
Turn-On Delay Time	t <sub>d</sub> (on)	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 12.8 W ID @ 3.9 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 W		5	10	ns
Rise Time	t <sub>r</sub>			13	25	
Turn-Off Delay Time	t <sub>d</sub> (off)			10	20	
Fall Time	t <sub>f</sub>			10	20	
Turn-On Delay Time	t <sub>d</sub> (on)	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 12.8 W ID @ 3.9 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub>		25	50	
Rise Time	t <sub>r</sub>			100	200	

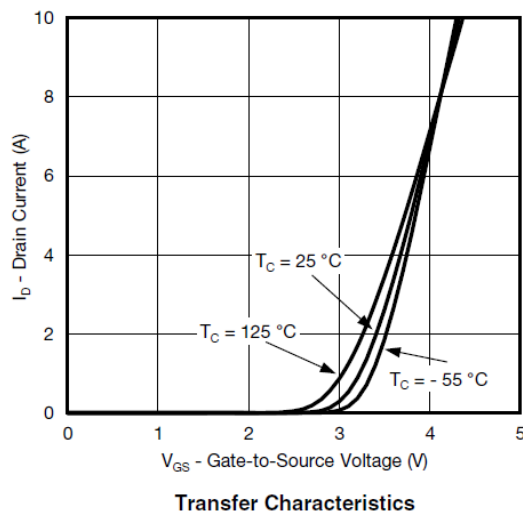
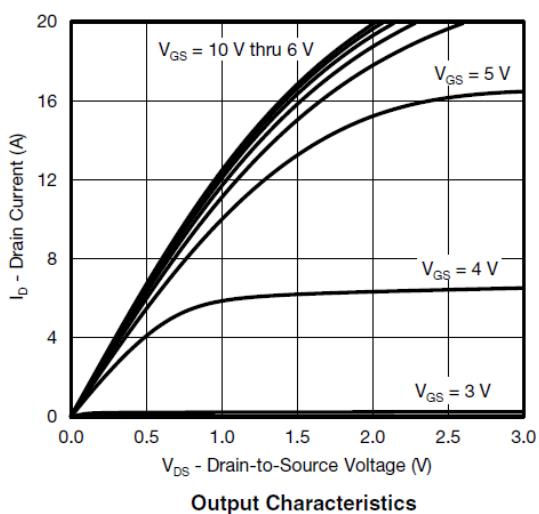
Turn-Off Delay Time	td(off)	= 1 W		15	30	
Fall Time	tf			25	50	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	IS	TC = 25 °C			12	A
Pulse Diode Forward Current <sup>a</sup>	ISM				15	
Body Diode Voltage	VSD	IS = 3.9 A		0.85	1.2	V
Body Diode Reverse Recovery Time	trr	IF = 3.9 A, dI/dt = 100 A/μs, TJ = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Qrr			30	60	nC
Reverse Recovery Fall Time	ta			20		ns
Reverse Recovery Rise Time	tb			10		

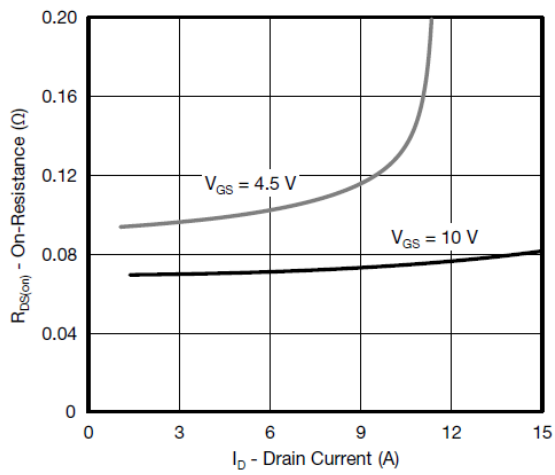
#### Notes:

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- Guaranteed by design, not subject to production testing.

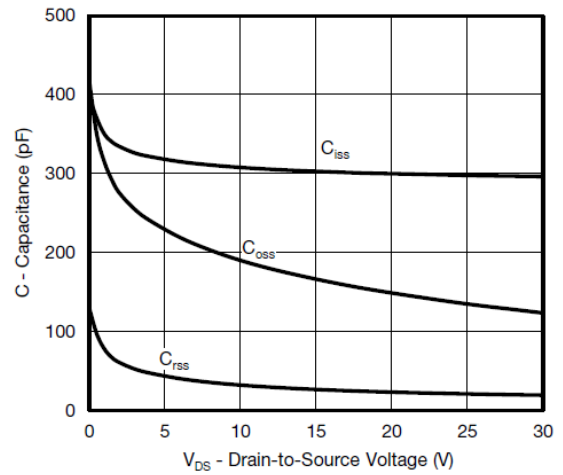
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

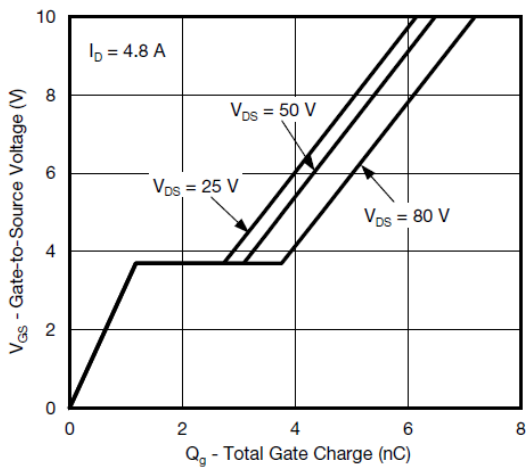




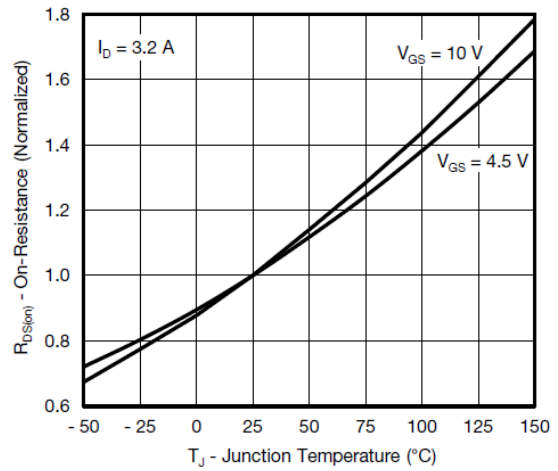
On-Resistance vs. Drain Current and Gate Voltage



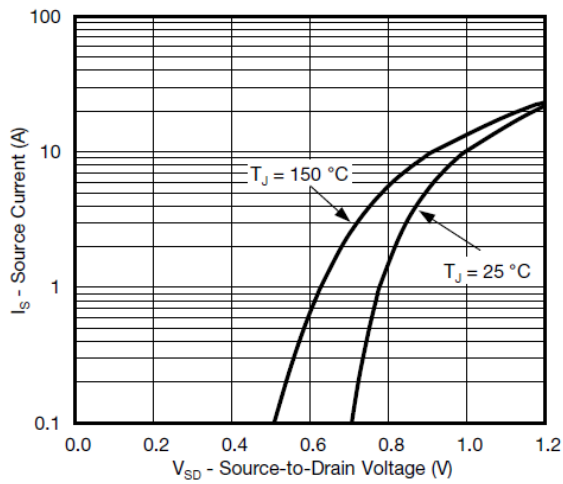
Capacitance



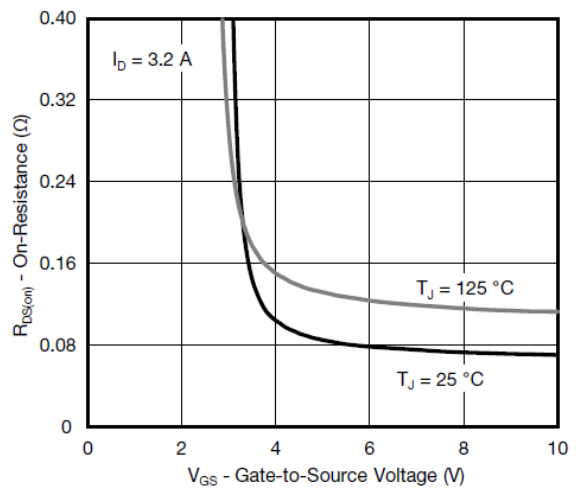
Gate Charge



On-Resistance vs. Junction Temperature

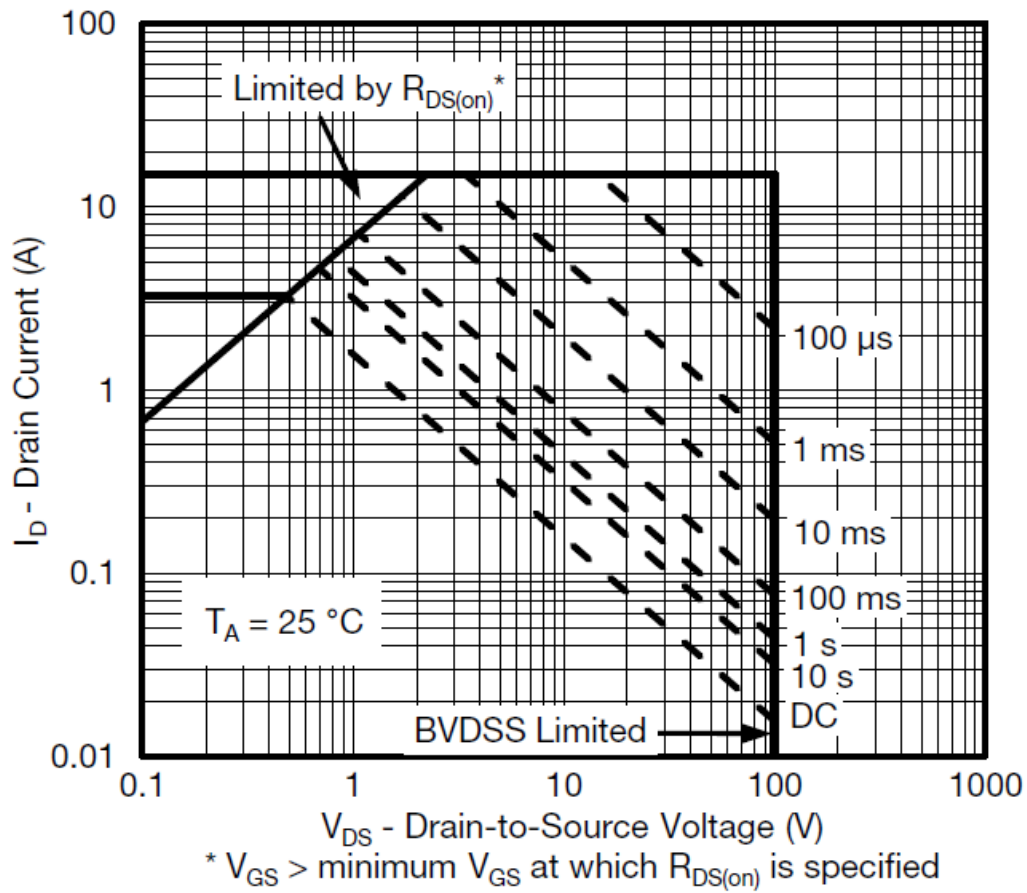
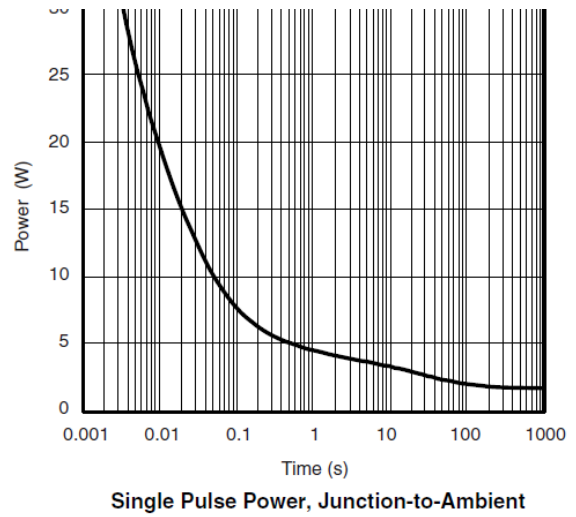
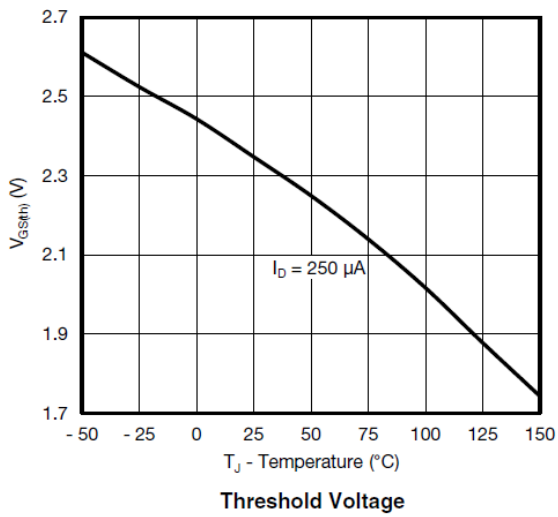


Source-Drain Diode Forward Voltage

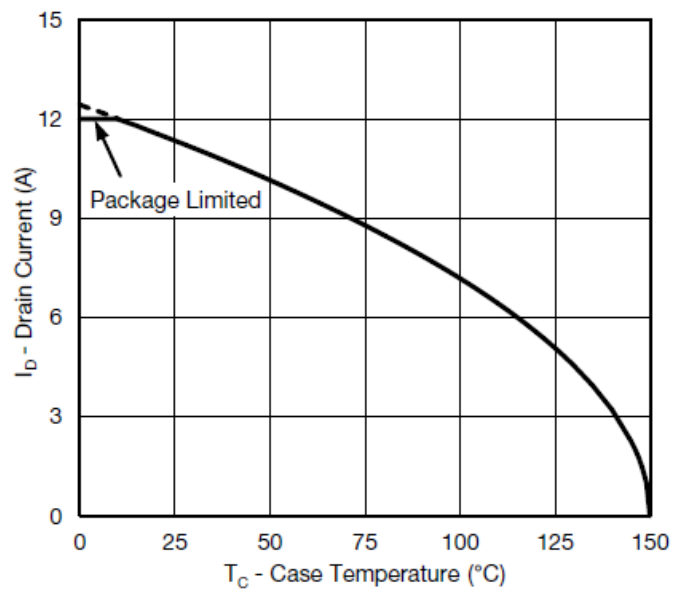


On-Resistance vs. Gate-to-Source Voltage

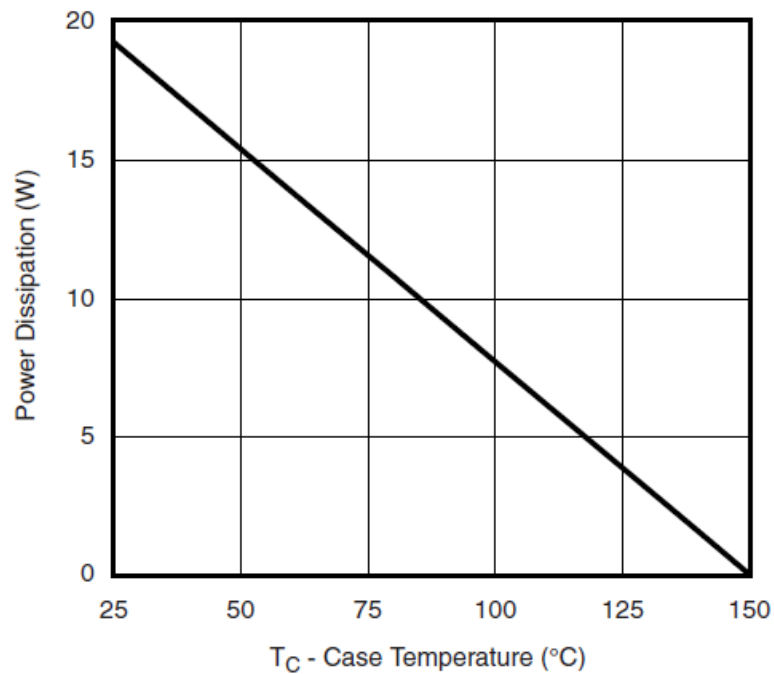




Safe Operating Area, Junction-to-Ambient  
TYPICAL CHARACTERISTICS (25  $^{\circ}C$ , unless otherwise noted)



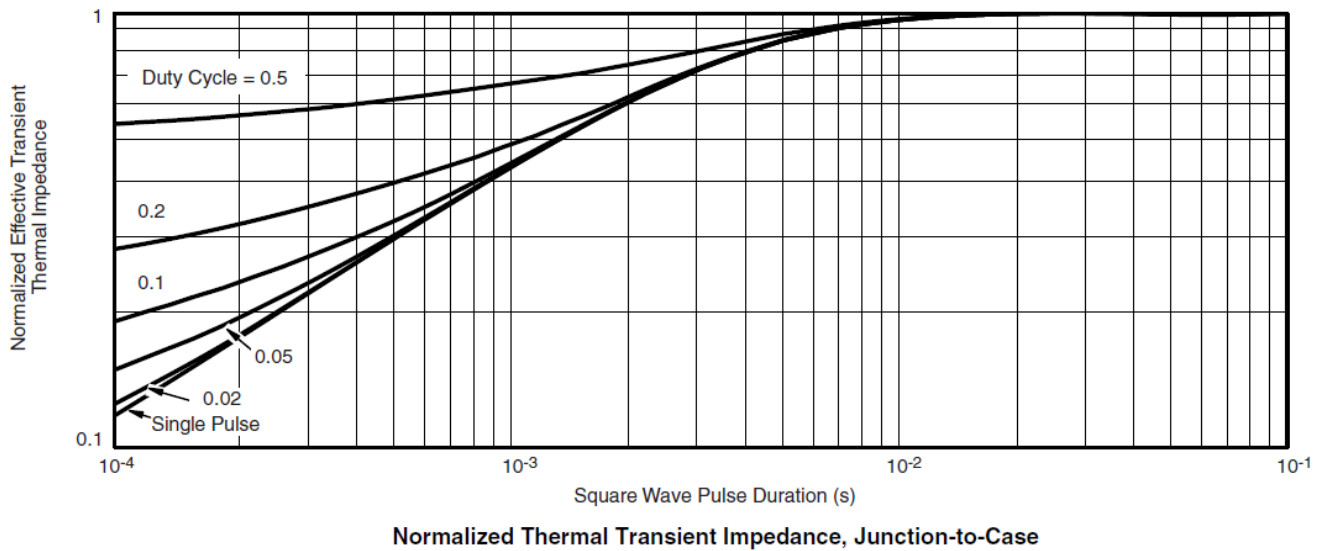
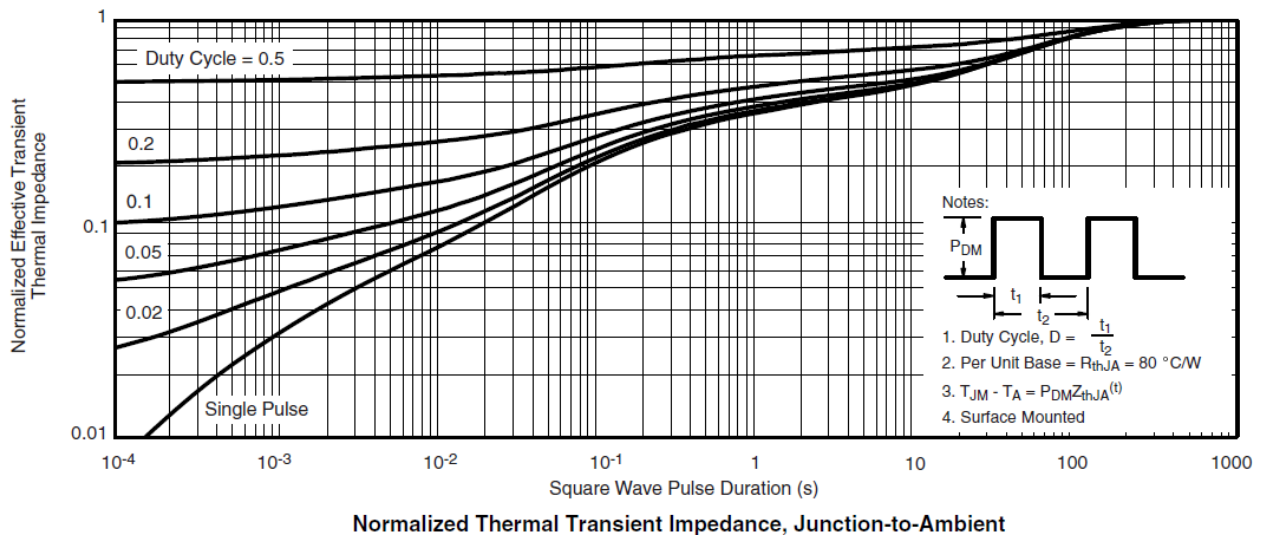
**Current Derating\***



**Power, Junction-to-Case**

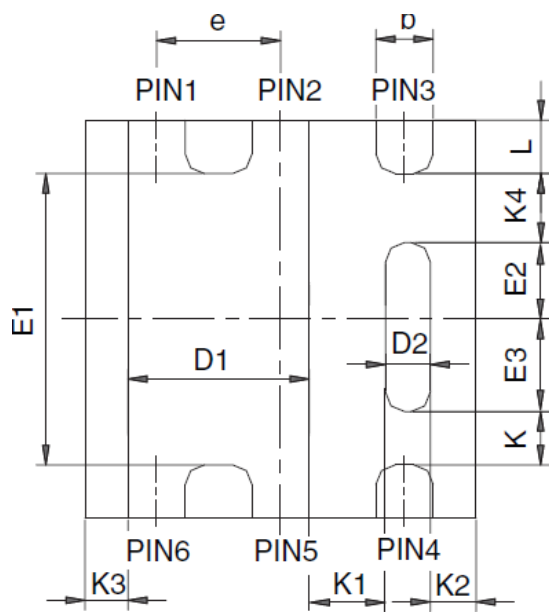
\* The power dissipation PD is based on  $T_J(\text{max.}) = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**

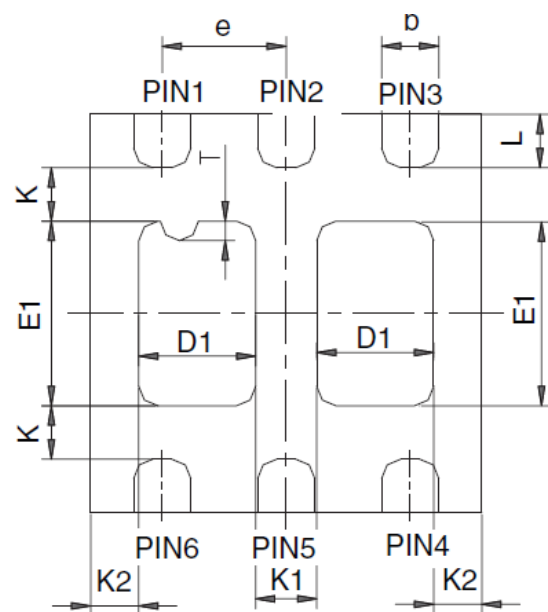


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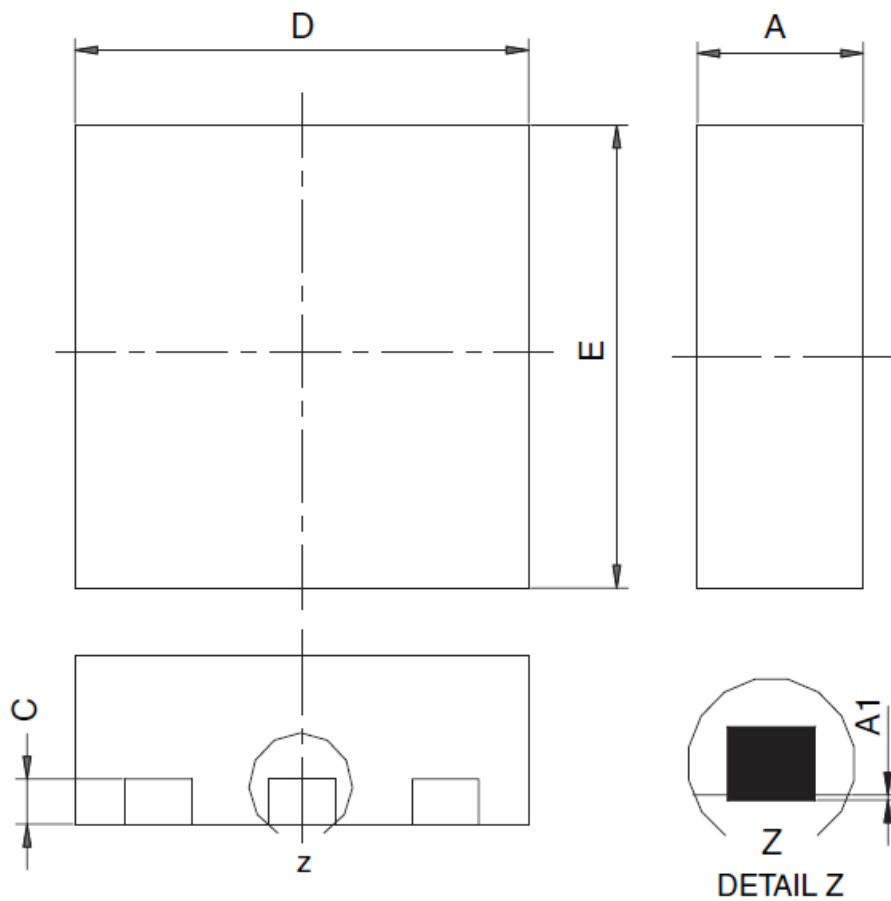
**PowerPAK® SC70-6L**



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL

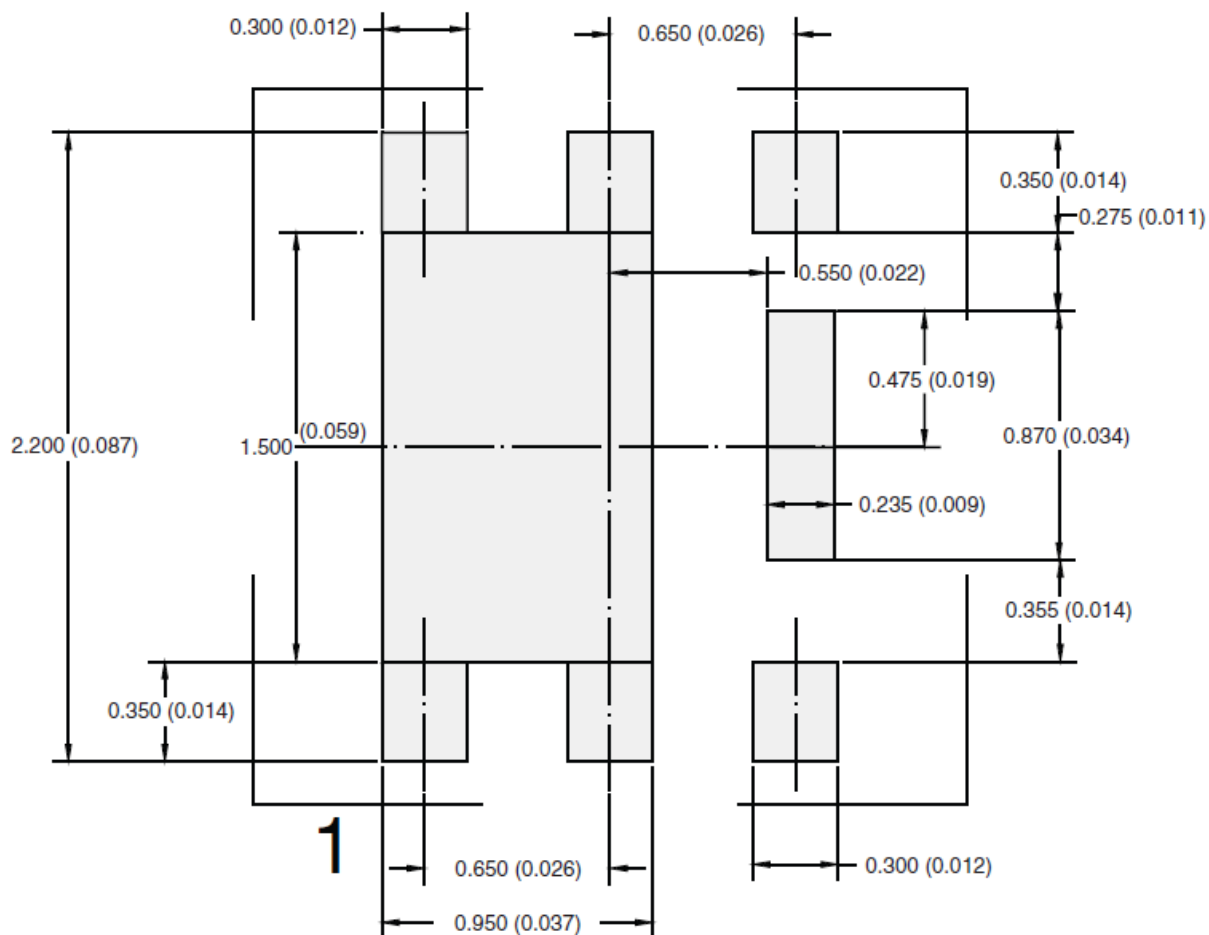


#### Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
<b>A1</b>	0	—	0.05	0	—	0.002	0	—	0.05	0	—	0.002
<b>b</b>	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
<b>C</b>	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
<b>D</b>	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
<b>D1</b>	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
<b>D2</b>	0.135	0.235	0.335	0.005	0.009	0.013						
<b>E</b>	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
<b>E1</b>	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
<b>E2</b>	0.345	0.395	0.445	0.014	0.016	0.018						
<b>E3</b>	0.425	0.475	0.525	0.017	0.019	0.021						
<b>e</b>	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
<b>K</b>	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
<b>K1</b>	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
<b>K2</b>	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
<b>K3</b>	0.225 TYP			0.009 TYP								
<b>K4</b>	0.355 TYP			0.014 TYP								
<b>L</b>	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
<b>T</b>							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C-07431 – Rev. C, 06-Aug-07 DWG: 5934												

## RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

## Disclaimer

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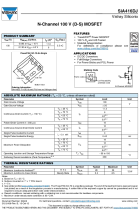
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**Documents / Resources**



[VISHAY SIA416DJ Siliconix Discrete Semiconductor](#) [pdf] Owner's Manual  
SIA416DJ Siliconix Discrete Semiconductor, SIA416DJ, Siliconix Discrete Semiconductor, Discrete Semiconductor, Semiconductor

**References**

- [Vishay Intertechnology: Passives & Discrete Semiconductors](#)
- [User Manual](#)

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