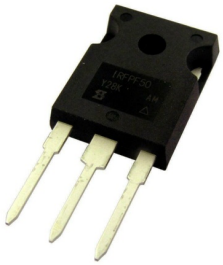


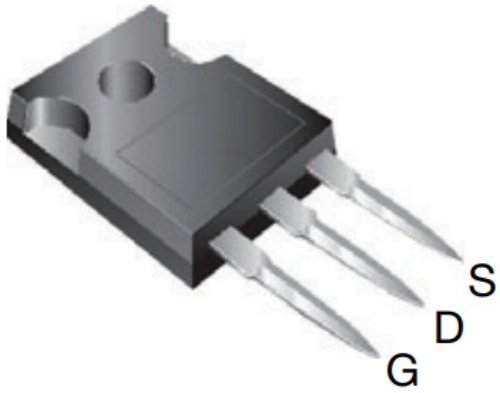
VISHAY IRFPF50 Siliconix Power MOSFET Instruction Manual

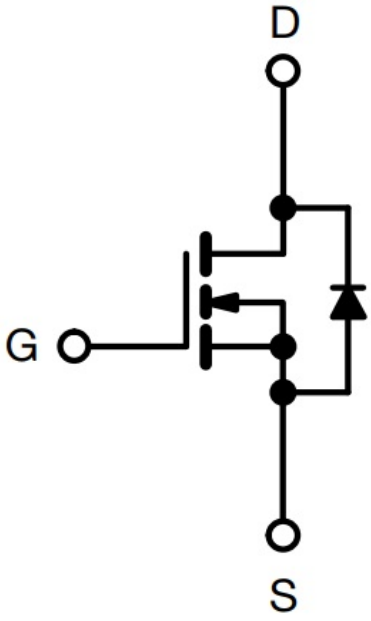
IRFPF50
Vishay Siliconix
www.vishay.com

Contents

Power MOSFET

TO-247AC





N-Channel MOSFET

PRODUCT SUMMARY		
VDS On	900	
RDS(on) (1-1)	Vas = 10 V	2.
Qg max.) (nC)	200	
Qgs (nC)	24	
Qgd (nC)	110	
Configuration	Single	

FEATURES

RoHS*
Available

- Dynamic dV/dt rated
- Repetitive avalanche rated
- Isolated central mounting hole
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant.
Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFPF50PbF

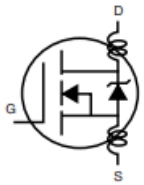
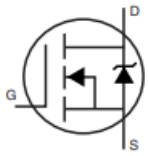
ABSOLUTE MAXIMUM RATINGS (Tc = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			VDS	900	V
Gate-source voltage			Vas	± 20	
Continuous drain current	V35 at 10 V	Tc = 25 ° C	ID	7.	A
		c = T 100 °C		4.	
Pulsed drain current a			‘Dm	27	
Linear derating factor				2.	Wit
Single pulse avalanche energy b			EAS	880	mJ
Repetitive avalanche current a			IAR	7.	A
Repetitive avalanche energy a			EAR	19	mJ
Maximum power dissipation	Tc = 25 °C		PD	190	W
Peak diode recovery dV/dt c			dV/dt	2.	V/ns
Operating junction and storage temperature range			Tj, Tstg	-55 to +150	°C
Soldering recommendations (peak te mperature)	for 10 s			300 d	
Mounting torque	6-32 or M3 screw			10	lbf .in
				1.	N .m

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. VDD = 50 V, starting TJ = 25 °C, L = 37 mH, Rg = 25 Ω, IAS = 6.7 A (see fig. 12)
c. ISD ≤ 6.7 A, dI/dt ≤ 130 A/µs, VDD ≤ 600, TJ ≤ 150 °C
d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	RthJA		40	°C/W
Case-to-sink, flat, greased surface	Rthcs	0.24		
Maximum junction-to-case (drain)	RthjC		0.65	

SPECIFICATIONS (Tj = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TW.	MAX.	UNIT
Static							
Drain-source breakdown voltage	VPS	VGs = 0 V, ID = 250 pA		900	–	–	V
VDs temperature coefficient	AN/Dsiii	Reference to 25 °C, lc, = 1 mA		–	1.	–	V/°C
Gate-source threshold voltage	VG5(th)	VDs = VGS, ID = 250 pA		2.0	–	4.0	V
Gate-source leakage	IGss	VGs = ± 20 V			–	± 100	nA
Zero gate voltage drain current	IDSS	VDs = 900 V, VGs = 0 V				100	pA
		Vps = 720 V, VGs = 0 V, TJ = 125 °C				500	
Drain-source on-state resistance	RDs(on)	VGs = 10 V	lo = 4.0 Ab			2.	Q
Forward transconductance	%	Vps = 100 v, lo = 4.0 Ab		5.		–	S
Dynamic							
Input capacitance	Gas	Vss = 0 V, Vps = 25 V, f = 1.0 MHz, see fig. 5		–	2900	–	pF
Output capacitance	Coss				270	–	
Reverse transfer capacitance	Gras				92	–	
Total gate charge	Qg	VGs = 10 V	lo = 6.7 A, Vps = 360 V, see fig. 6 and 13 b		–	200	nC
Gate-source charge	Ogs					24	
Gate-drain charge	Ogd					110	
Turn-on delay time	td(on)	VDD = 450 V, ID = 6.7 A , RG = 6.2 Q, RD = 67 0, see fig. 1 06			20		ns
Rise time	ti.				34	–	
Turn-off delay time	td(off)				130	–	

Fall time	tf			37	–	
Internal drain inductance	LD	Between l 6 mm (0.25′) from package and center of die contact		5.0	–	nH
Internal source inductance	Ls			13	–	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	Is	MOSFET symbol showing the integral reverse p – n junction diode		–	7.	A
Pulsed diode forward current a	ISM			–	27	
Body diode voltage	VS0	TJ = 25 °C, Is = 6.7 A, VGs = 0 Vb			2.	V
Body diode reverse recovery ti me	trr	TJ = 25 °C, IF= 6.7 A, dVdt = 10 0 A/psb		610	920	ns
Body diode reverse recovery c harge	Qrr			3.	5.	pC
Forward turn-on time	ton	Intrinsic turn-on time is negligible (turn-on is dominated by Ls an d LS				

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS

(25 °C, unless otherwise noted)

Fig. 1 – Typical Output Characteristics, TC = 25 °C

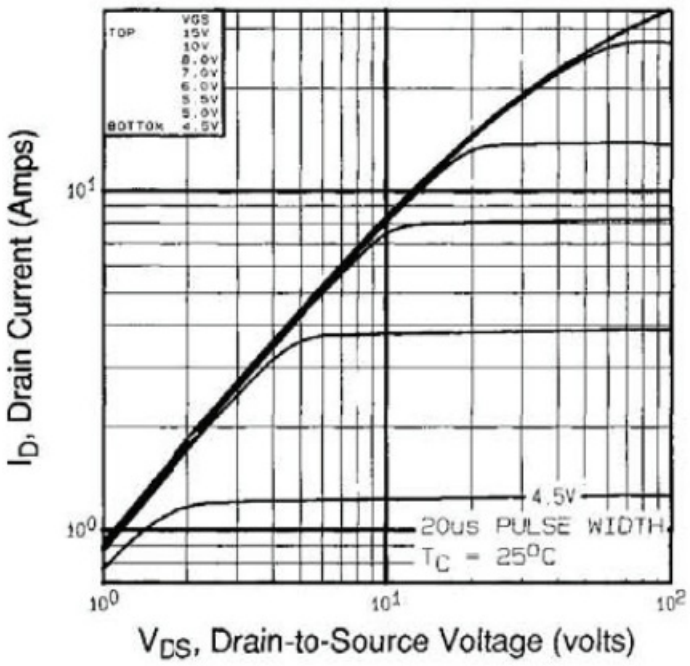


Fig. 2 – Typical Output Characteristics, TC = 150 °C

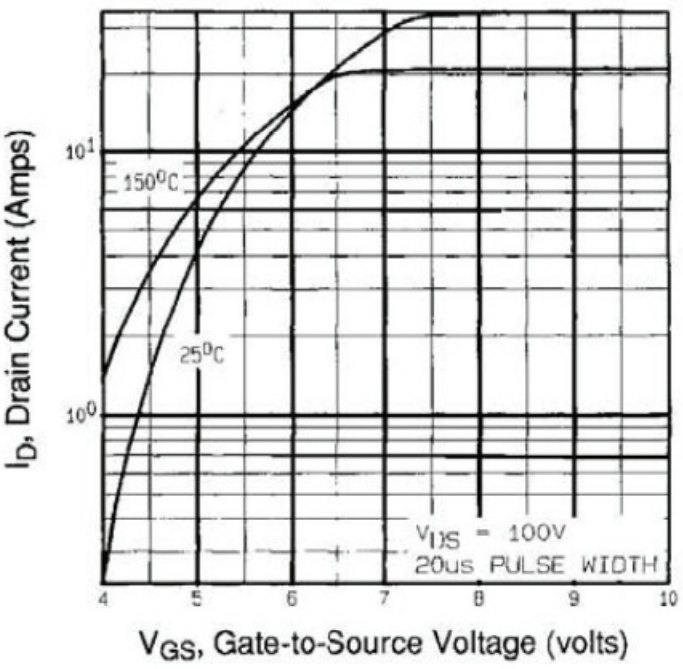


Fig. 3 – Typical Transfer Characteristics

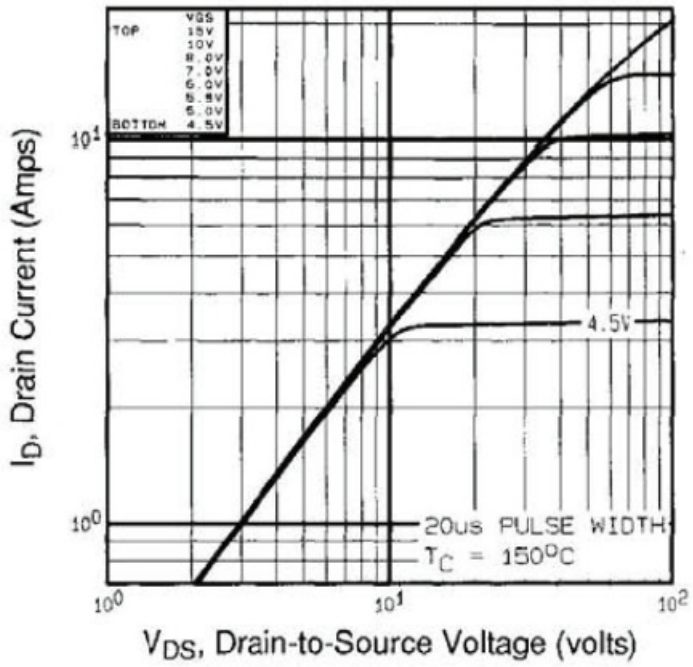


Fig. 4 – Normalized On-Resistance vs. Temperature

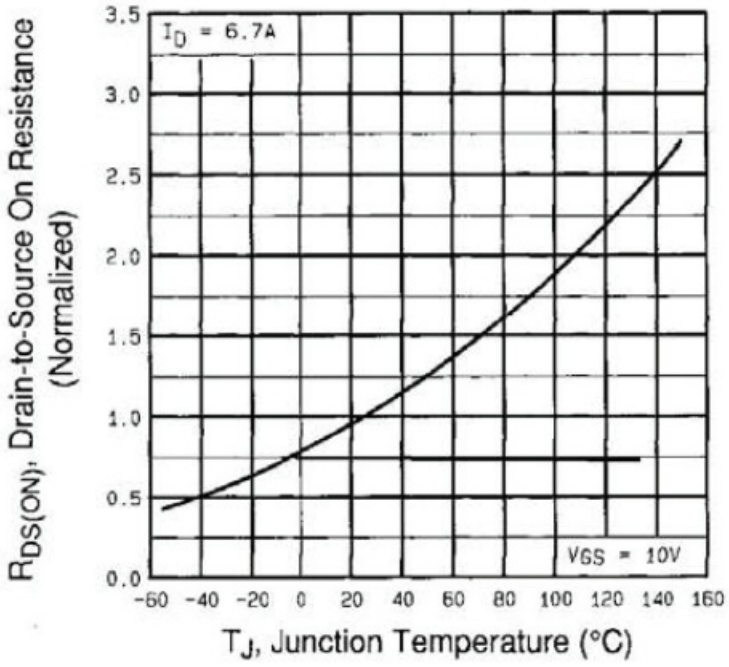


Fig. 5 – Typical Capacitance vs. Drain-to-Source Voltage

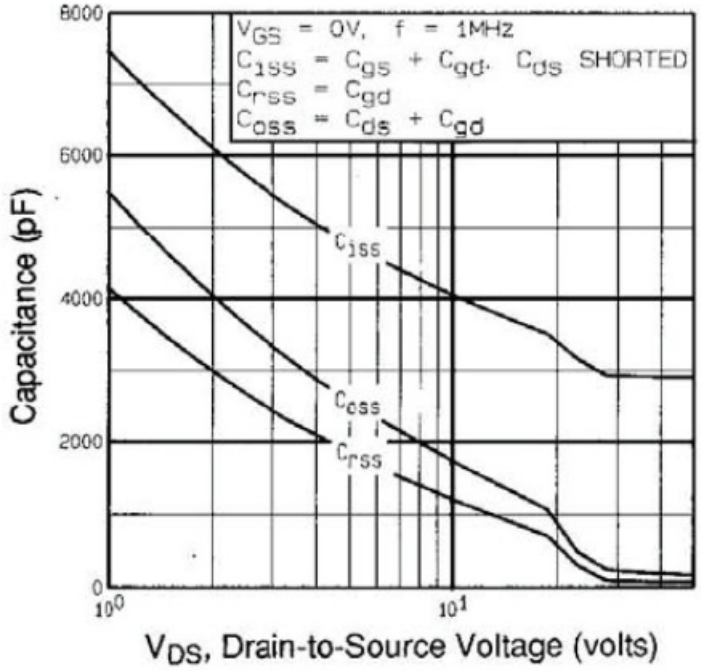


Fig. 7 – Typical Source-Drain Diode Forward Voltage

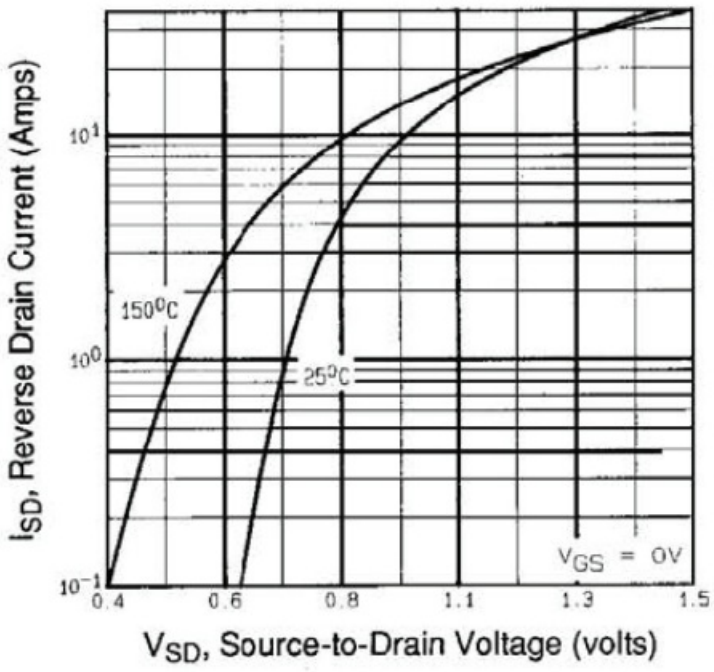


Fig. 6 – Typical Gate Charge vs. Gate-to-Source Voltage

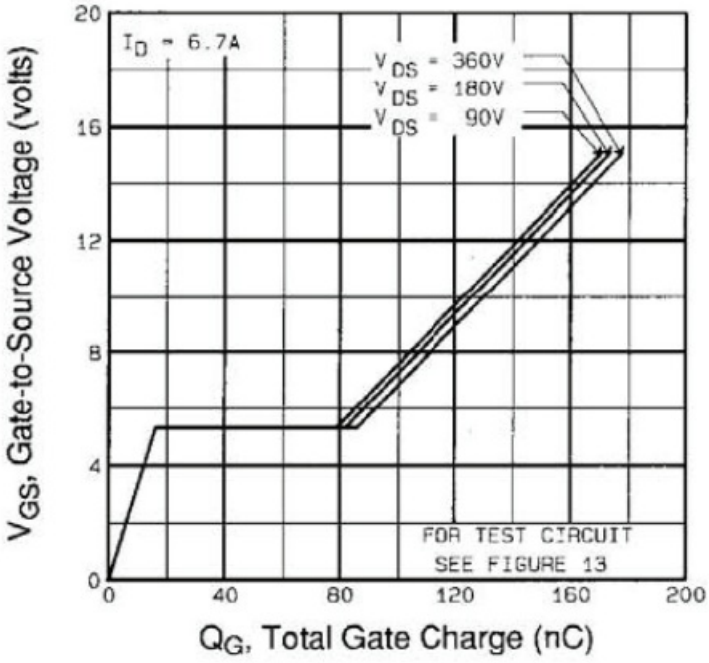


Fig. 8 – Maximum Safe Operating Area

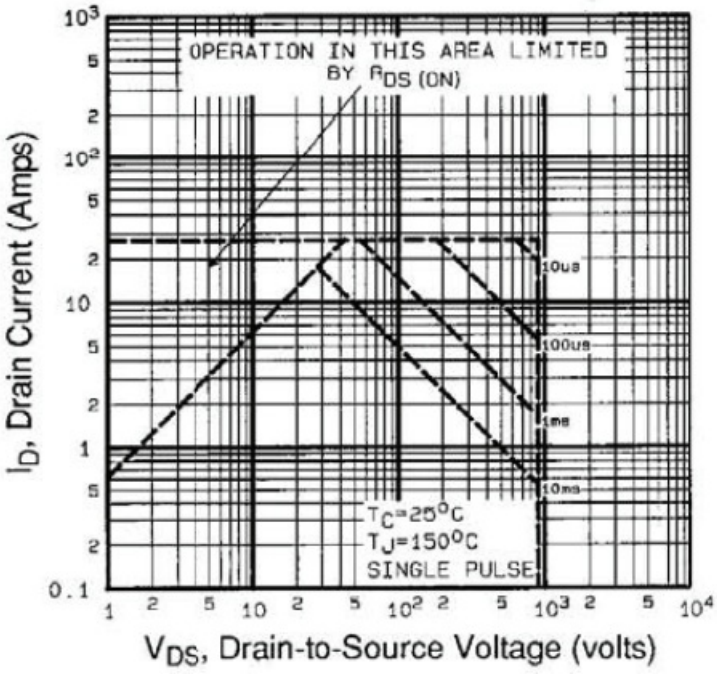


Fig. 9 – Maximum Drain Current vs. Case Temperature

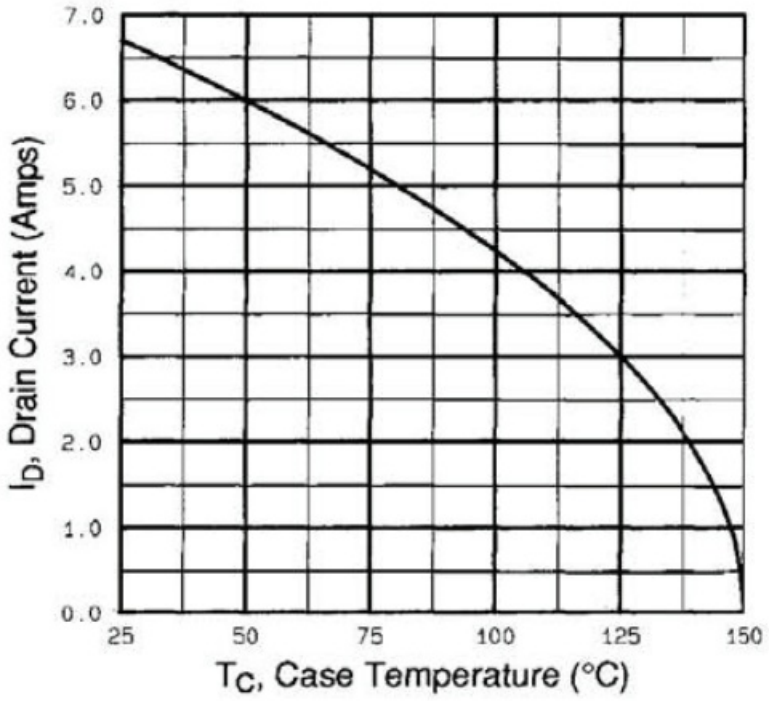


Fig. 10 – Switching Time Test Circuit

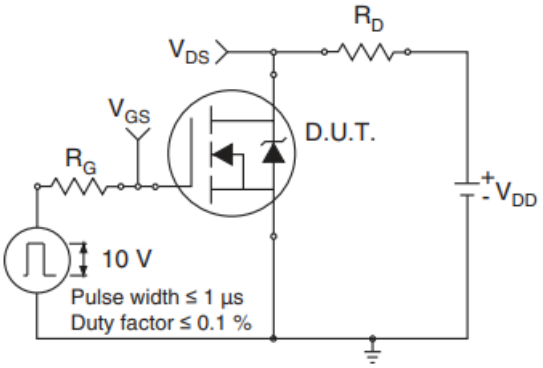


Fig. 10 – Switching Time Test Circuit

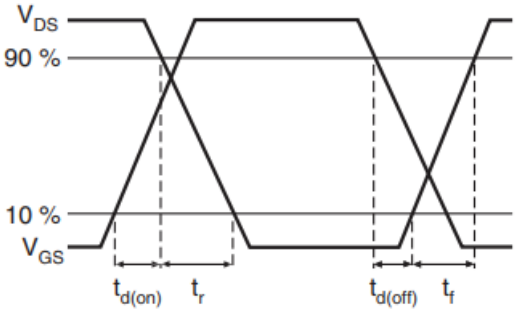


Fig. 12 – Maximum Effective Transient Thermal Impedance, Junction-to-Case

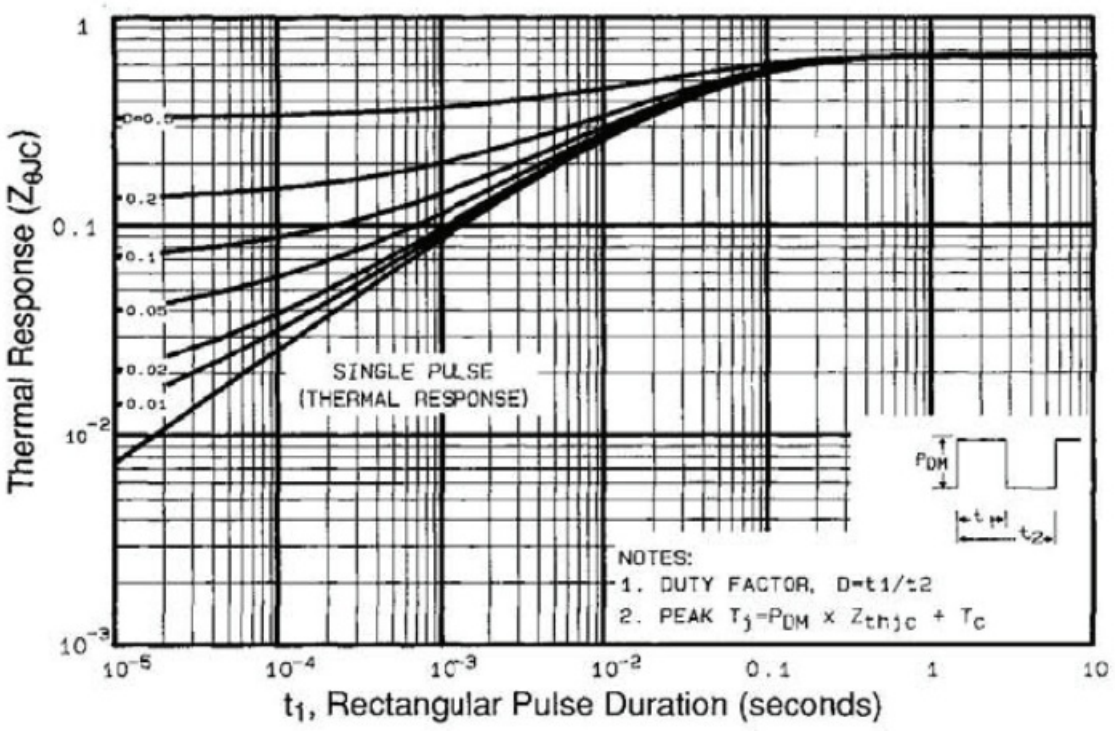


Fig. 13 – Unclamped Inductive Test Circuit

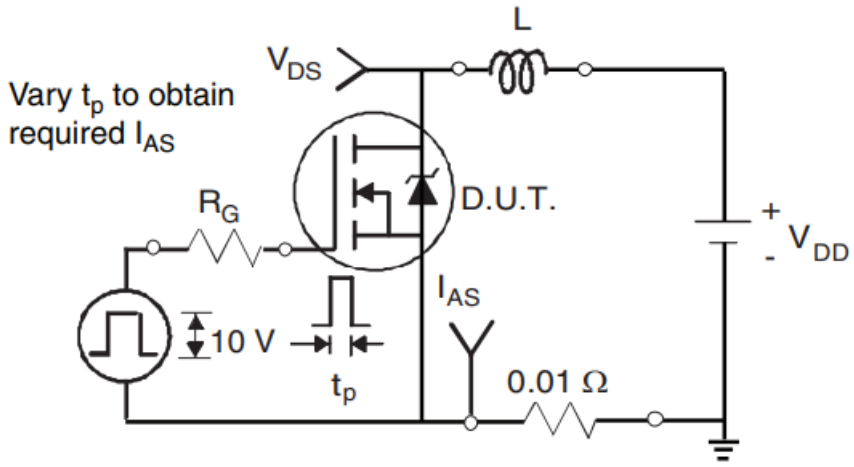


Fig. 14 – Unclamped Inductive Waveforms

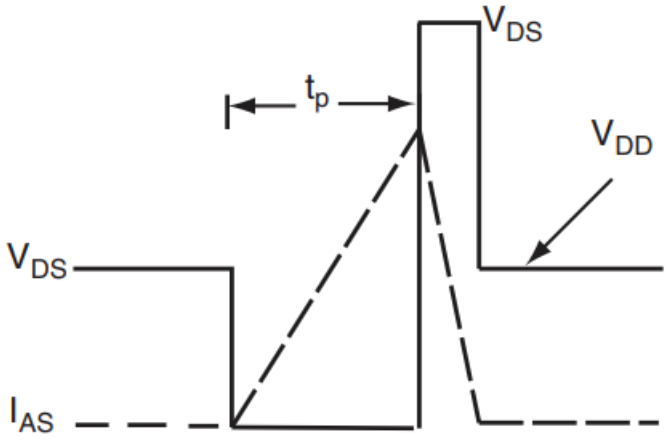


Fig. 15 – Maximum Avalanche Energy vs. Drain Current

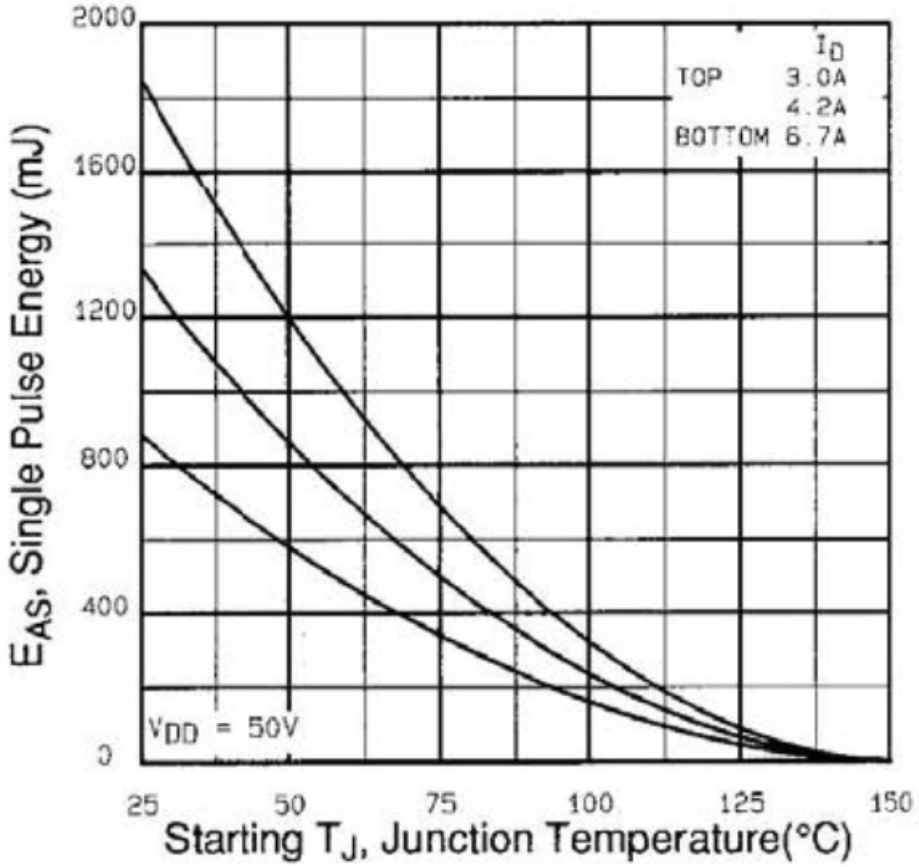


Fig. 16 – Basic Gate Charge Waveform

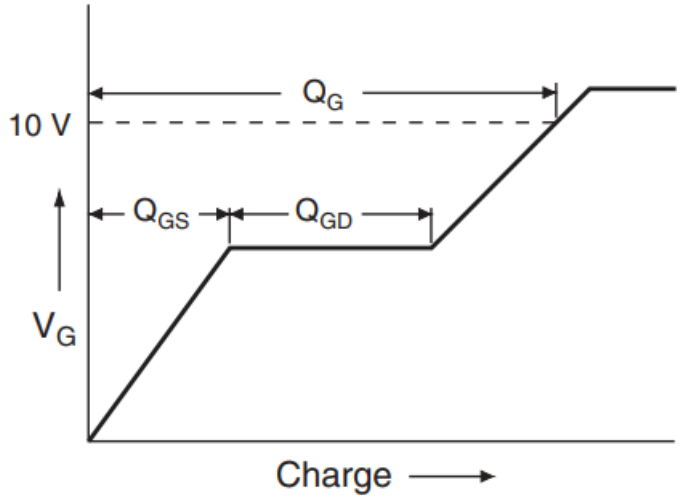
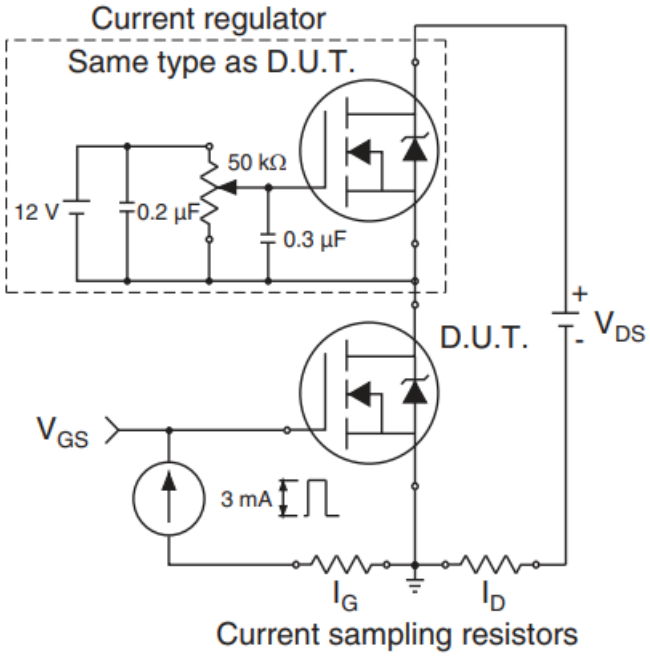
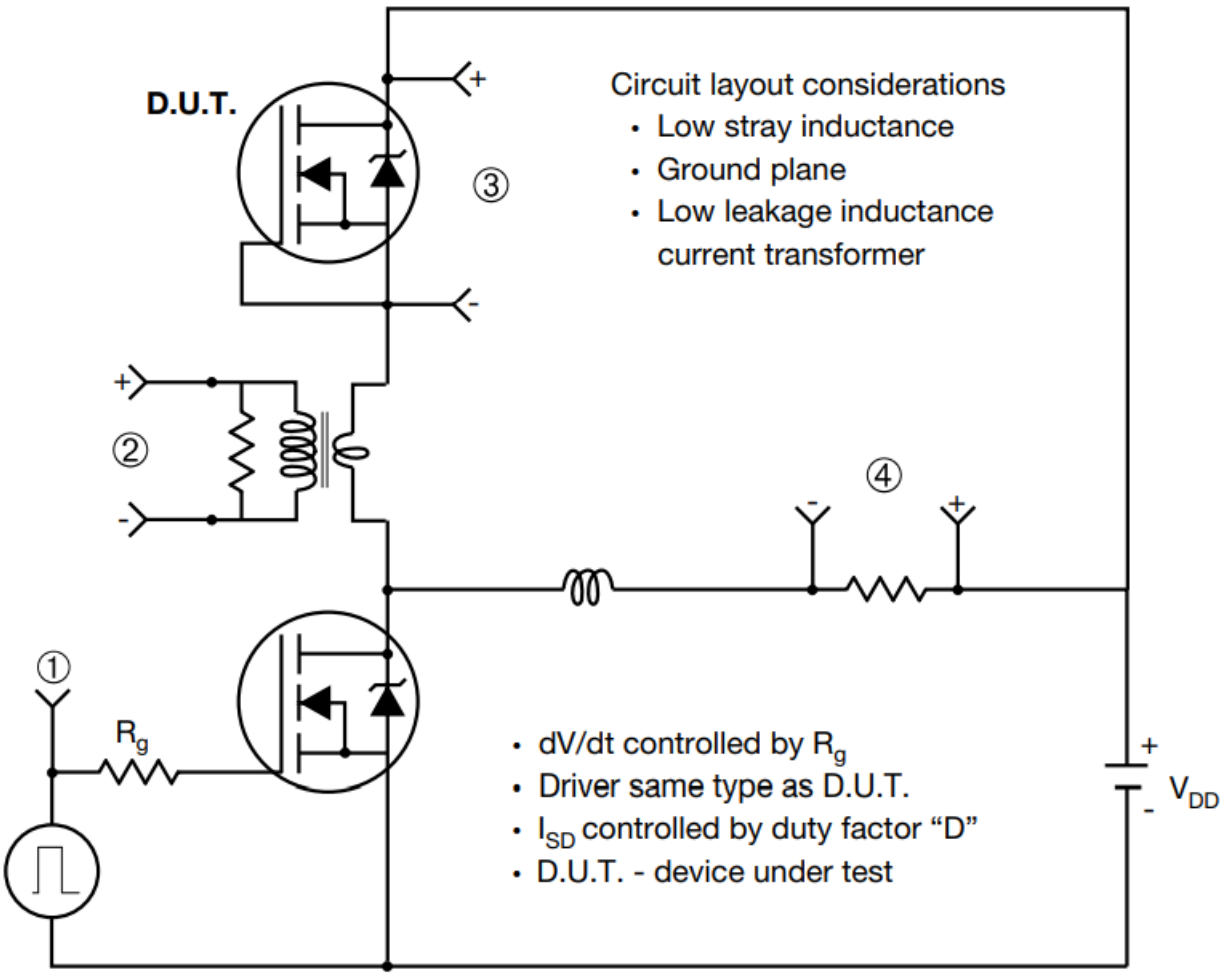


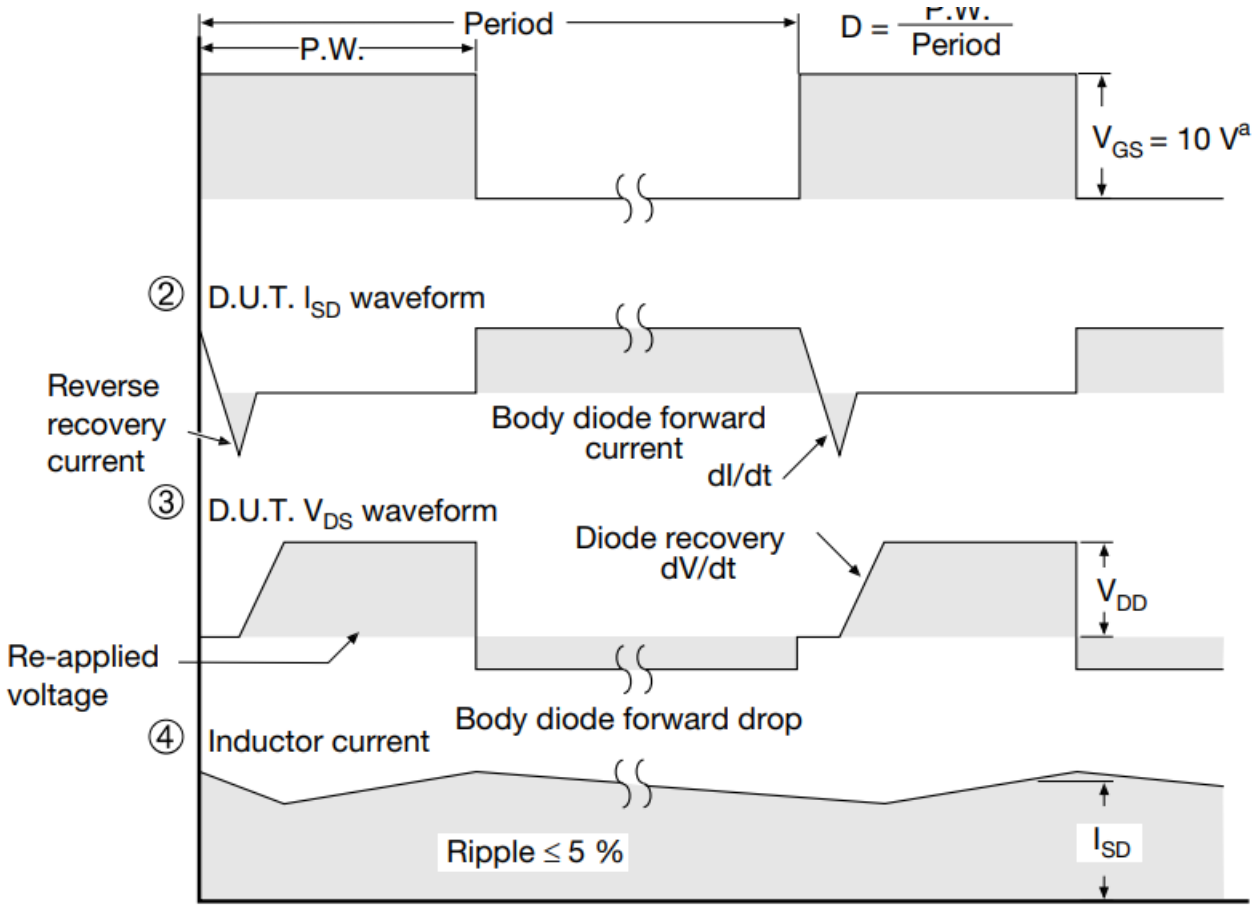
Fig. 17 – Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



Driver gate drive

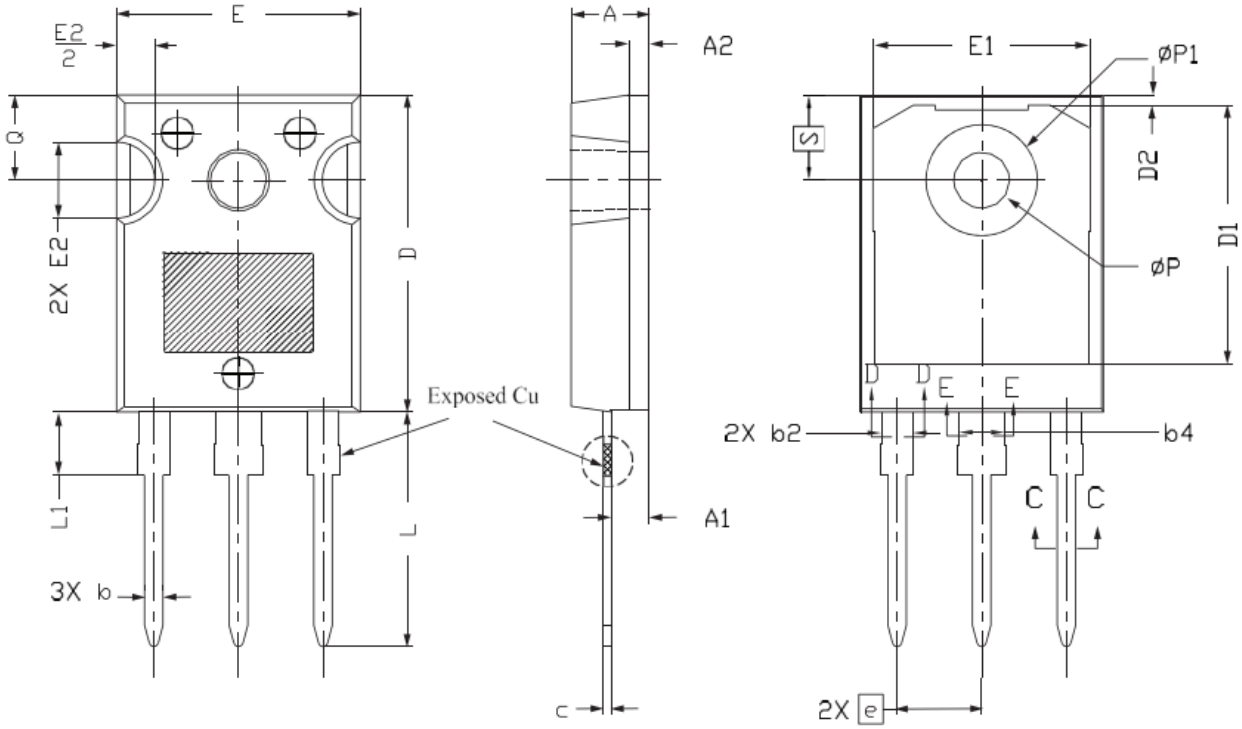


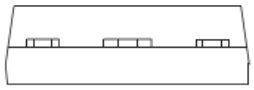
Note
a. VGS= 5 V for logic level devices
Fig. 18 – For N-Channel

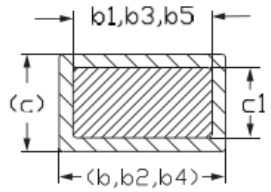
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see **www.vishay.com/ppg?91251**.

TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D–D,E–E

	MILLIMETERS			
DIM.	**MIN.**	**NOM.**	**MAX.**	**NOTES**
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

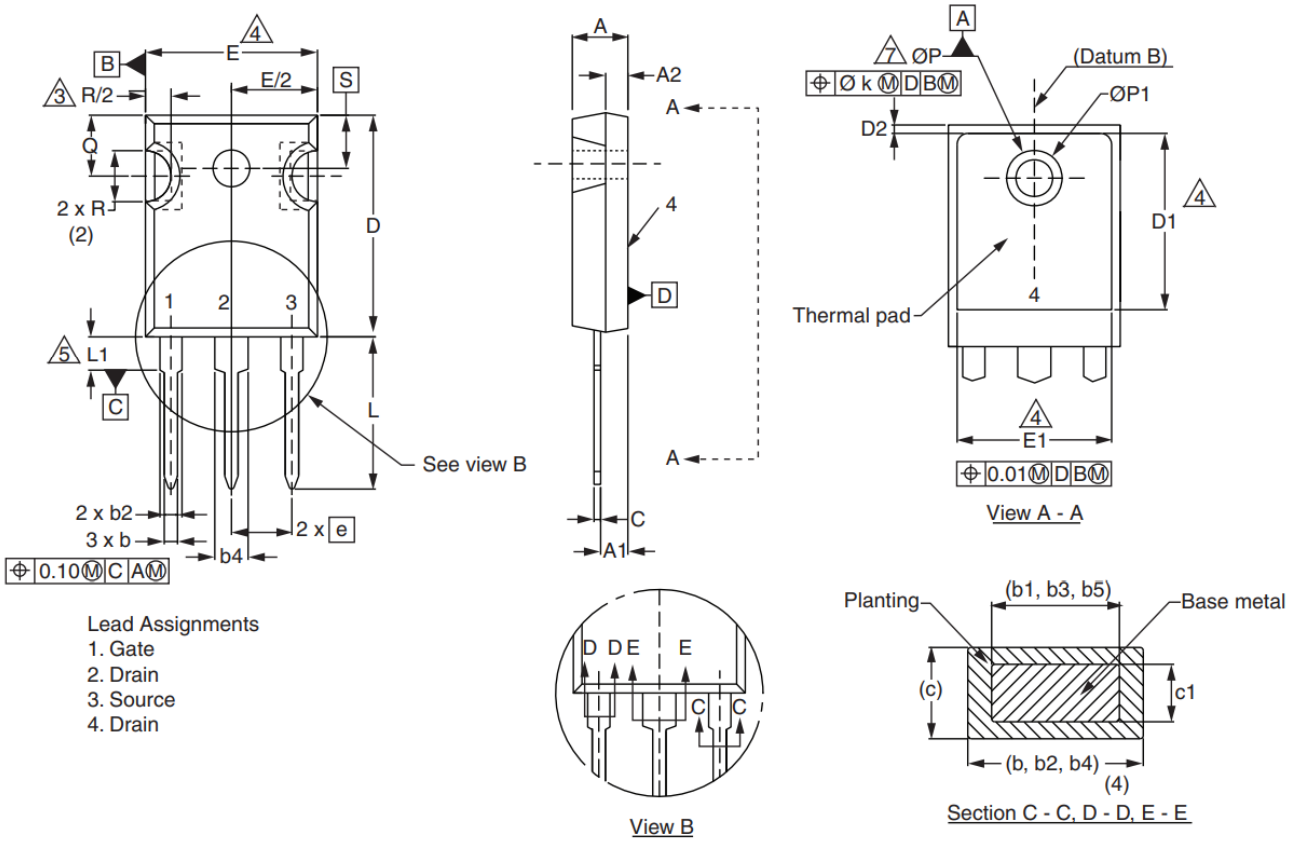
	MILLIMETERS			
DIM.	**MIN.**	**NOM.**	**MAX.**	**NOTES**
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

Notes

1. Package reference: JEDEC
2. TO247, variation AC
3. All dimensions are in mm
4. Slot required, notch may be rounded
5. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
6. Thermal pad contour optional with dimensions D1 and E1
7. Lead finish uncontrolled in L1
8. Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
9. Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

Package Information

VERSION 2: FACILITY CODE = Y



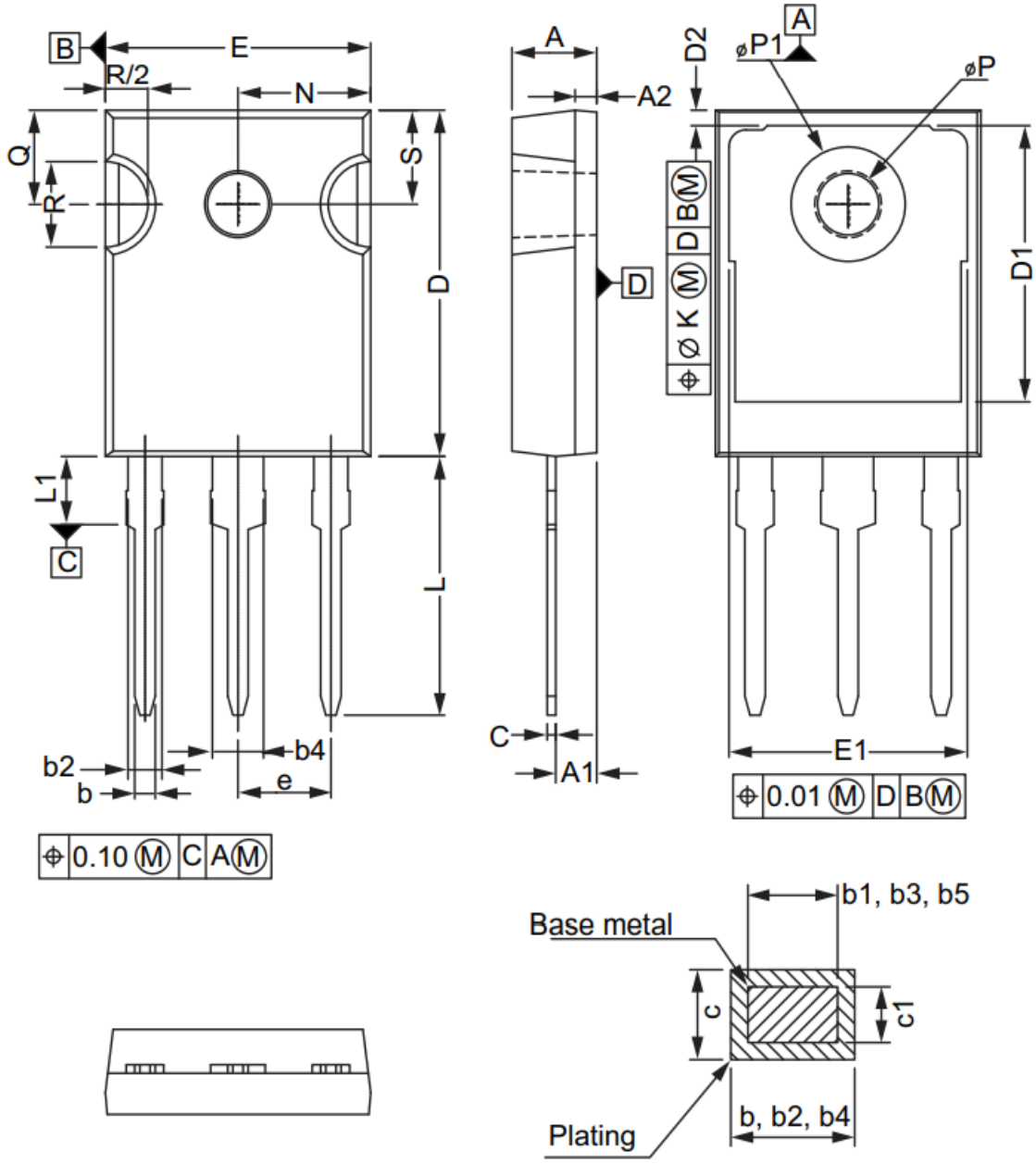
	MILLIMETERS		
DIM.	**MIN.**	**MAX.**	**NOTES**
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	–	

	MILLIMETERS		
DIM.	**MIN.**	**MAX.**	**NOTES**
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	–	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	–	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Contour of slot optional
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005″) per side. These dimensions are measured at the outermost extremes of the plastic body
4. Thermal pad contour optional with dimensions D1 and E1
5. Lead finish uncontrolled in L1
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154″)
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c

VERSION 3: FACILITY CODE = N


B
E
R/2
N
Q
R
S
D
L1
C
L
b2
b
b4
e
0.10 M C A M
A
A2
D
C
A1
D2
øP1
A
øP
D1
D B M
Ø K M
E1
0.01 M D B M

b1, b3, b5
Base metal
c
c1
Plating
b, b2, b4

	MILLIMETERS	
DIM.	**MIN.**	**MAX.**
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	–

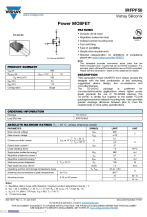
	MILLIMETERS	
DIM.	**MIN.**	**MAX.**
D2	0.51	1.35
E	15.29	15.87
E1	13.46	–
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	–	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Contour of slot optional
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005″) per side. These dimensions are measured at the outermost extremes of the plastic body
4. Thermal pad contour optional with dimensions D1 and E1
5. Lead finish uncontrolled in L1
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154″)

Legal Disclaimer Notice

Documents / Resources

	VISHAY IRFPF50 Siliconix Power MOSFET [pdf] Instruction Manual IRFPF50, IRFPF50 Siliconix Power MOSFET, MOSFET, Power MOSFET, IRFPF50 Power MOSFET, Siliconix Power MOSFET

References

- applications.no
- vishay.com/doc?91000
- IRFPF50 MOSFETs | Vishay