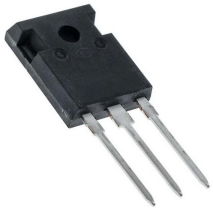
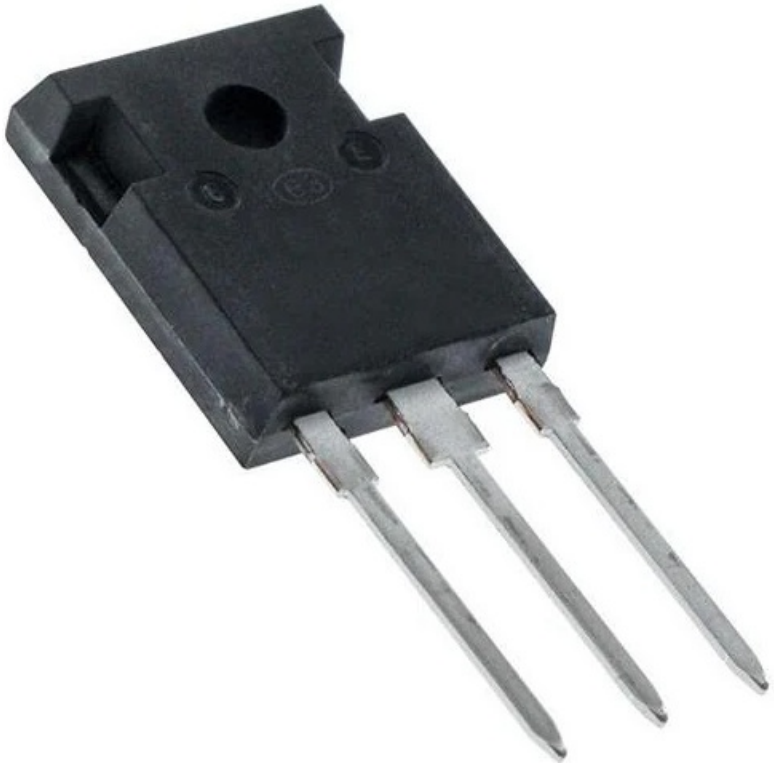
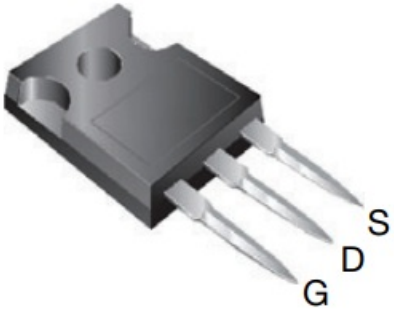


VISHAY IRFPC60LC Siliconix Mouser India Instructions

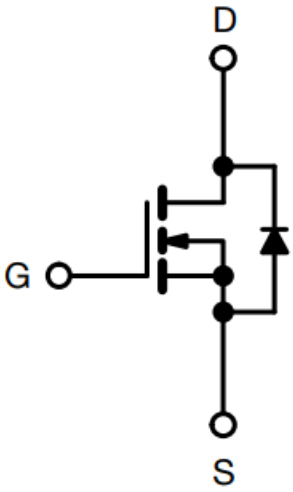
VISHAY IRFPC60LC Siliconix Mouser India Instructions



TO-247AC



N-Channel MOSFET’



Contents

PRODUCT SUMMARY

V_{DS} (V)	600	
RDS(on) (W)	V_{GS} = 10 V	0.40
Q_g (max.) (nC)	120	
Q_{gs} (nC)	29	
Q_{gd} (nC)	48	
Configuration	Single	

FEATURES

- Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V VGS rating
- Reduced Ciss, Coss, Crss
- Isolated central mounting hole
- Dynamic dV/dt rated
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see **www.vishay.com/doc?99912**

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant.
Please see the information / tables in this datasheet for details

DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs.
Utilizing advanced Power MOSFETs technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings.
These device improvements combined with the proven ruggedness and reliability of Power MOSFETs offer the designer a new standart in power transistors for switching applications.
The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFPC60LCPbF

ABSOLUTE MAXIMUM RATINGS

(T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			VDS	600	V
Gate-source voltage			VGS	± 30	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	16	A
		T_C = 100 °C		10	
Pulsed drain current a			IDM	64	
Linear derating factor				2.2	W/°C
Single pulse avalanche energy b			EAS	1000	mJ
Repetitive avalanche current a			IAR	16	A
Repetitive avalanche energy a			EAR	28	mJ
Maximum power dissipation	T_C = 25 °C		P_D	280	W
Peak diode recovery dV/dt c			dV/dt	3.0	V/ns
Operating junction and storage temperature range			TJ, Tstg	-55 to +150	°C
Soldering recommendations (peak temperature)	for 10 s			300 d	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

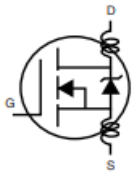
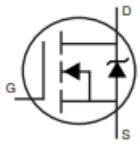
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. VDD = 25 V, starting TJ = 25 °C, L = 7.2 mH, Rg = 25 Ω, IAS = 16 A (see fig. 12)
c. ISD ≤ 16 A, dI/dt ≤ 140 A/μs, VDD ≤ VDS, TJ ≤ 150 °C
d. 1.6 mm from c

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	RthJA	–	40	°C/W
Case-to-sink, flat, greased surface	RthCS	0.24	–	
Maximum junction-to-case (drain)	RthJC	–	0.45	

SPECIFICATIONS (Tj = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	Vos	VGs = 0 V, ID = 250 pA		600		–	V
Vjas temperature coefficient	AVGillij	Reference to 25 °C, ID = 1 mA		–	0.63		V/°C
Gate-source threshold voltage	VGSM	VDs = V. ID = 250 pA		2.0		4.0	V
Gate-source leakage	IGss	VGs = ± 20 V		–		t 100	DA
Zero gate voltage drain current	loss	VDD = 600V, VDD = OV				25	PA
		VD = 480 V, VGs = 0 V, Tj = 125 ° C		–		250	
Drain-source on-state resistance	RDSon)	VGs = 10 V I	io = 9.6 Al’	–		0.40	(2
Forward transconductance	gts	VDs = 50 V, ID = 9.6 A		11		–	S
Dynamic							
Input capacitance	Ciss	VDs = 0 V. VDs = 25 V. f = 1.0 MHz, see fig. 5		–	3500	–	pF
Output capacitance	Coss			–	400		
Reverse transfer capacitance	Crss			–	39	–	
Output capacitance	9	VDs=10V	b= 16 A, VDS = 360 V, see fig. 6 and 13 b				nC
	O se			–	–	29	
Effective output capacitance	Ogd			–	–	48	
Total gate charge	feicini			–	17	–	

Gate-source charge	t,	VD0 = 300 V, ID = 16 A, Rg = 4.3 CI, RD = 18 CI, see fig. 10 lii	–	57	–	ns
Gate-drain charge	frrioff)		–	43	–	
Turn-on delay time	tr		–	38	–	
Intemal drain inductance	Lo	Between lead, 6 mm (0.251 from package and center of die contact 	–	5.0	–	nH
Internal source inductance	Ls		–	13	–	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	IS	MOSFET symbol showing the integral reverse p – n junction. diode 	–	–	16	A
Pulsed diode forward currents	Ism		–		64	
Body diode voltage	VSD	T j = 25 °C, Is = 16 A, VGs= 0 V b	–		2.	V
Body diode reverse recovery time	tn.	= 16 A, dVdt = 100 A/ps	–	650	980	ns
Body diode reverse recovery charge	On	TJ 25 °C, = IF	–	6.0	9.0	pC
Forward turn-on time	ton	Intrinsic turn-on time is negligible (turn-on is dominated by Ls and Lo)				

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS

(25 °C, unless otherwise noted)

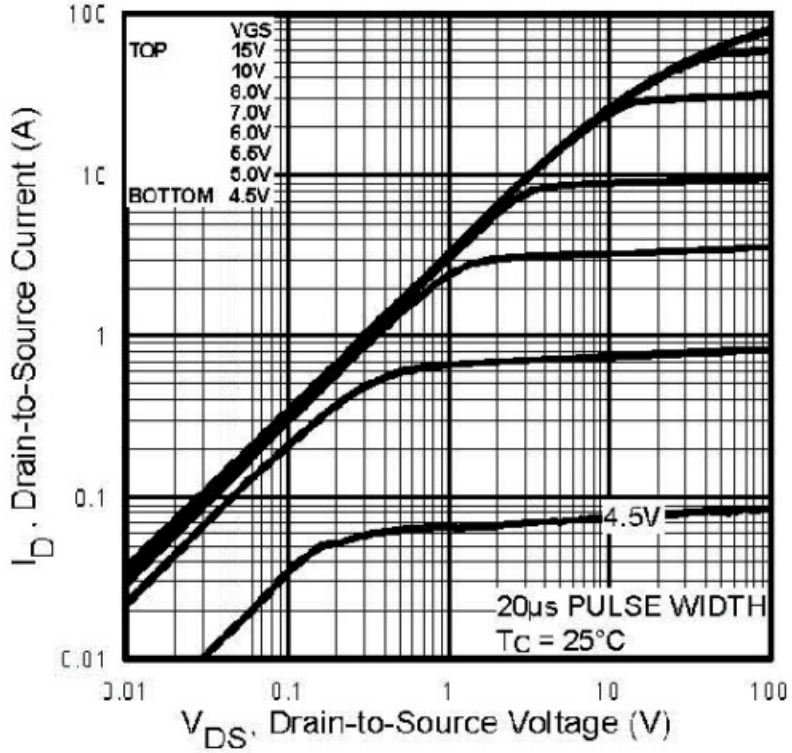


Fig. 1 – Typical Output Characteristics, TC = 25 °C

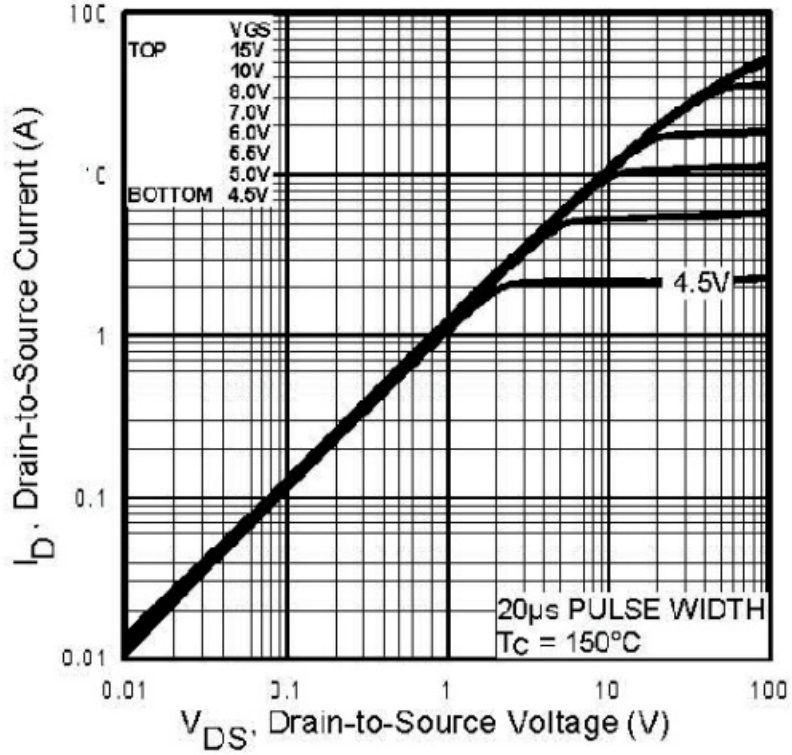


Fig. 2 – Typical Output Characteristics, TC = 150 °C

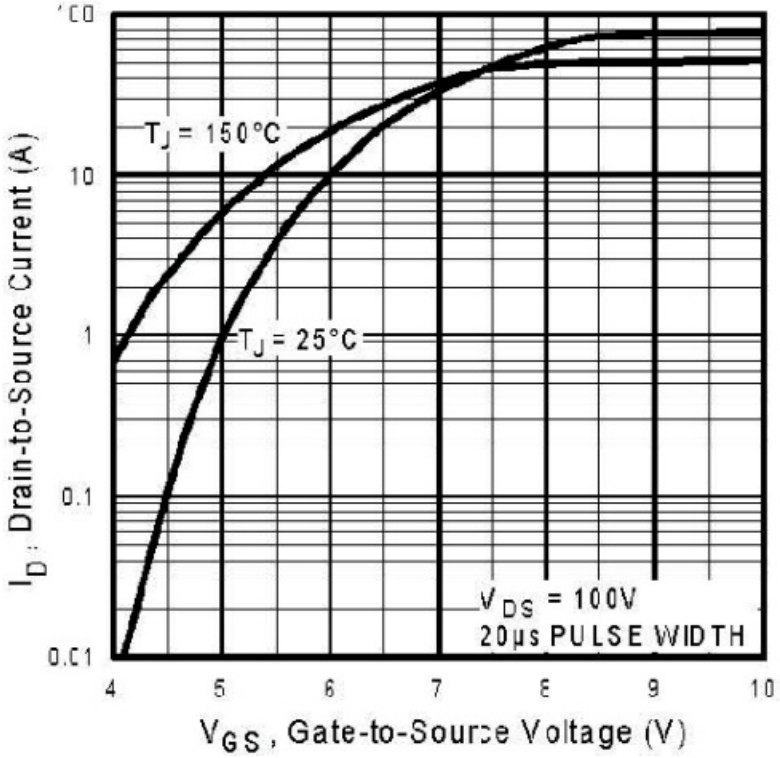


Fig. 3 – Typical Transfer Characteristics

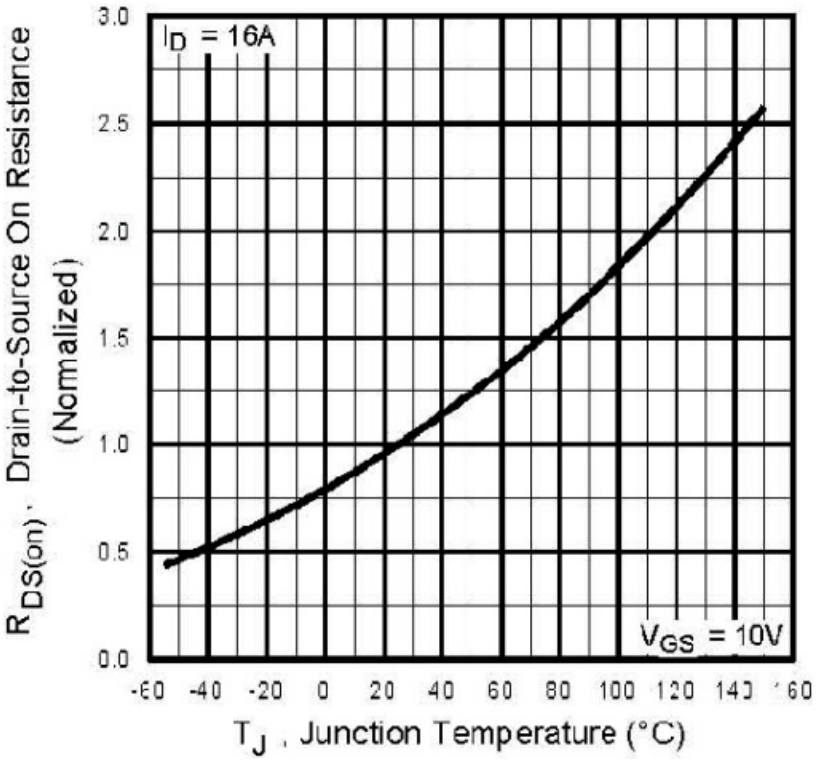


Fig. 4 – Normalized On-Resistance vs. Temperature

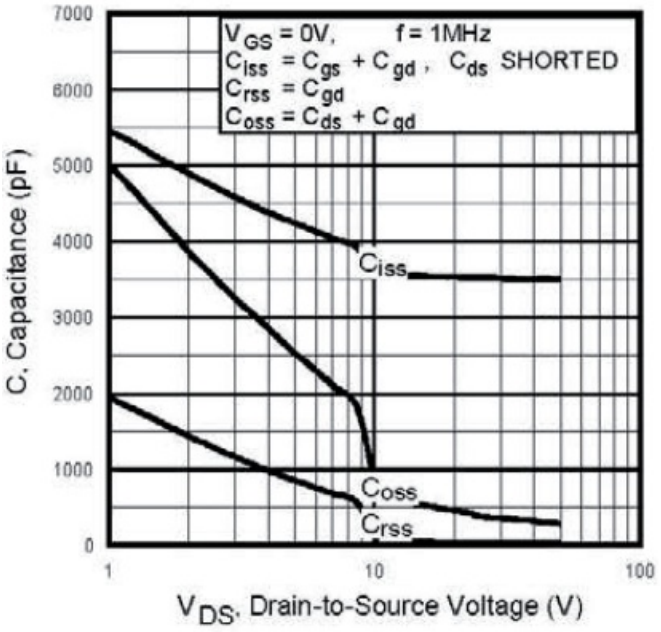


Fig. 5 – Typical Capacitance vs. Drain-to-Source Voltage

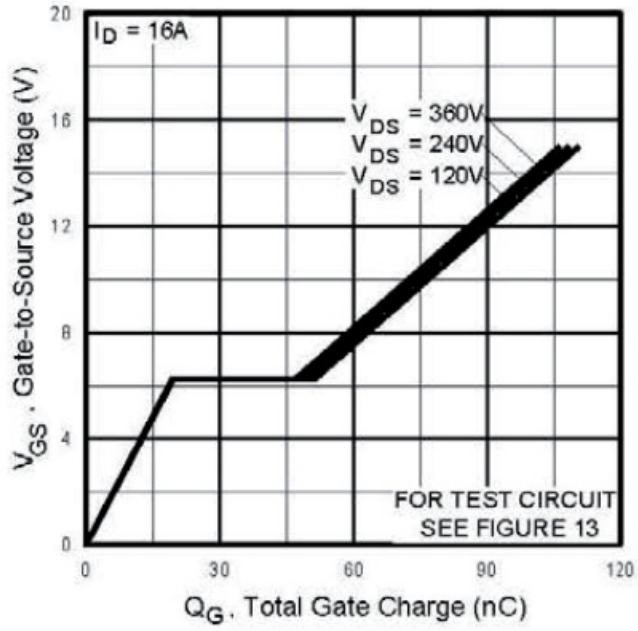


Fig. 6 – Typical Gate Charge vs. Gate-to-Source Voltage

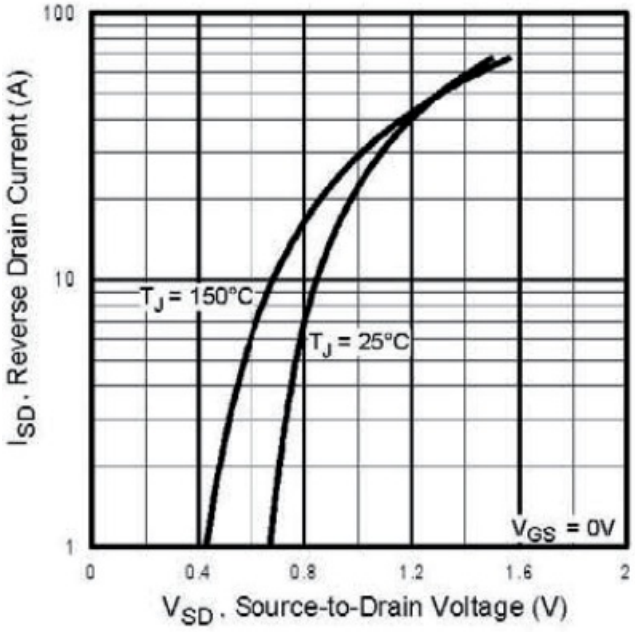


Fig. 7 – Typical Source-Drain Diode Forward Voltage

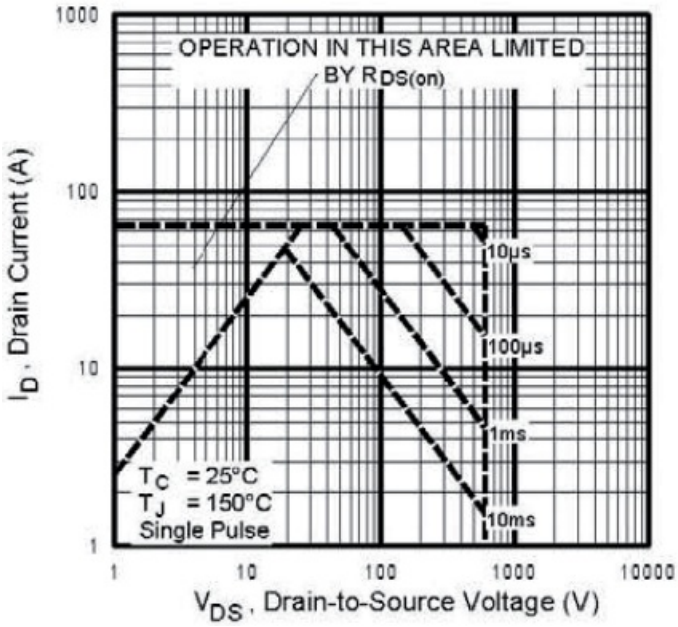


Fig. 8 – Maximum Safe Operating Area

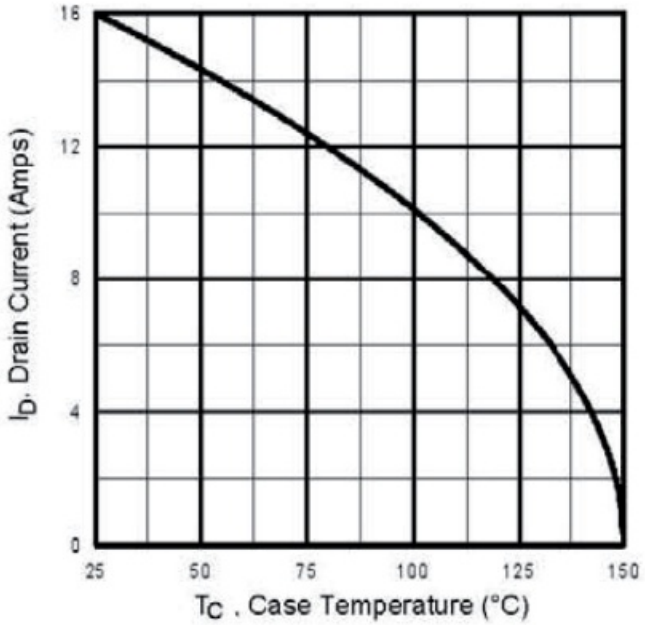


Fig. 9 – Maximum Drain Current vs. Case Temperature

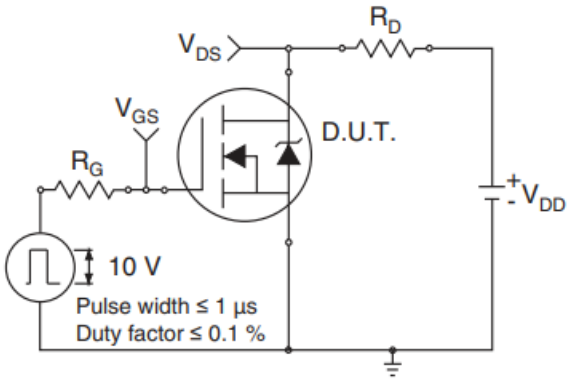


Fig. 10 – Switching Time Test Circuit

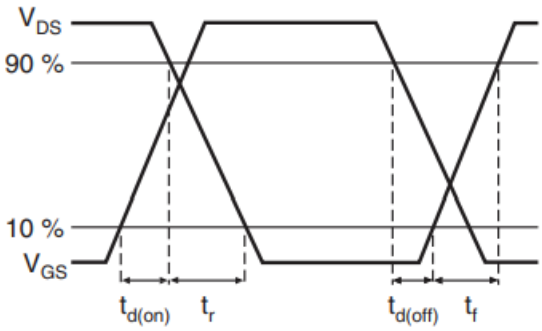


Fig. 11 – Switching Time Waveforms

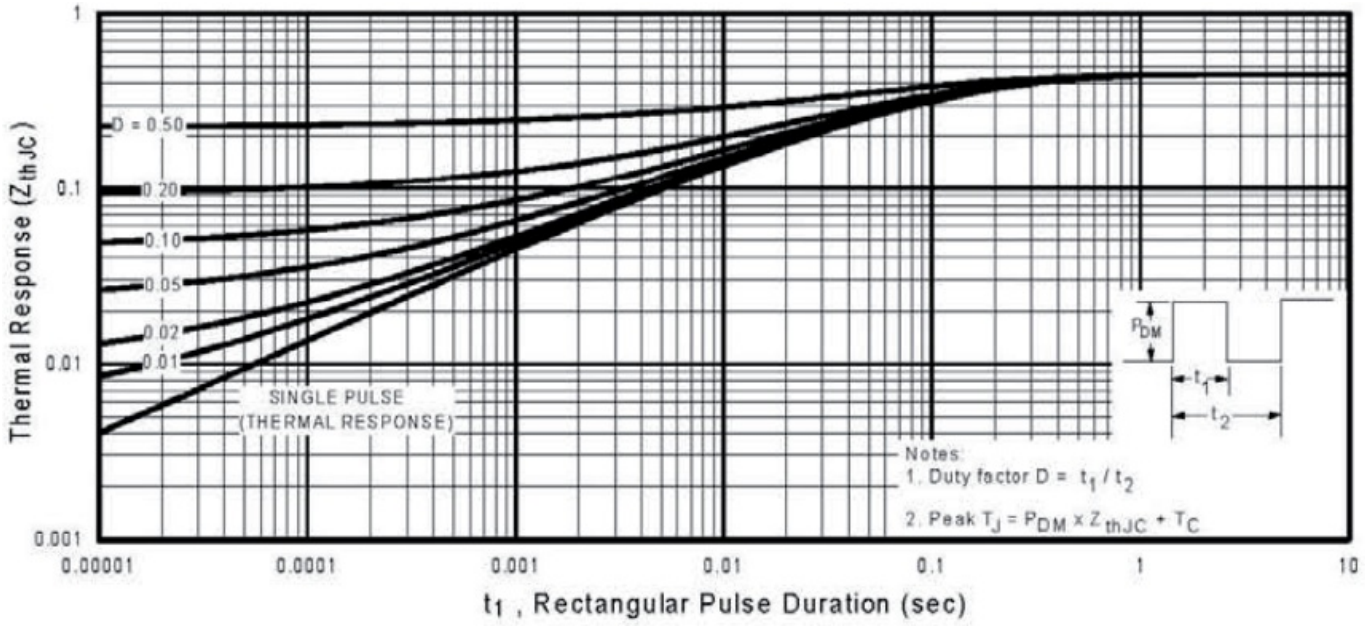


Fig. 12 – Maximum Effective Transient Thermal Impedance, Junction-to-Case

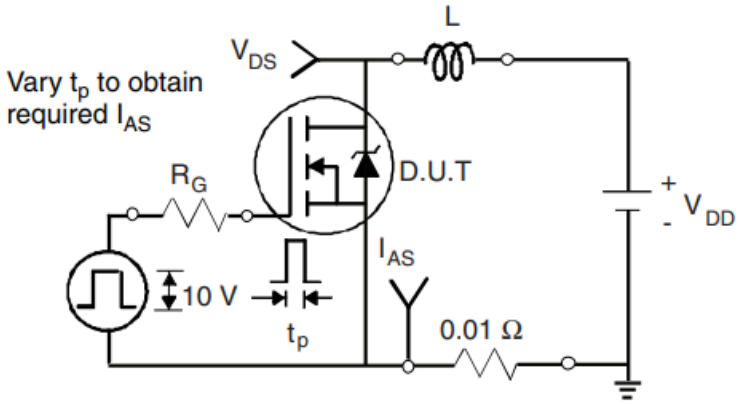


Fig. 13 – Unclamped Inductive Test Circuit

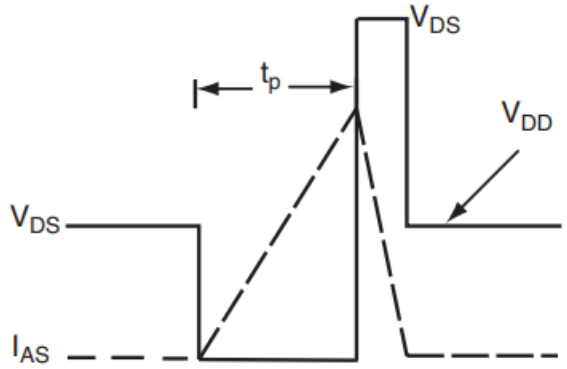


Fig. 14 – Unclamped Inductive Waveforms

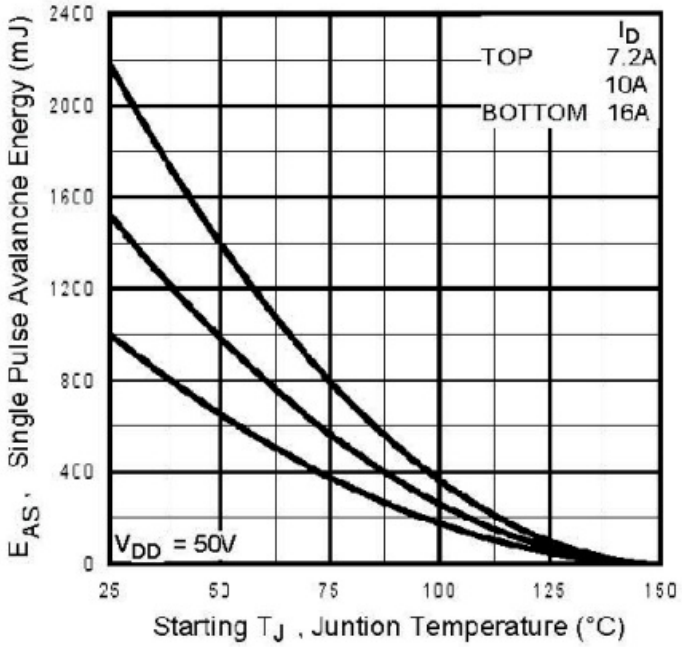


Fig. 15 – Maximum Avalanche Energy vs. Drain Current

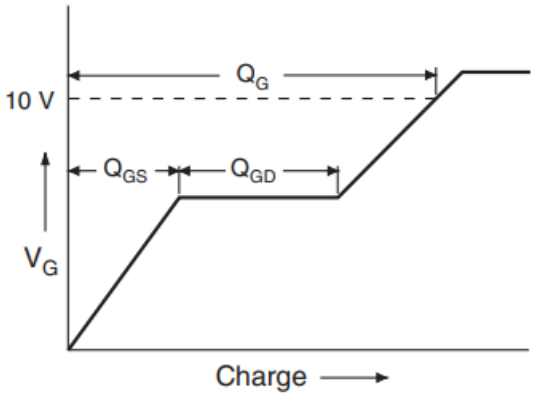


Fig. 16 – Basic Gate Charge Waveform

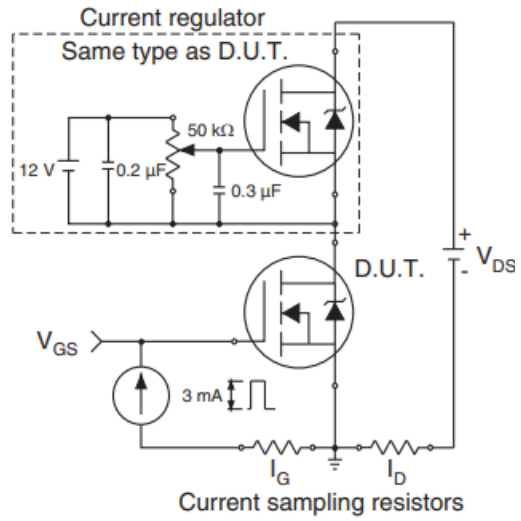


Fig. 17 – Gate Charge Test

Peak Diode Recovery dV/dt Test Circuit

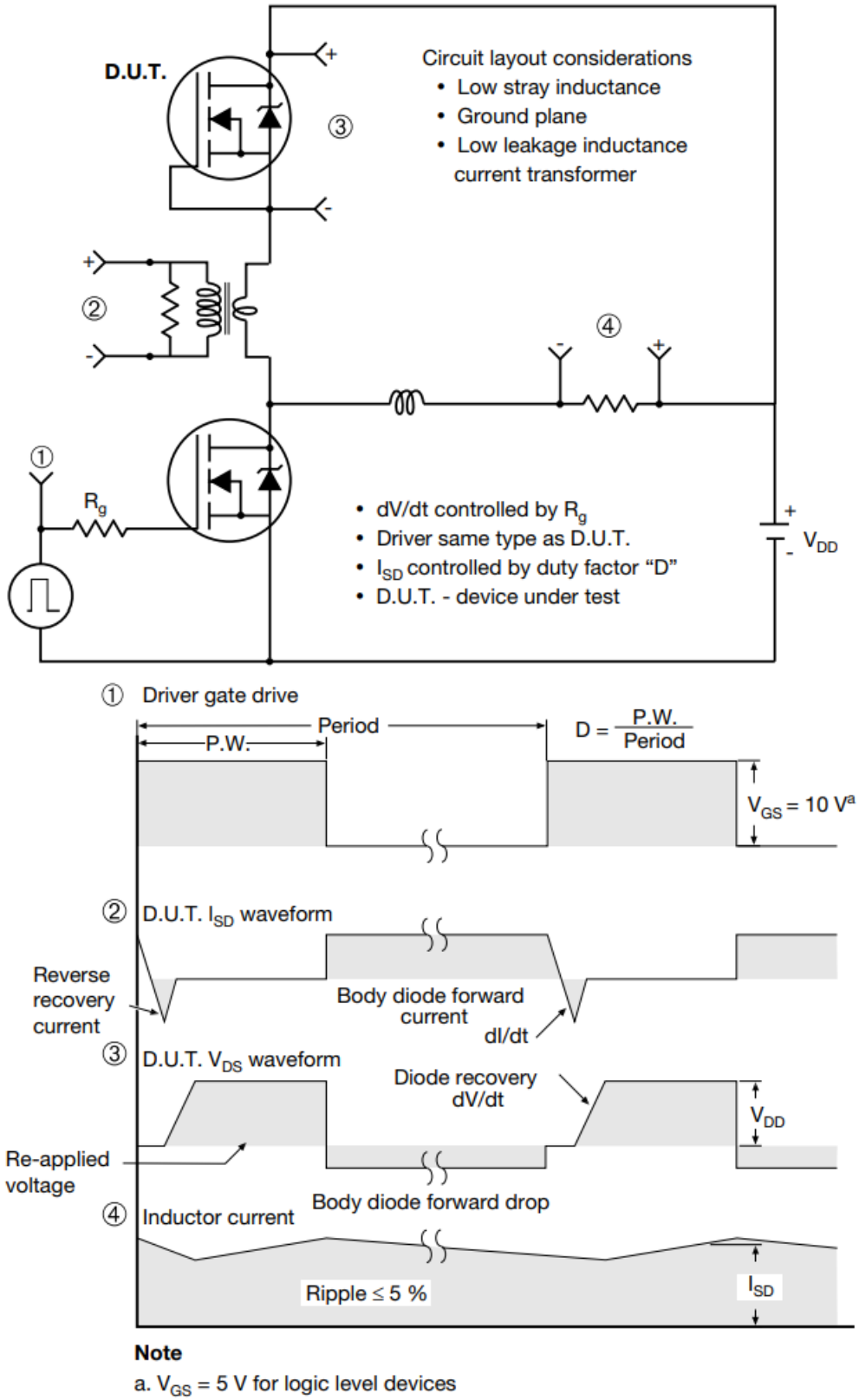


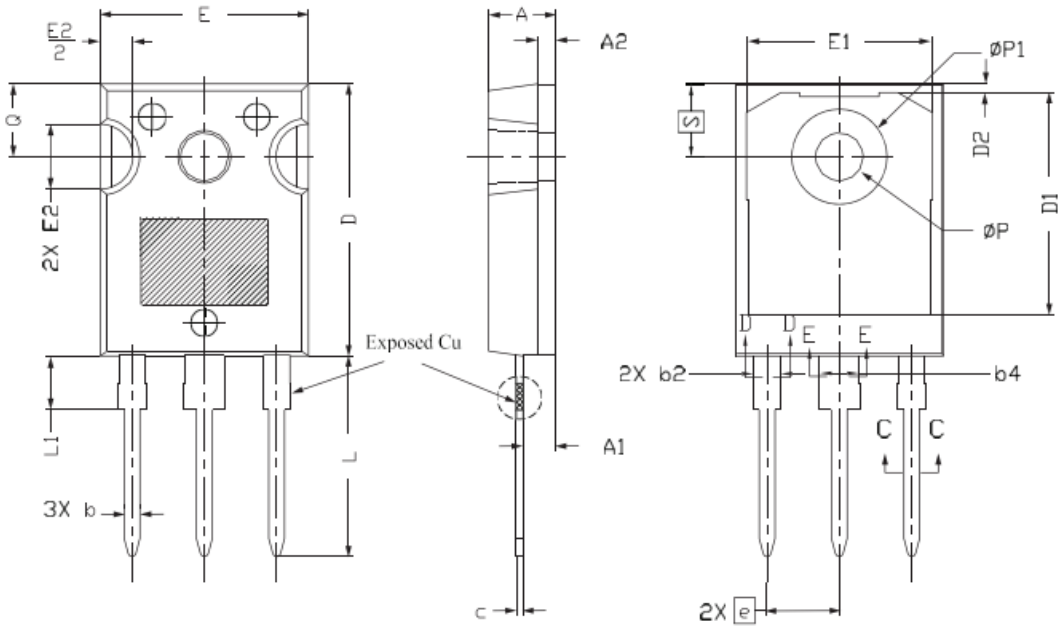
Fig. 18 – For N-Channel

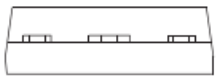
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91244.

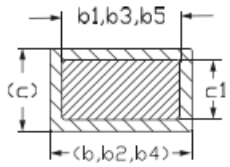
Package Information

TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D--D,E--E

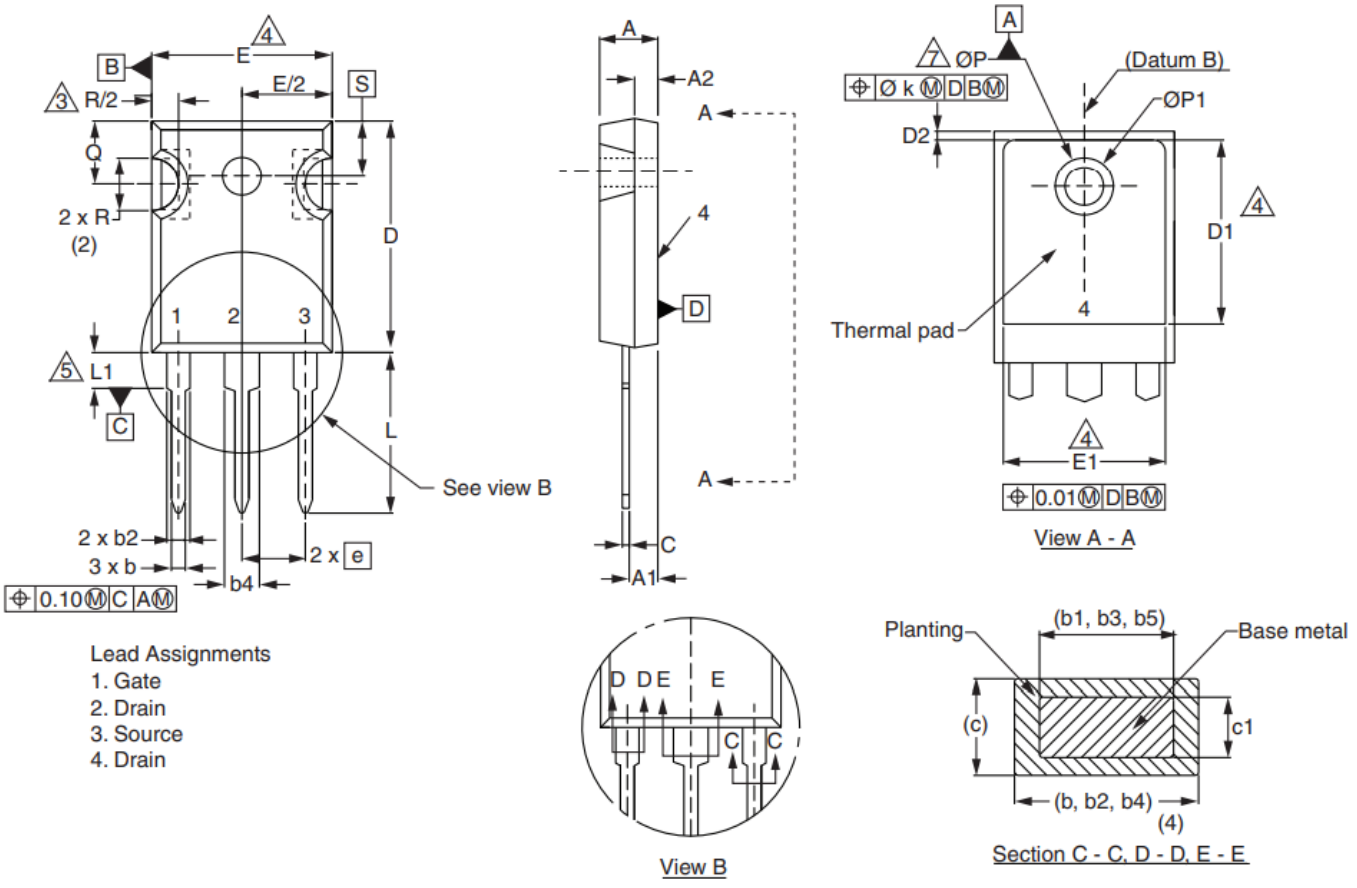
	MILLIMETERS			
DIM.	**MIN.**	**NOM.**	**MAX.**	**NOTES**
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

	MILLIMETERS			
DIM.	**MIN.**	**NOM.**	**MAX.**	**NOTES**
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

Notes

1. Package reference: JEDEC® TO247, variation AC
2. All dimensions are in mm
3. Slot required, notch may be rounded
4. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
5. Thermal pad contour optional with dimensions D1 and E1
6. Lead finish uncontrolled in L1
7. Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
8. Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

VERSION 2: FACILITY CODE = Y



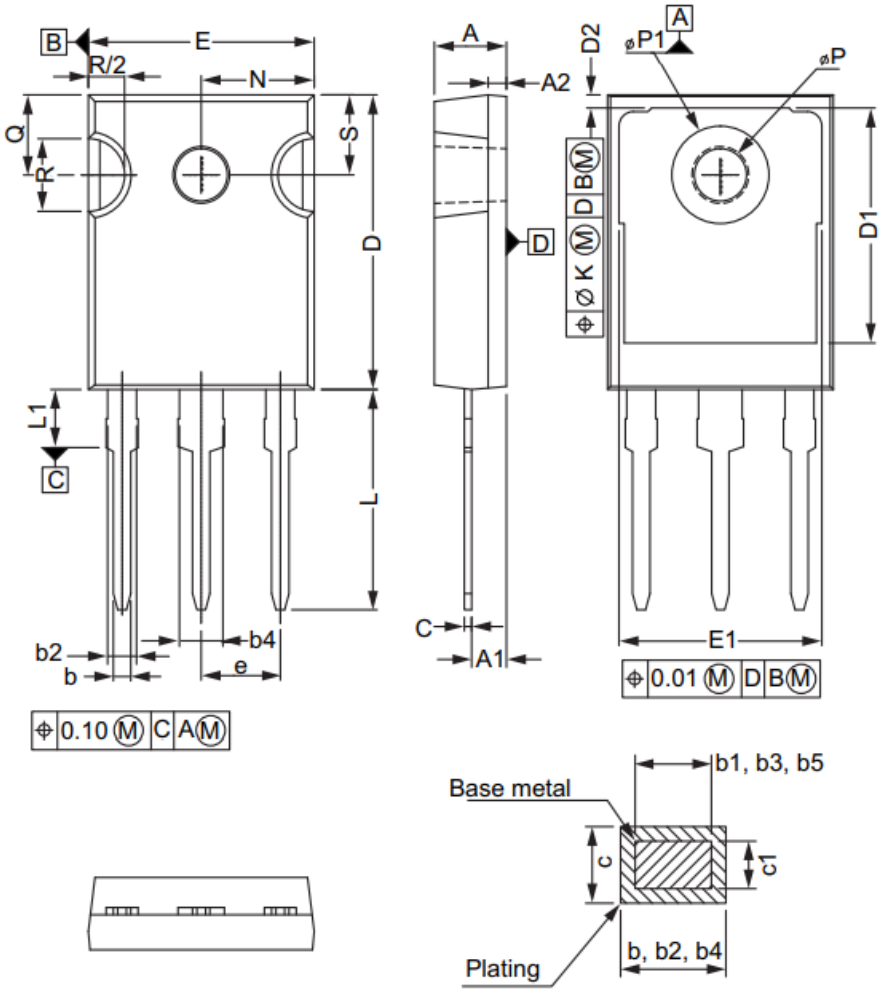
	MILLIMETERS		
DIM.	**MIN.**	**MAX.**	**NOTES**
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	–	

	MILLIMETERS		
DIM.	**MIN.**	**MAX.**	**NOTES**
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	–	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	–	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Contour of slot optional
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005″) per side. These dimensions are measured at the outermost extremes of the plastic body
4. Thermal pad contour optional with dimensions D1 and E1
5. Lead finish uncontrolled in L1
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154″)
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c

VERSION 3: FACILITY CODE = N



	MILLIMETERS				MILLIMETERS	
DIM.	**MIN.**	**MAX.**		**DIM.**	**MIN.**	**MAX.**
A	4.65	5.31		D2	0.51	1.35
A1	2.21	2.59		E	15.29	15.87
A2	1.17	1.37		E1	13.46	–
b	0.99	1.40		e	5.46 BSC	
b1	0.99	1.35		k	0.254	
b2	1.65	2.39		L	14.20	16.10
b3	1.65	2.34		L1	3.71	4.29
b4	2.59	3.43		N	7.62 BSC	
b5	2.59	3.38		P	3.56	3.66
c	0.38	0.89		P1	–	7.39
c1	0.38	0.84		Q	5.31	5.69
D	19.71	20.70		R	4.52	5.49
D1	13.08	–		S	5.51 BSC	
ECN: E22-0452-Rev. G, 31-Oct-2022 DWG: 5971						

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Contour of slot optional
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005″) per side. These dimensions are measured at the outermost extremes of the plastic body
4. Thermal pad contour optional with dimensions D1 and E1
5. Lead finish uncontrolled in L1
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154″)

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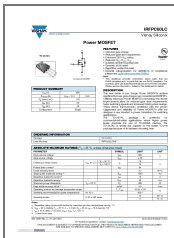
Documents / Resources

	VISHAY IRFPC60LC Siliconix Mouser India [pdf] Instructions IRFPC60LC Siliconix Mouser India, IRFPC60LC, Siliconix Mouser India, Mouser India, India

References

- Vishay Intertechnology: Passives & Discrete Semiconductors
- User Manual