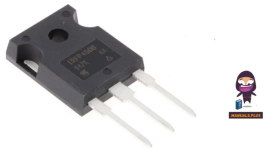
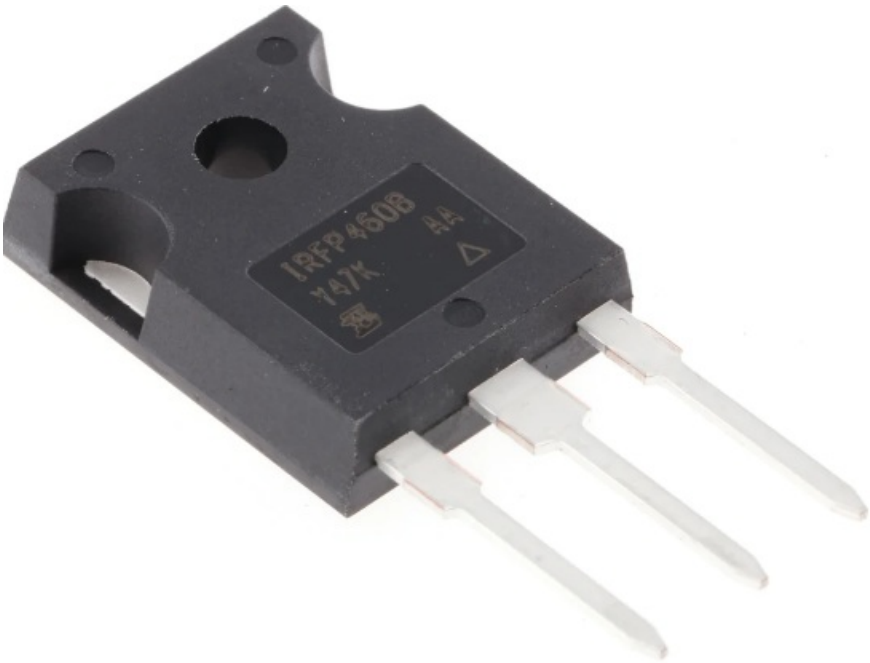
VISHAY IRFP460B D Series Power MOSFET



VISHAY IRFP460B D Series Power MOSFET User Manual

Contents

VISHAY IRFP460B D Series Power MOSFET



Product Information

- The IRFP460B and SiHG460B are D Series Power MOSFETs manufactured by Vishay Siliconix. These MOSFETs are N-Channel devices designed for high voltage applications.
- The IRFP460B has a drain-source voltage (VDS) rating of 550 V and a gate-source voltage (VGS) rating of 10 V. It comes in a TO-247AC package with lead (Pb)-free and halogen-free options.
- The SiHG460B has the same specifications as the IRFP460B and is also available in a TO-247AC package.

Specifications

Parameter	Symbol	Value	Unit
Drain-Source Voltage	VDS	550	V
Gate-Source Voltage	VGS	10	V
Pulsed Drain Current	ID	170	A
Maximum Power Dissipation	PD	300	W
Operating Junction and Storage Temperature Range	TJ, Tstg	-55 to +150	°C

Product Usage Instructions

Installation

1. Ensure that the power supply is turned off and disconnected before installation.
2. Select an appropriate heat sink for the MOSFET to dissipate heat effectively.
3. Mount the MOSFET securely on the heat sink using thermal paste or a thermal pad.
4. Connect the drain, gate, and source pins of the MOSFET to the appropriate circuitry according to your application requirements.
5. Double-check all connections and ensure that there are no short circuits before applying power.

Operation

Once the MOSFET is properly installed, follow these guidelines for its operation:

- Ensure that the gate-source voltage (VGS) does not exceed the specified maximum value of 10 V.
- Maintain the drain-source voltage (VDS) within the specified range of up to 550 V.
- Do not exceed the maximum pulsed drain current (ID) rating of 170 A.
- Monitor the temperature of the MOSFET during operation and ensure it stays within the specified operating temperature range of -55 to +150 °C.

FAQ

Q: Are the IRFP460B and SiHG460B lead (Pb)-free?

A: Yes, both models are available in lead (Pb)-free options. The IRFP460B is also available in a lead (Pb)-free and halogen-free version.

Q: What is the maximum power dissipation of the MOSFET?

A: The maximum power dissipation (PD) is 300 W.

Q: Can I use these MOSFETs in high voltage applications?

A: Yes, these MOSFETs are designed for high voltage applications with a drain-source voltage (VDS) rating of 550 V.

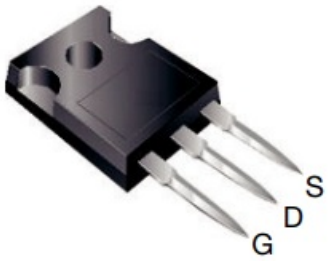
Q: What is the recommended operating temperature range for the MOSFET?

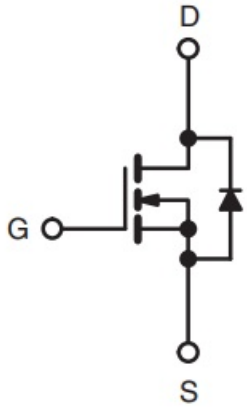
A: The recommended operating temperature range is -55 to +150 °C.

D Series Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (W)	V_{GS} = 10 V	0.25
Q_g max. (nC)	170	
Q_{gs} (nC)	14	
Q_{gd} (nC)	28	
Configuration	Single	

TO-247AC





N-Channel MOSFET

FEATURES

- Optimal Design
  - Low Area Specific On-Resistance
  - Low Input Capacitance (C_{iss})
  - Reduced Capacitive Switching Losses
  - High Body Diode Ruggedness
  - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
  - Low Cost
  - Simple Gate Drive Circuitry
  - Low Figure-of-Merit (FOM): $R_{on} \times Q_g$
  - Fast Switching
- Material categorization: For definitions of compliance please see **www.vishay.com/doc?99912**
- **Note**

  * Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

APPLICATIONS

- Consumer Electronics

  Displays (LCD or Plasma TV)
- Server and Telecom Power Supplies

  SMPS
- Industrial
  - Welding
  - Induction Heating
  - Motor Drives
- Battery Chargers
- SMPS

  Power Factor Correction (PFC)

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFP460BPbF
Lead (Pb)-free and Halogen-free	SiHG460B-GE3

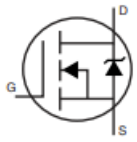
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			VDS	500	V
Gate-Source Voltage			VGS	± 20	
Gate-Source Voltage AC (f > 1 Hz)				30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	20	A
		T_C = 100 °C		13	
Pulsed Drain Currenta			IDM	62	
Linear Derating Factor				2.2	W/°C
Single Pulse Avalanche Energyb			EAS	281	mJ
Maximum Power Dissipation			P_D	278	W
Operating Junction and Storage Temperature Range			TJ, Tstg	– 55 to + 150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	24	V/ns
Reverse Diode dV/dtd				0.36	
Soldering Recommendations (Peak Temperature)	for 10 s			300c	°C

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. VDD = 50 V, starting TJ = 25 °C, L = 10 mH, Rg = 25 , IAS = 7.5 A.
- c. 1.6 mm from case.
- d. ISD ID, starting TJ = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	RthJA	–	40	°C/W
Maximum Junction-to-Case (Drain)	RthJC	–	0.45	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	VDS	V_{GS} = 0 V, I_D = 250 μA	500	–	–	V
V_{DS} Temperature Coefficient	DV_{DS}/T_J	Reference to 25 °C, I_D = 250 μA	–	0.56	–	V/°C
Gate-Source Threshold Voltage (N)	VGS(th)	V_{DS} = V_{GS}, I_D = 250 μA	2	–	4	V
Gate-Source Leakage	IGSS	V_{GS} = ± 20 V	–	–	± 100	nA
Zero Gate Voltage Drain Current	IDSS	V_{DS} = 500 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	–	–	10	
Drain-Source On-State Resistance	RDS(on)	V_{GS} = 10 V, I_D = 10 A	–	0.2	0.25	W
Forward Transconductance	gfs	V_{DS} = 50 V, I_D = 10 A	–	12	–	S
Dynamic						
Input Capacitance	Ciss	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	–	3094	–	pF
Output Capacitance	Coss		–	152	–	
Reverse Transfer Capacitance	Crss		–	13	–	
Effective output capacitance, energy relateda	Co(er)	V_{GS} = 0 V, V_{DS} = 0 V to 400 V	–	131	–	
Effective output capacitance, time relatedb	Co(tr)		–	189	–	
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 10 A, V_{DS} = 400 V	–	85	170	nC
Gate-Source Charge	Qgs		–	14	–	
Gate-Drain Charge	Qgd		–	28	–	
Turn-On Delay Time	td(on)	V_{DD} = 400 V, I_D = 10 A, V_{GS} = 10 V, R_g = 9.1 W	–	24	50	ns
Rise Time	t_r		–	31	62	
Turn-Off Delay Time	td(off)		–	117	176	
Fall Time	t_f		–	56	112	
Gate Input Resistance	R_g	f = 1 MHz, open drain	–	1.8	–	W
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p – n junction diode	–	–	20	

Pulsed Diode Forward Current	ISM		–	–	80	A
Diode Forward Voltage	VSD	T_J = 25 °C, I_S = 10 A, V_{GS} = 0 V	–	–	1.2	V
Reverse Recovery Time	trr	T_J = 25 °C, I_F = I_S = 10 A, dI/dt = 100 A/µs, V_R = 20 V	–	437	–	ns
Reverse Recovery Charge	Qrr		–	5.9	–	µC
Reverse Recovery Current	IRRM		–	25	–	A

Notes

- a. Coss(er) is a fixed capacitance that gives the same energy as Coss while VDS is rising from 0 % to 80 % VDS.
- b. Coss(tr) is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 % to 80 % VDS.

TYPICAL CHARACTERISTICS

(25 °C, unless otherwise noted)

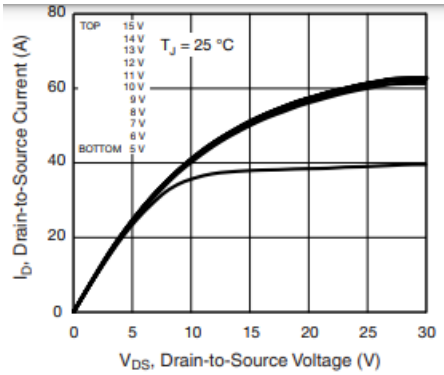


Fig. 1 - Typical Output Characteristics

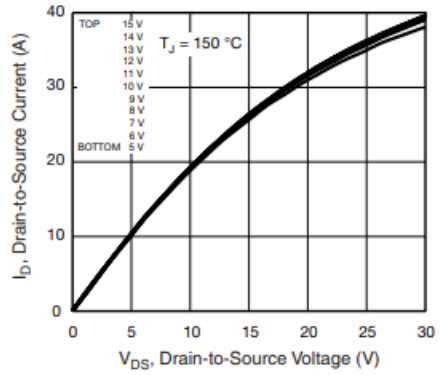


Fig. 2 - Typical Output Characteristics

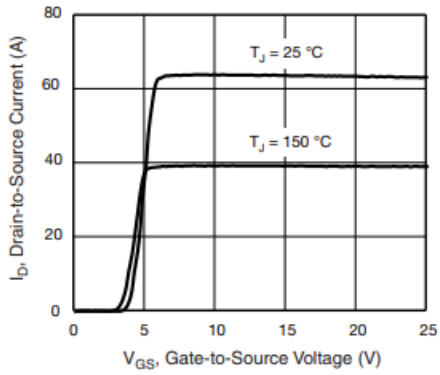


Fig. 3 - Typical Transfer Characteristics

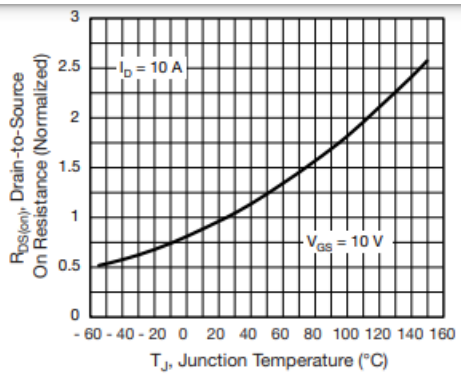


Fig. 4 - Normalized On-Resistance vs. Temperature

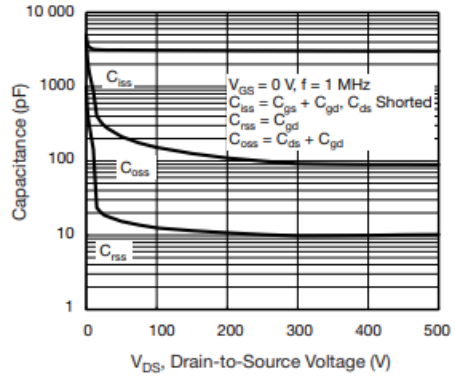


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

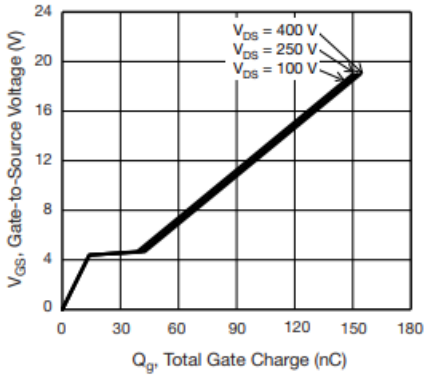


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

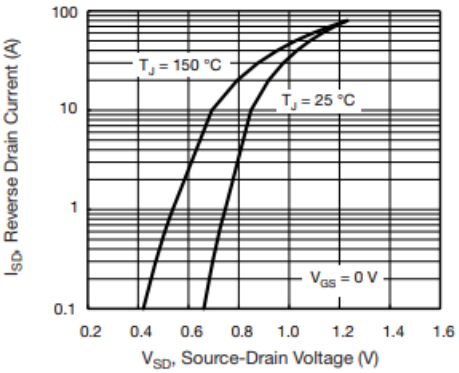


Fig. 7 - Typical Source-Drain Diode Forward Voltage

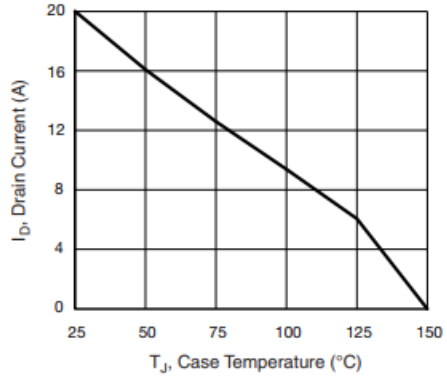


Fig. 9 - Maximum Drain Current vs. Case Temperature

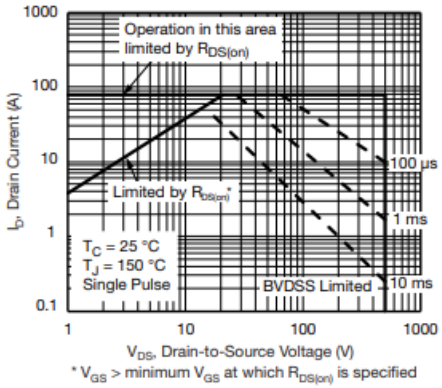


Fig. 8 - Maximum Safe Operating Area

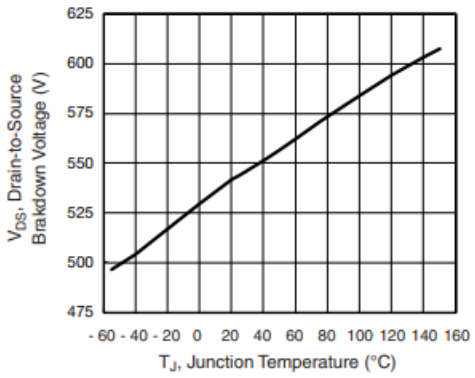


Fig. 10 - Temperature vs. Drain-to-Source Voltage

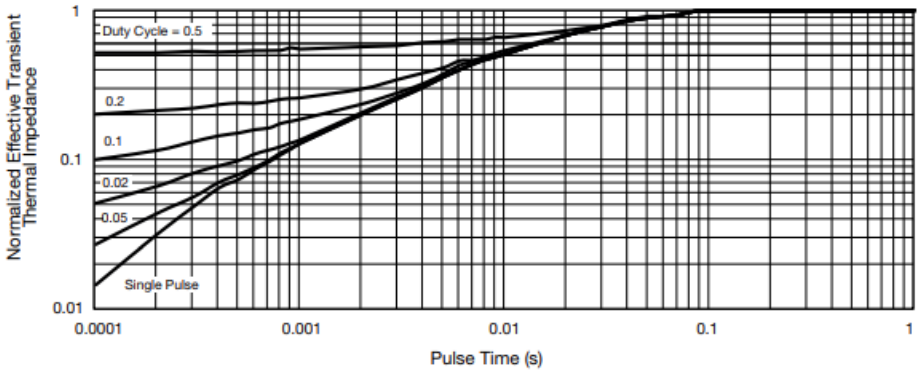


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

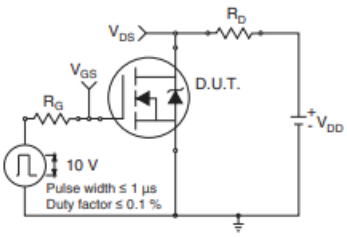


Fig. 12 - Switching Time Test Circuit

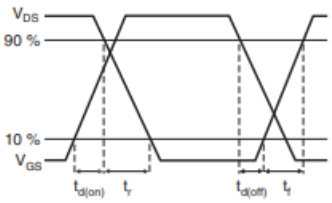


Fig. 13 - Switching Time Waveforms

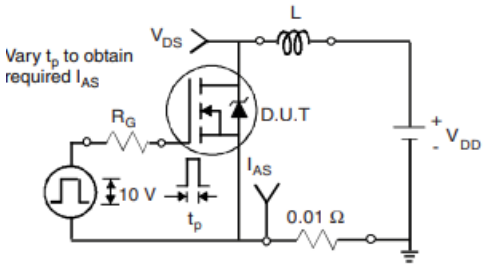


Fig. 14 - Unclamped Inductive Test Circuit

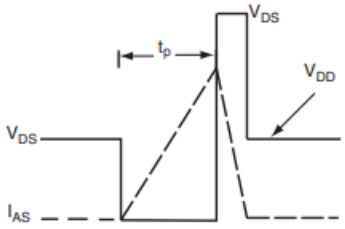


Fig. 15 - Unclamped Inductive Waveforms

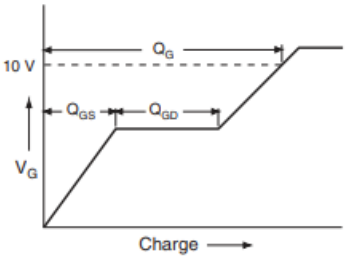


Fig. 16 - Basic Gate Charge Waveform

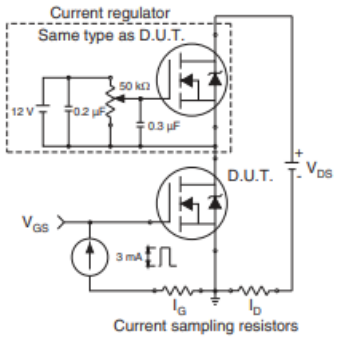


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

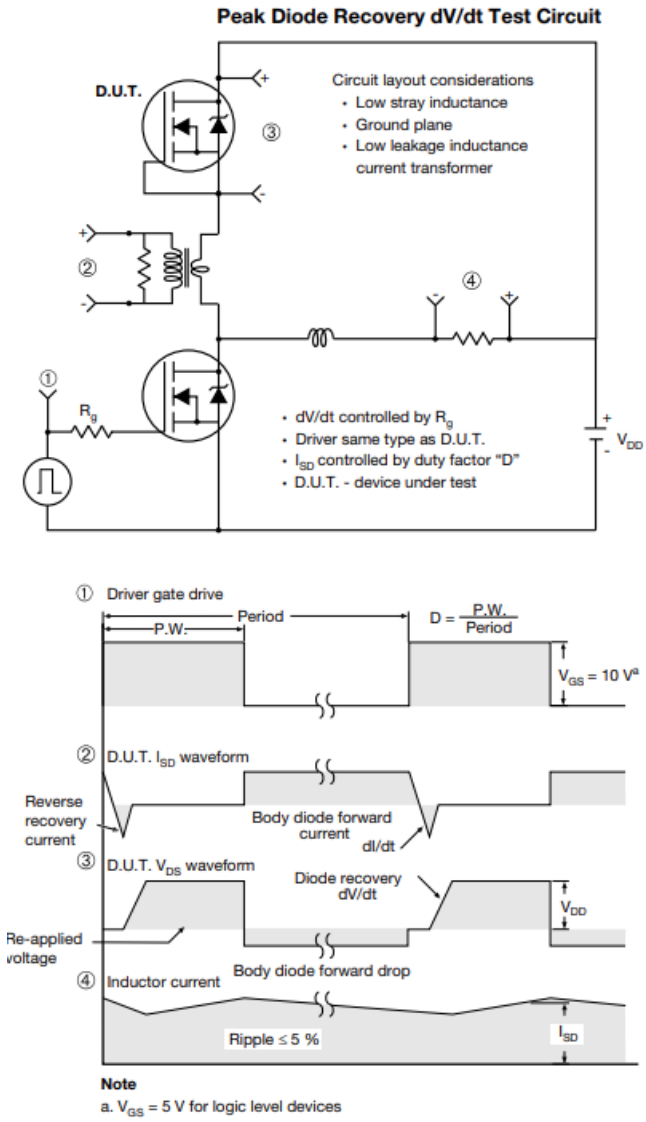
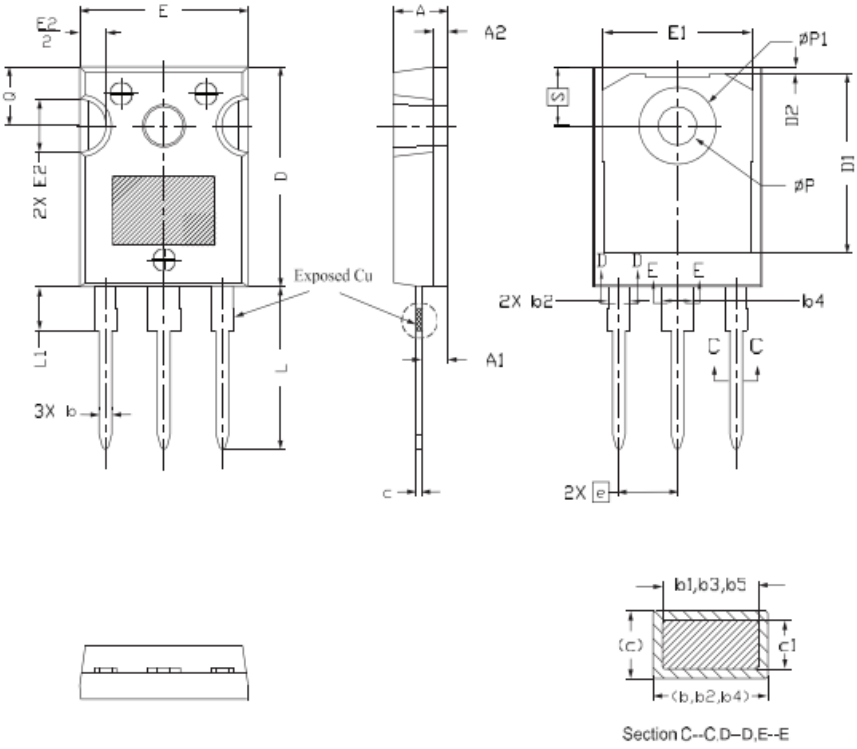


Fig. 18 - For N-Channel

TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9



Section C--C,D--D,E--E

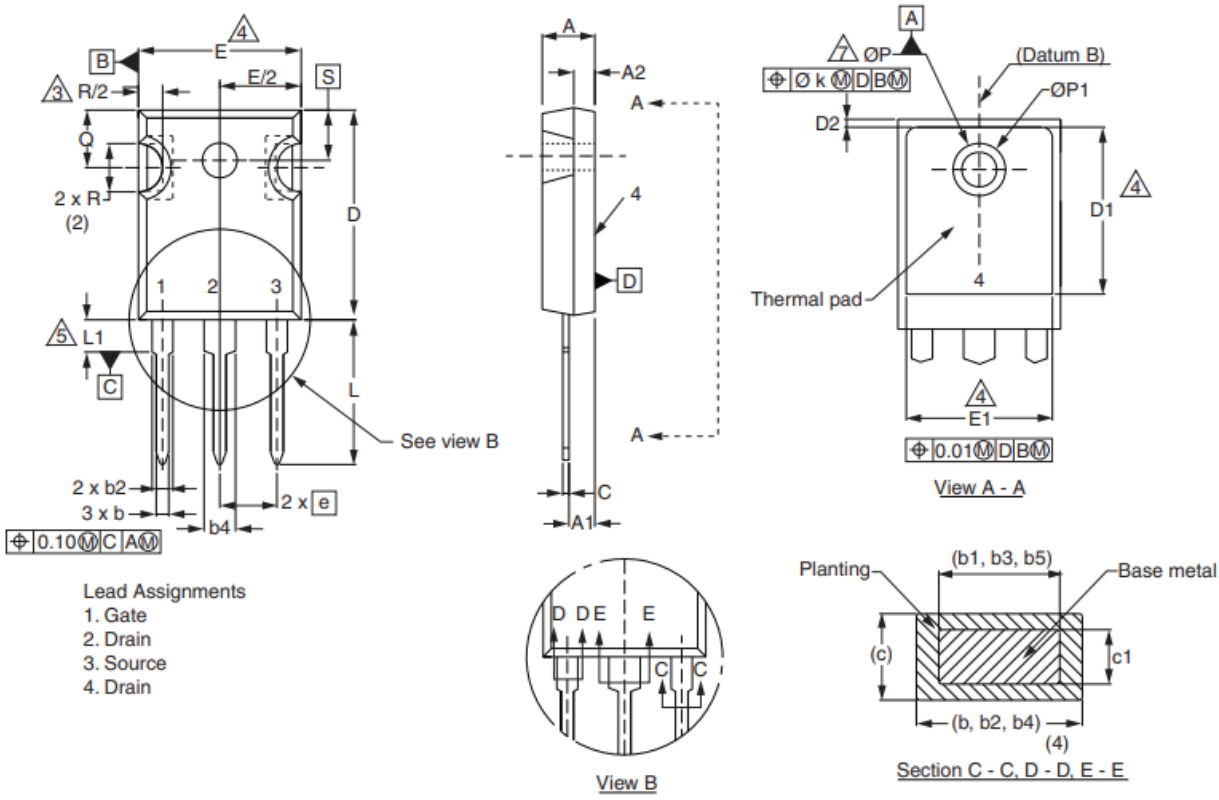
	MILLIMETERS			
DIM.	**MIN.**	**NOM.**	**MAX.**	**NOTES**
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

	MILLIMETERS			
DIM.	**MIN.**	**NOM.**	**MAX.**	**NOTES**
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

Notes

1. Package reference: JEDEC® TO247, variation AC
2. All dimensions are in mm
3. Slot required, notch may be rounded
4. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
5. Thermal pad contour optional with dimensions D1 and E1
6. Lead finish uncontrolled in L1
7. Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
8. Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

VERSION 2: FACILITY CODE = Y



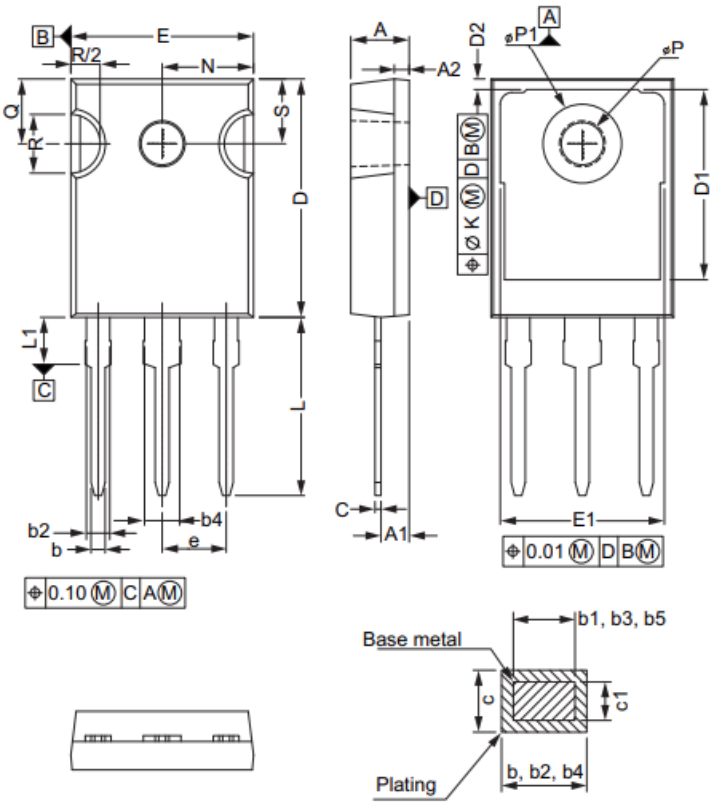
	MILLIMETERS		
DIM.	**MIN.**	**MAX.**	**NOTES**
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	–	

	MILLIMETERS		
DIM.	**MIN.**	**MAX.**	**NOTES**
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	–	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	–	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Contour of slot optional
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005″) per side. These dimensions are measured at the outermost extremes of the plastic body
4. Thermal pad contour optional with dimensions D1 and E1
5. Lead finish uncontrolled in L1
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154″)
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c

VERSION 3: FACILITY CODE = N



	MILLIMETERS				MILLIMETERS	
DIM.	**MIN.**	**MAX.**		**DIM.**	**MIN.**	**MAX.**
A	4.65	5.31		D2	0.51	1.35
A1	2.21	2.59		E	15.29	15.87
A2	1.17	1.37		E1	13.46	–
b	0.99	1.40		e	5.46 BSC	
b1	0.99	1.35		k	0.254	
b2	1.65	2.39		L	14.20	16.10
b3	1.65	2.34		L1	3.71	4.29
b4	2.59	3.43		N	7.62 BSC	
b5	2.59	3.38		P	3.56	3.66
c	0.38	0.89		P1	–	7.39
c1	0.38	0.84		Q	5.31	5.69
D	19.71	20.70		R	4.52	5.49
D1	13.08	–		S	5.51 BSC	
ECN: E22-0452-Rev. G, 31-Oct-2022 DWG: 5971						

Notes

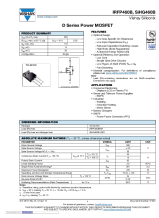
1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Contour of slot optional

3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005″) per side. These dimensions are measured at the outermost extremes of the plastic body
4. Thermal pad contour optional with dimensions D1 and E1
5. Lead finish uncontrolled in L1
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154″)

Disclaimer

For technical questions, contact: hvm@vishay.com

Documents / Resources

	VISHAY IRFP460B D Series Power MOSFET [pdf] User Manual IRFP460B D Series Power MOSFET, IRFP460B, D Series Power MOSFET, Power MOSFET, MOSFET

References

- Vishay Intertechnology: Passives & Discrete Semiconductors
- vishay.com/doc?91000
- vishay.com/doc?99912
- IRFP460B, SiHG460B MOSFETs | Vishay
- User Manual