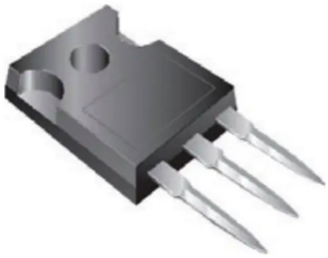
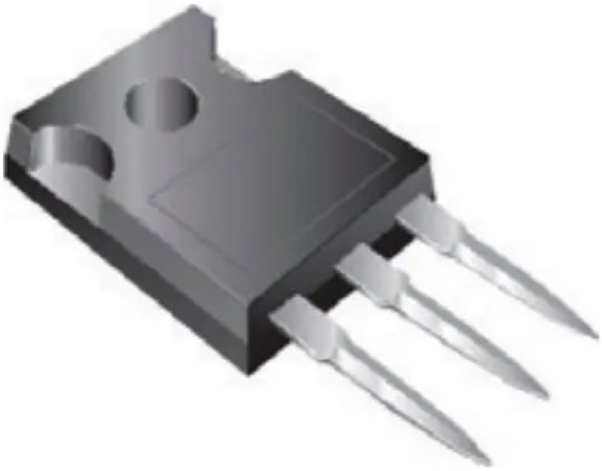


VISHAY IRFP360 Siliconix Power Mosfet Owner's Manual

VISHAY IRFP360 Siliconix Power Mosfet Owner's Manual

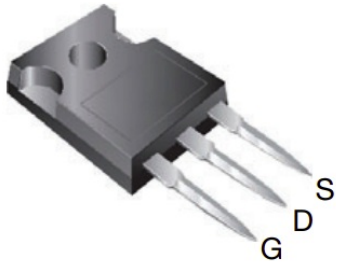


Contents

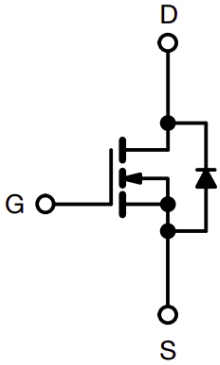
Product Information

Power MOSFET

TO-247AC



N-Channel MOSFET



PRODUCT SUMMARY		
V_{DS} (V)	400	
RDS(on) (W)	V_{GS} = 10 V	0.20
Q_g (max.) (nC)	210	
Q_{gs} (nC)	30	
Q_{gd} (nC)	110	
Configuration	Single	

FEATURES

Available

RoHS*

Available

- Dynamic dV/dt rated
- Repetitive avalanche rated
- Isolated central mounting hole
- Fast switching
- Ease of paralleling
- Simple drive requirements
- **Material categorization:** for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-

compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant.
Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The
TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFP360PbF

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

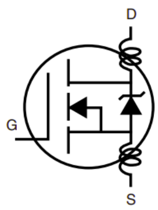
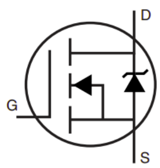
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-source voltage			VDS	400	V
Gate-source voltage			VGS	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	23	A
		T_C = 100 °C		14	
Pulsed drain currenta			IDM	92	
Linear derating factor				2.2	W/°C
Single pulse avalanche energy b			EAS	1200	mJ
Repetitive avalanche current a			IAR	23	A
Repetitive avalanche energy a			EAR	28	mJ
Maximum power dissipation	T_C = 25 °C		P_D	280	W
Peak diode recovery dV/dt c			dV/dt	4.0	V/ns
Operating junction and storage temperature range			TJ, Tstg	-55 to +150	°C
Soldering recommendations (peak temperature)	for 10 s			300d	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. VDD = 50 V, starting TJ = 25 °C, L = 4.0 mH, Rg = 25 Ω, IAS = 23 A (see fig. 12)
c. ISD ≤ 23 A, dI/dt ≤ 170 A/μs, VDD ≤ VDS, TJ ≤ 150 °C
d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	RthJA	–	40	°C/W
Case-to-sink, flat, greased surface	RthCS	0.24	–	
Maximum junction-to-case (drain)	RthJC	–	0.45	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	VDS	V_{GS} = 0 V, I_D = 250 μA		400	–	–	V
V_{DS} temperature coefficient	DV DS/ T_J	Reference to 25 °C, I_D = 1 mA		–	0.56	–	V/°C
Gate-source threshold voltage	VGS(th)	V_{DS} = V_{GS}, I_D = 250 μA		2.0	–	4.0	V
Gate-source leakage	IGSS	V_{GS} = ± 20 V		–	–	± 100	nA
Zero gate voltage drain current	IDSS	V_{DS} = 400 V, V_{GS} = 0 V		–	–	25	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125 °C		–	–	250	
Drain-source on-state resistance	RDS(on)	V_{GS} = 10 V	I_D = 14 A b	–	–	0.20	W
Forward transconductance	gfs	V_{DS} = 50 V, I_D = 14 A b		14	–	–	S
Dynamic							
Input capacitance	Ciss			–	4500	–	

Output capacitance	C_{oss}	V_{GS} = 0 V, V_{DS} = 25 V,f = 1.0 MHz, see fig. 5	–	1100	–	pF
Reverse transfer capacitance	C_{rss}		–	490	–	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 23 A, V_{DS} = 320 V,see fig. 6 and 13 b	–	–	210	nC
Gate-source charge	Q_{gs}		–	–	30	
Gate-drain charge	Q_{gd}		–	–	110	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 200 V, I_D = 23 A ,R_g = 4.3 W, R_D = 8.3 W, see fig. 10 b	–	18	–	ns
Rise time	t_r		–	79	–	
Turn-off delay time	$t_{d(off)}$		–	100	–	
Fall time	t_f		–	67	–	
Internal drain inductance	L_D	Between lead,6 mm (0.25″) from package and center of die contact 	–	5.0	–	nH
Internal source inductance	L_S		–	13	–	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral; reversep – n junction diode 	–	–	23	A
Pulsed diode forward current a	I_{SM}		–	–	92	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 23 A, V_{GS} = 0 V b	–	–	1.8	V
Body diode reverse recovery time	trr	T_J = 25 °C, I_F = 23 A, dI/dt = 100 A/μs b	–	420	630	ns
Body diode reverse recovery charge	Q_{rr}		–	5.6	8.4	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

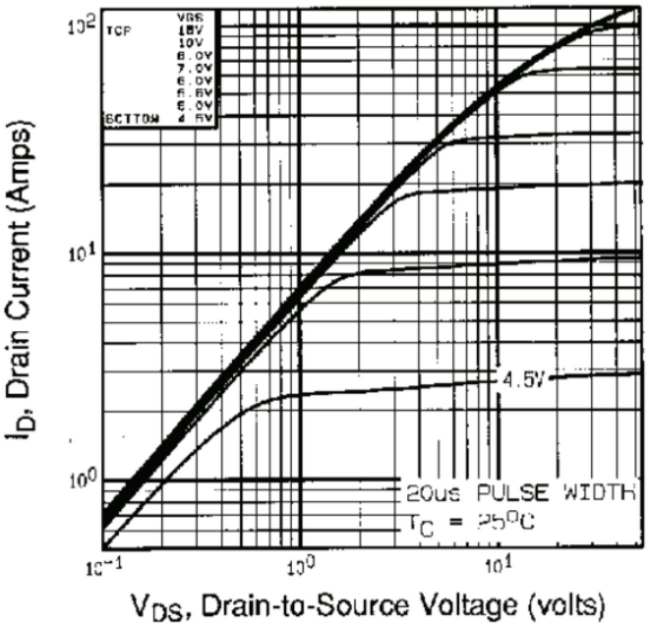
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

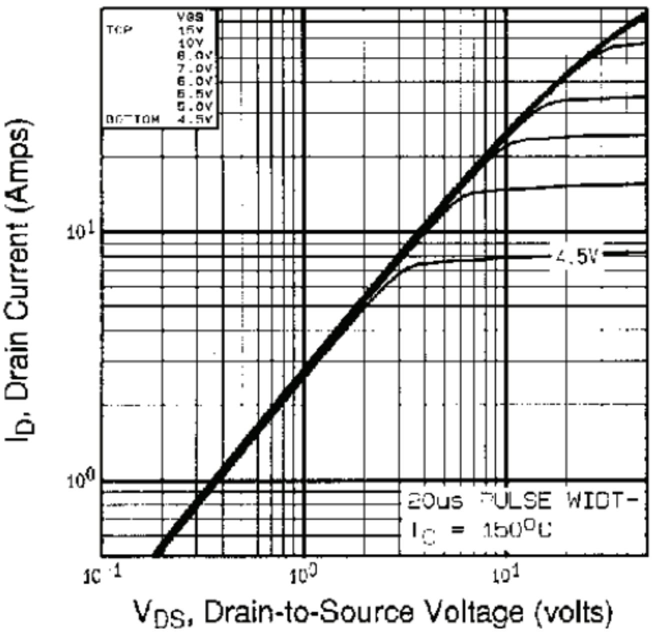
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

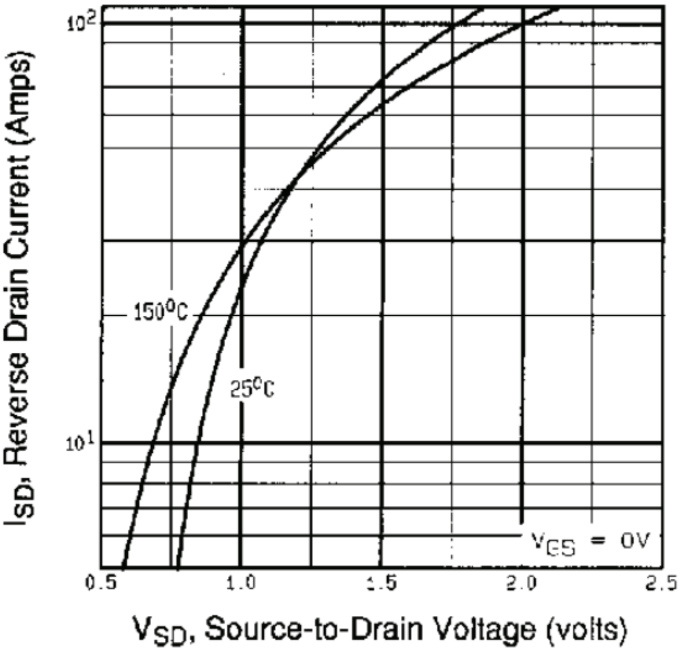
1. **Fig. 1 – Typical Output Characteristics, TC = 25 °C**



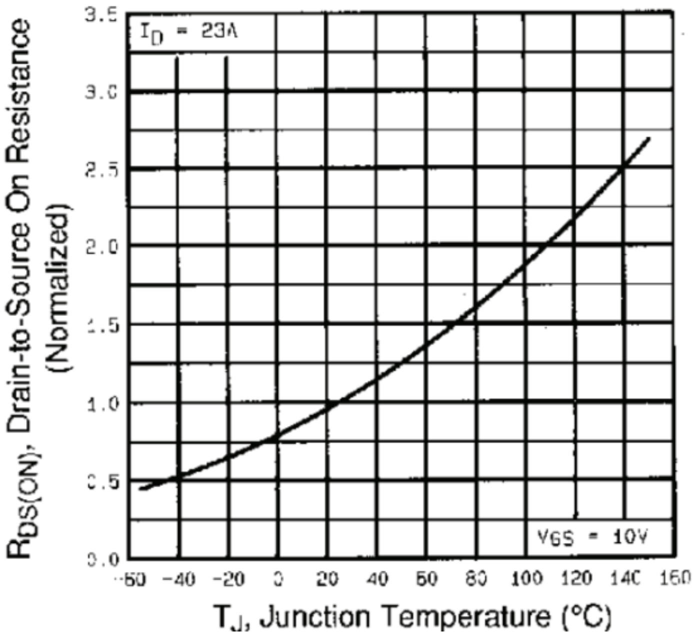
2. **Fig. 2 – Typical Output Characteristics, TC = 150 °C**



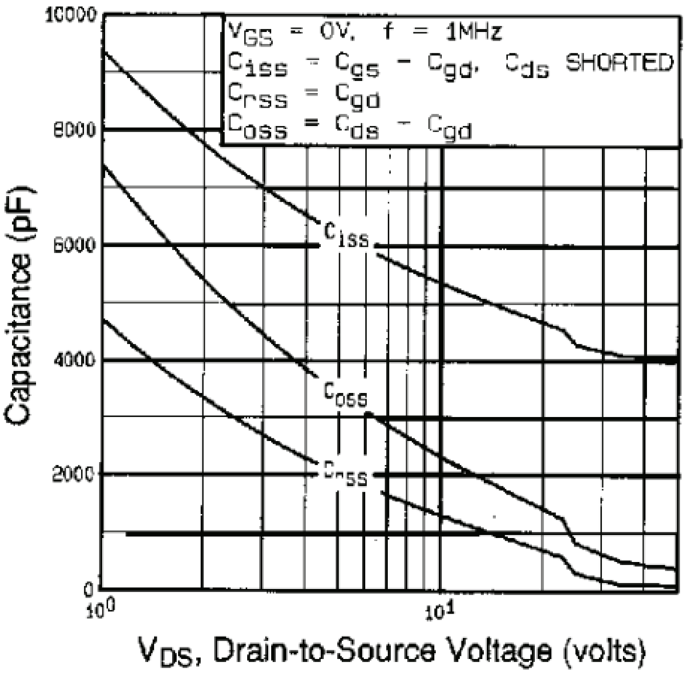
3. **Fig. 3 – Typical Transfer Characteristics**



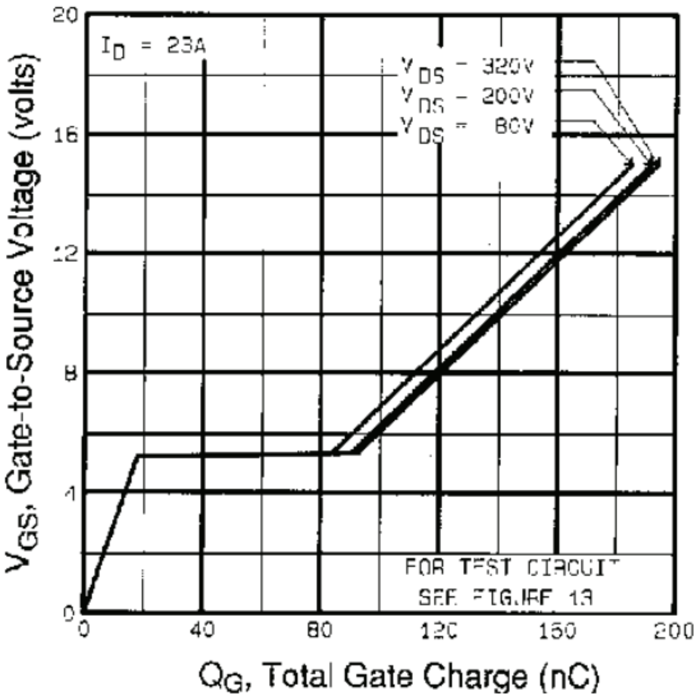
4. **Fig. 4 – Normalized On-Resistance vs. Temperature**



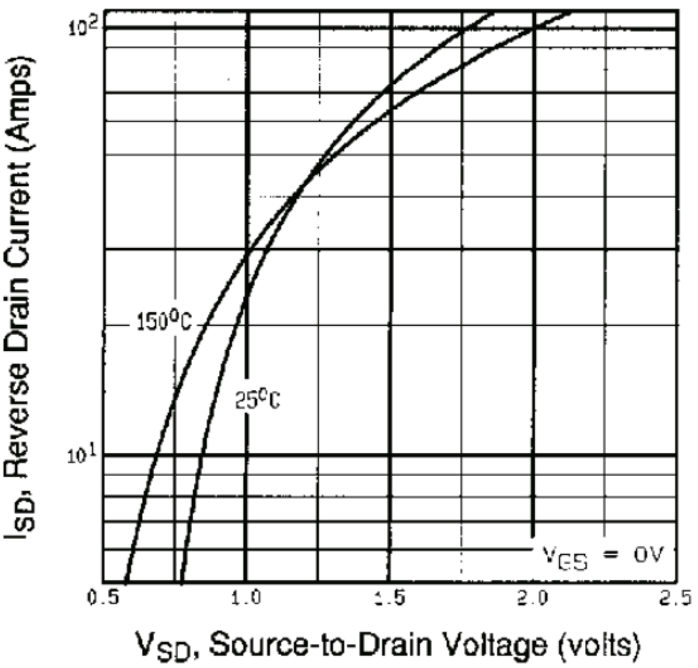
5. **Fig. 5 – Typical Capacitance vs. Drain-to-Source Voltage**



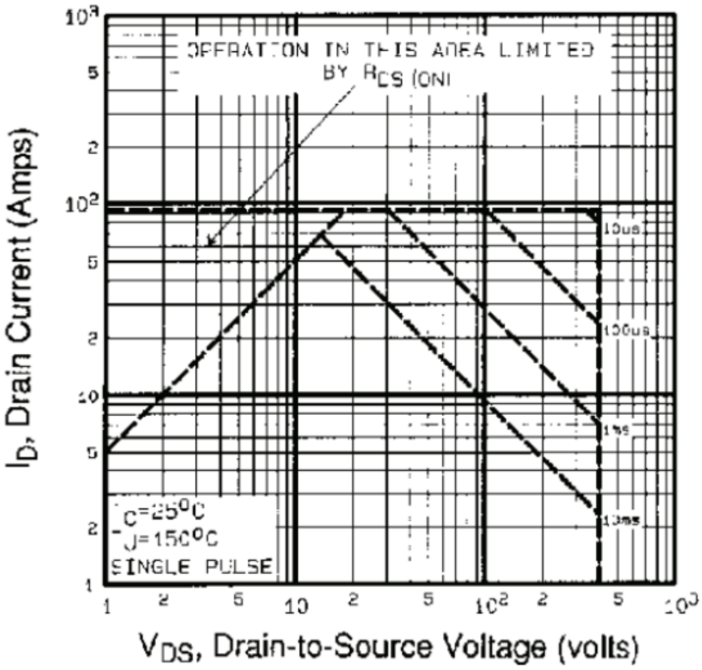
6. **Fig. 6 – Typical Gate Charge vs. Gate-to-Source Voltage**



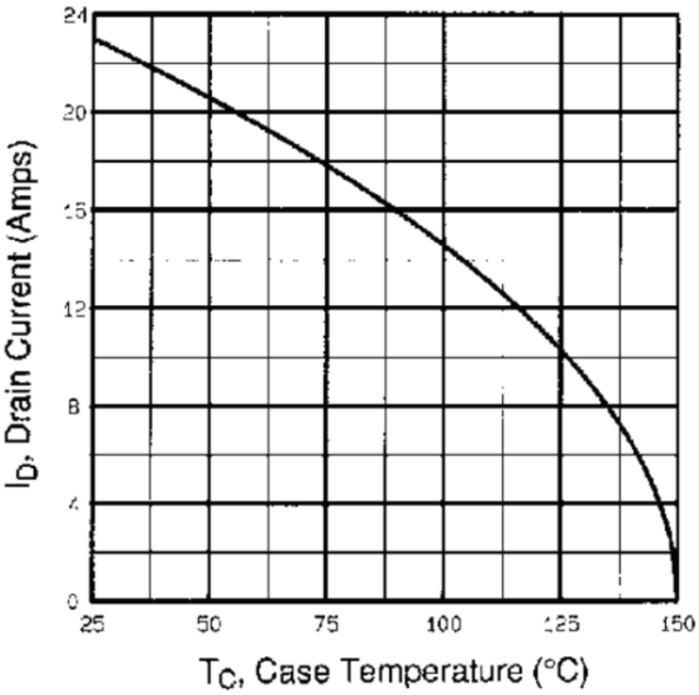
7. **Fig. 7 – Typical Source-Drain Diode Forward Voltage**



8. **Fig. 8 – Maximum Safe Operating Area**



9. **Fig. 9 – Maximum Drain Current vs. Case Temperature**



10. **Fig. 10a – Switching Time Test Circuit**

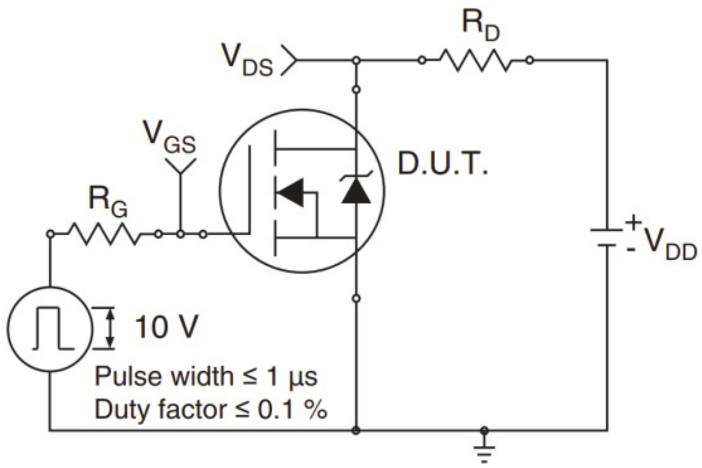
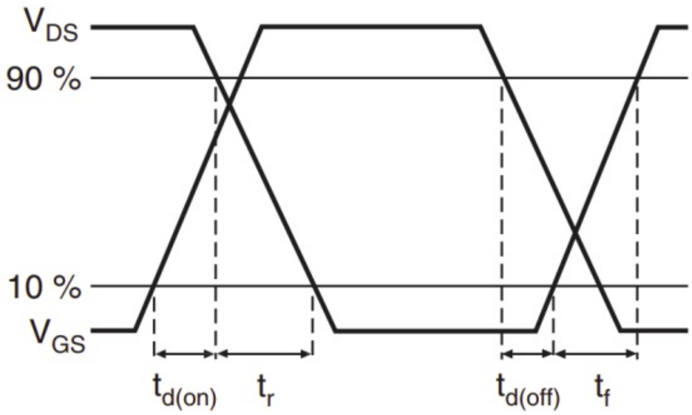
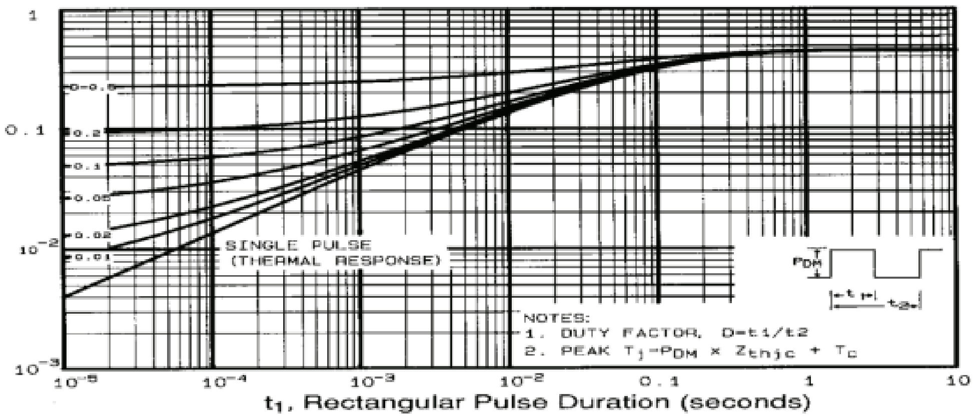


Fig. 10b – Switching Time Waveforms



11. **Fig. 11 – Maximum Effective Transient Thermal Impedance, Junction-to-Case**



12. **Fig. 12a – Unclamped Inductive Test Circuit**

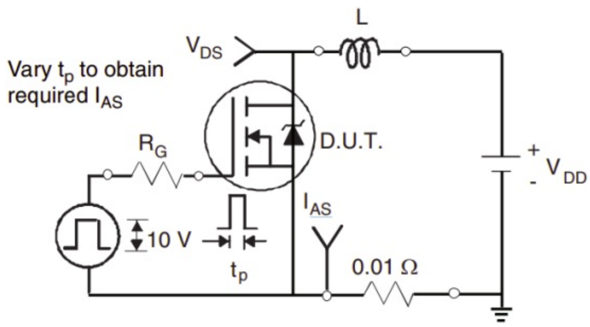


Fig. 12b – Unclamped Inductive Waveforms

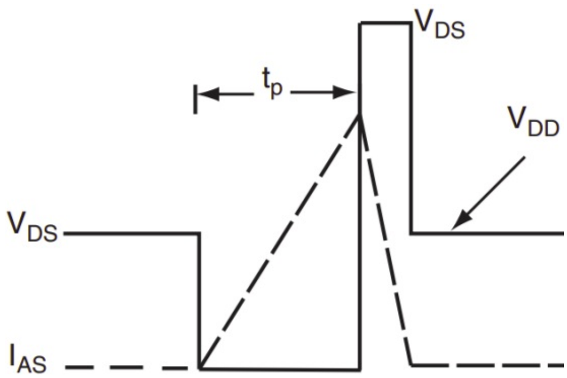
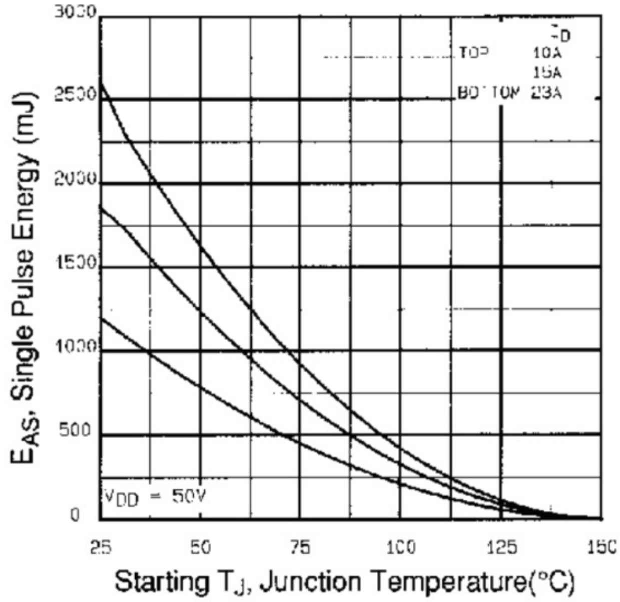


Fig. 12c – Maximum Avalanche Energy vs. Drain Current



13. **Fig. 13a – Basic Gate Charge Waveform**

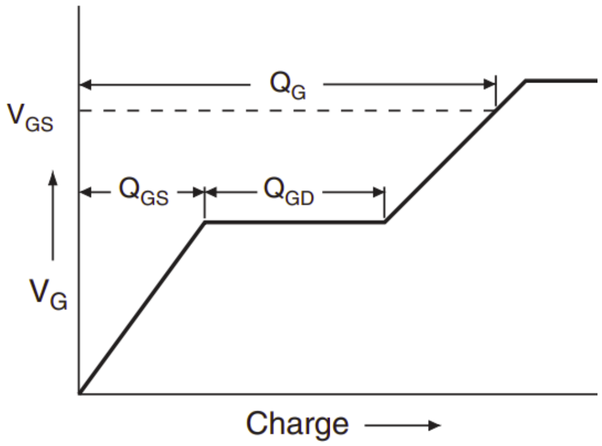
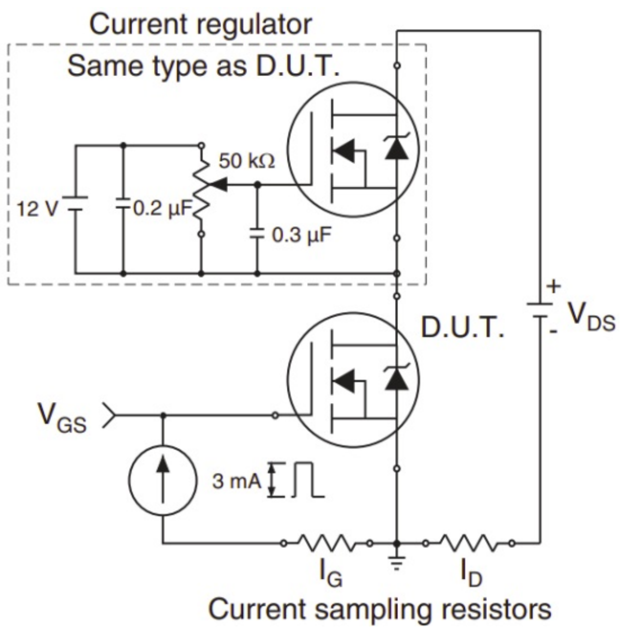
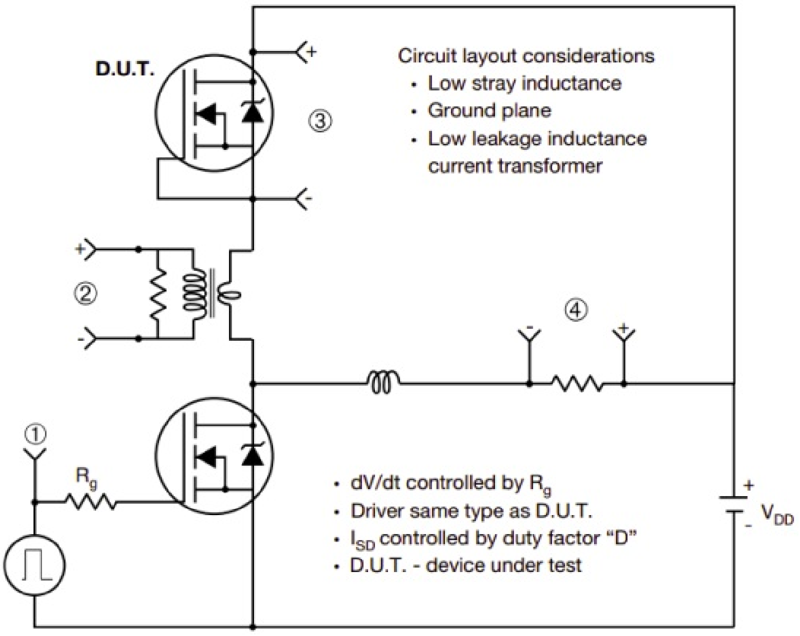


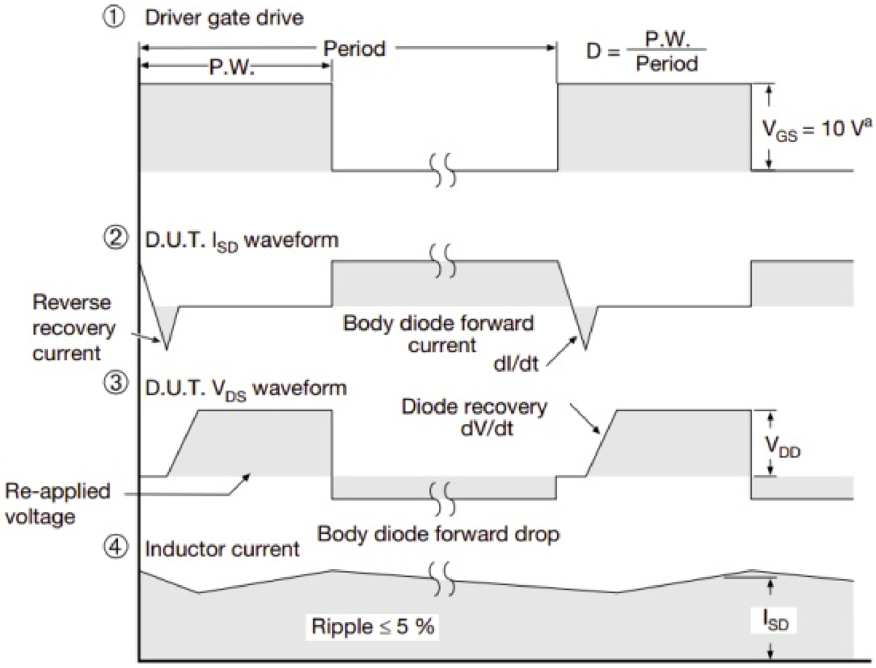
Fig. 13b – Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



14. **Fig. 14 – For N-Channel**

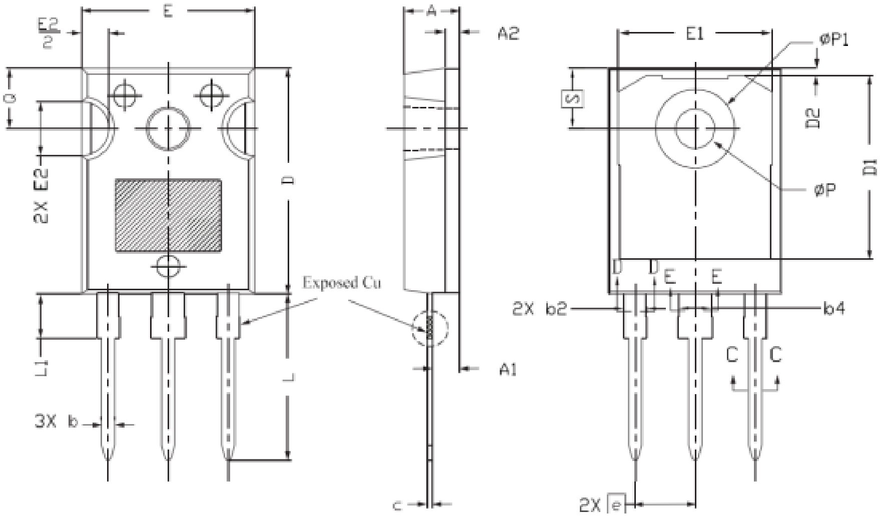


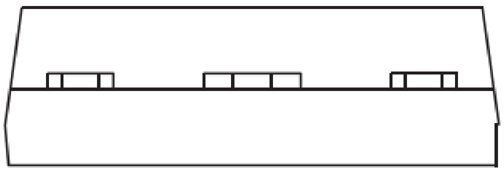
Note

a. VGS = 5 V for logic level devices

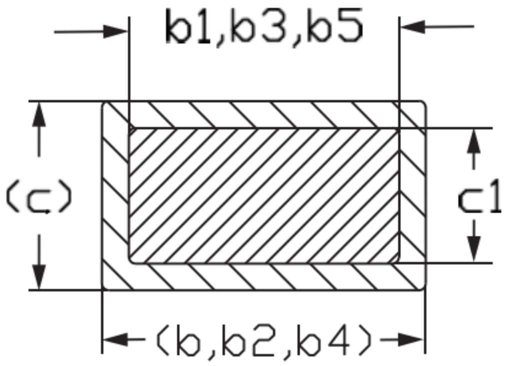
TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9





	MILLIMETERS			
DIM.	**MIN.**	**NOM.**	**MAX.**	**NOTES**
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4



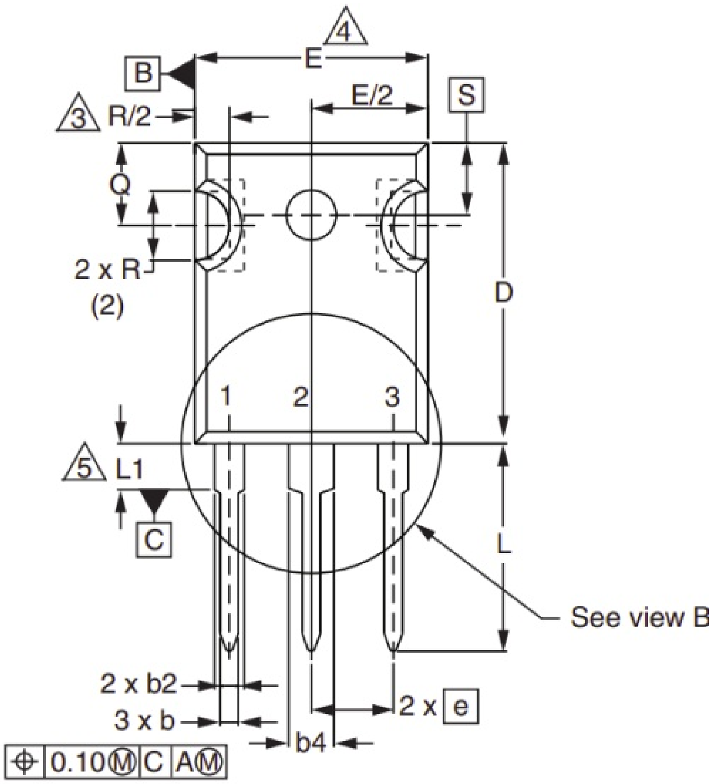
Section C--C,D--D,E--E

	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

Notes

1. **Package reference:** JEDEC® TO247, variation AC
2. All dimensions are in mm
3. Slot required, notch may be rounded
4. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
5. Thermal pad contour optional with dimensions D1 and E1
6. Lead finish uncontrolled in L1
7. Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
8. Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

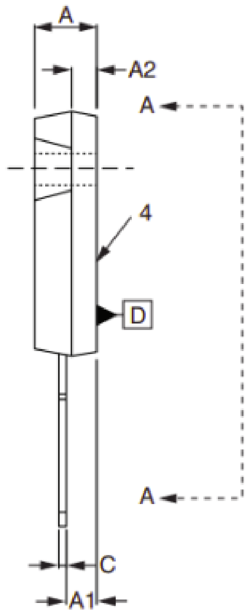
VERSION 2: FACILITY CODE = Y

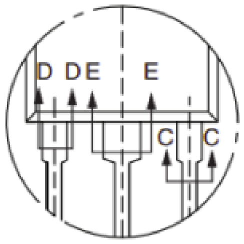


Lead Assignments

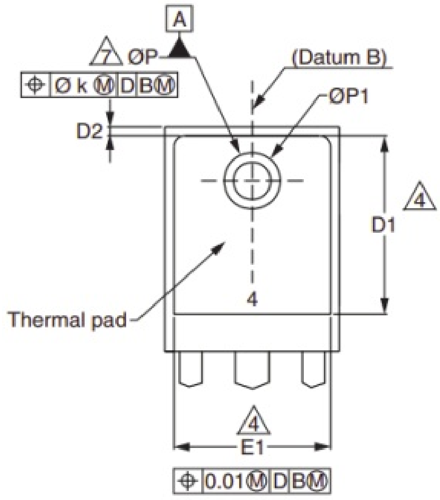
1. Gate
2. Drain
3. Source
4. Drain

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	–	

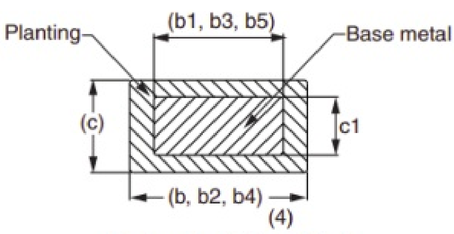




View B



View A - A



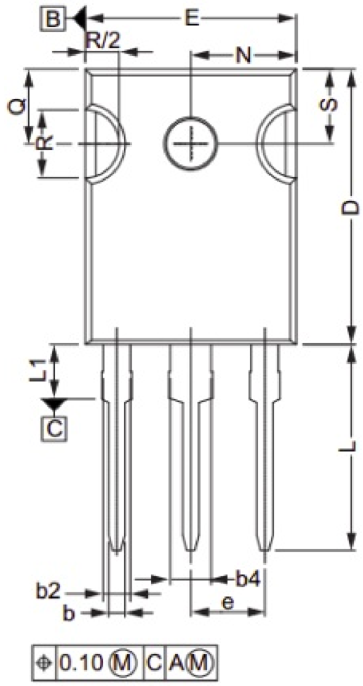
Section C - C, D - D, E - E

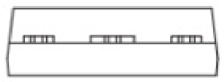
	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	–	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	–	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

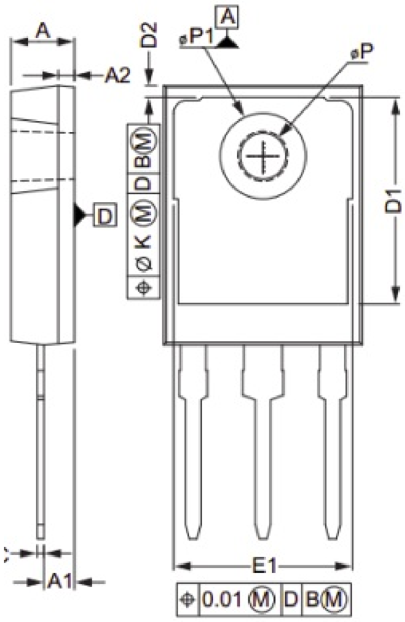
1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Contour of slot optional
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005″) per side. These dimensions are measured at the outermost extremes of the plastic body
4. Thermal pad contour optional with dimensions D1 and E1
5. Lead finish uncontrolled in L1
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154″)
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c

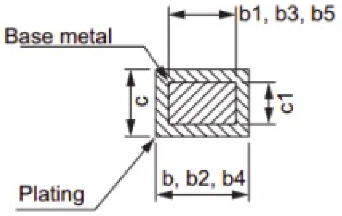
VERSION 3: FACILITY CODE = N





	MILLIMETERS	
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	–





	MILLIMETERS	
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	–
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	–	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022
DWG: 5971

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Contour of slot optional
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005″) per side. These dimensions are measured at the outermost extremes of the plastic body
4. Thermal pad contour optional with dimensions D1 and E1
5. Lead finish uncontrolled in L1
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154″)

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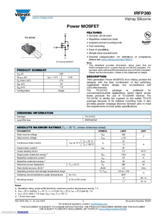
Documents / Resources

	VISHAY IRFP360 Siliconix Power Mosfet [pdf] Owner's Manual IRFP360PBF, IRFP360 Siliconix Power Mosfet, IRFP360, Siliconix Power Mosfet, Power Mosfet, Mosfet

References

- Vishay Intertechnology: Passives & Discrete Semiconductors
- User Manual