

# **VISHAY IRF9640 Channel MOSFET Transistor Instructions**

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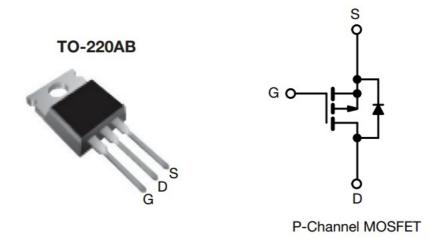
## **VISHAY IRF9640 Channel MOSFET Transistor**



## **FEATURES**

- Dynamic dV/dt rating
- · Repetitive avalanche rated
- P-channel

- · Fast switching
- · Ease of paralleling
- · Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	-200			
RDS(on) (W)	V <sub>GS</sub> = -10 V	0.50		
Q <sub>g</sub> max. (nC)	44			
Q <sub>gs</sub> (nC)	7.1			
Q <sub>gd</sub> (nC)	27			
Configuration	Single			

### Note

This datasheet provides information about parts that are RoHS-compliant and/or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant.

Please see the information/tables in this datasheet for details

### **DESCRIPTION**

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching,ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION				
Package	TO-220AB			
Lead (Pb)-free	IRF9640PbF			
Lead (Pb)-free and halogen-free	IRF9640PbF-BE3			

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 2	25 °C, unless	sotherwise	noted)		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			VDS	-200	V
Gate-source voltage			VGS	± 20	V
Continuous drain current	V <sub>GS</sub> at 10	T <sub>C</sub> = 25 °	- I <sub>D</sub>	-11	
Continuous drain current	V	T <sub>C</sub> = 100 °C		-6.8	A
Pulsed drain current a			IDM	-44	
Linear derating factor				1.0	W/°C
Single pulse avalanche energy b			EAS	700	mJ
Repetitive avalanche current a			IAR	-11	А
Repetitive avalanche energy a			EAR	13	mJ
Maximum power dissipation $T_C = 25  ^{\circ}C$			P <sub>D</sub>	125	W
Peak diode recovery dV/dt c			dV/dt	-5.0	V/ns
Operating junction and storage temperature range			TJ, Tstg	-55 to +150	
Soldering recommendations (peak tempe rature) d	For 10 s			300	°C
Mounting torque	6-32 or M3 screw			10	lbf · in
Mounting torque				1.1	N · m

## **Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- VDD = -50 V, starting TJ = 25 °C, L = 8.7 mH, Rg = 25  $\Omega$ , IAS = -11 A (see fig. 12)
- ISD  $\leq$  -11 A, dI/dt  $\leq$  150 A/ $\mu$ s, VDD  $\leq$  VDS, TJ  $\leq$  150 °C
- 1.6 mm from case

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	RthJA	_	62		
Case-to-sink, flat, greased surfac e	RthCS	0.50	-	°C/W	
Maximum junction-to-case (drain)	RthJC	_	1.0		

## **SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX	UNI T
Static	I				1		
Drain-source breakdown voltage	VDS	V <sub>GS</sub> = 0 V,	I <sub>D</sub> = -250 μA	-200	_	_	V
V <sub>DS</sub> temperature coefficient	DV <sub>DS</sub> /T <sub>J</sub>	Reference	to 25 °C, I <sub>D</sub> = -1 mA	_	-0.2	_	V/°C
Gate-source threshold voltage	VGS(th)	$V_{DS} = V_{GS}$	I <sub>D</sub> = -250 μA	-2.0	_	-4.0	٧
Gate-source leakage	IGSS	V <sub>GS</sub> = ± 20	V	_	_	± 10	nA
		V <sub>DS</sub> = -200	V <sub>DS</sub> = -200 V, V <sub>GS</sub> = 0 V		_	-100	
Zero gate voltage drain current	IDSS	V <sub>DS</sub> = -160 5 °C	V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 12	_	_	-500	μΑ
Drain-source on-state resistance	RDS(on)	V <sub>GS</sub> = -10	I <sub>D</sub> = -6.6 A b	_	_	0.50	W
Forward transconductance	gfs	V <sub>DS</sub> = -50 V, I <sub>D</sub> = -6.6 A b		4.1	_	_	S
Dynamic					•		
Input capacitance	Ciss	$V_{GS} = 0 \text{ V}, V_{DS} = -25 \text{ V},$		_	1200	_	pF
Output capacitance	Coss		f = 1.0 MHz, see fig. 5		370	_	
Reverse transfer capacitance	Crss		, 0	_	81	_	'
Total gate charge	Qg			_	_	44	
Gate-source charge	Qgs	$V_{GS} = -10$ $I_D = -11 \text{ A, } V_{DS} = -1$ $60 \text{ V.}$		_	_	7.1	
Gate-drain charge	Qgd	VGS = -10	60 V, see fig. 6 and 13 b	_	_	27	nC
Turn-on delay time	td(on)			_	14	_	
Rise time	t <sub>r</sub>	V <sub>DD</sub> = -100 V, I <sub>D</sub> = -11 A		_	43	_	ns
Turn-off delay time	td(off)	0	$R_g = 9.1 \text{ W}, R_D = 8.6 \text{ W}, \text{ see fig.}$ 10 b		39	_	
Fall time	t <sub>f</sub>	10 b			38	_	
Gate input resistance	L <sub>D</sub>		D	_	4.5	_	
Internal drain inductance	Ls	G		_	7.5	_	nH
Internal source inductance	R <sub>g</sub>	f = 1 MHz, o	0.3	_	1.7	W	

Continuous source-drain diode c urrent	I <sub>S</sub>		_	_	-11	
Pulsed diode forward current a	ISM	G S S	-	_	-44	Α
Body diode voltage	VSD	$T_J = 25  ^{\circ}\text{C},  I_S = -11  \text{A},  V_{GS} = 0  \text{V}$ b	_	_	-5	V
Body diode reverse recovery tim e	trr	T <sub>J</sub> = 25 °C, I <sub>F</sub> = -11 A, dI/dt = 100 A/μs b	_	250	300	ns
Body diode reverse recovery cha rge	Qrr		-	2.9	3.6	μC
Forward turn-on time	ton	Intrinsic turn-on time is negligible ( and $L_{\text{D}}$ )	(turn-on	is domi	nated b	y L <sub>S</sub>

## **Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width  $\leq$  300  $\mu$ s; duty cycle  $\leq$  2 %

## **TYPICAL CHARACTERISTICS**

(25 °C, unless otherwise noted)

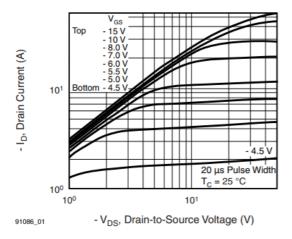


Fig. 1 - Typical Output Characteristics,  $T_C = 25$  °C

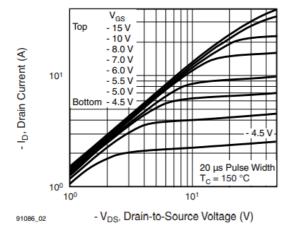


Fig. 2 - Typical Output Characteristics,  $T_C$  = 150 °C

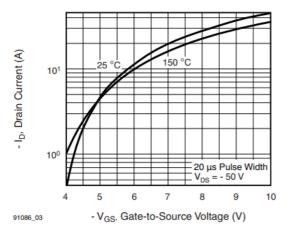


Fig. 3 - Typical Transfer Characteristics

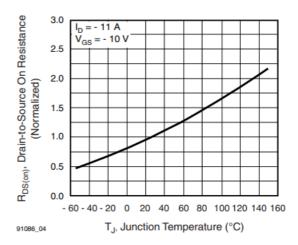


Fig. 4 - Normalized On-Resistance vs. Temperature

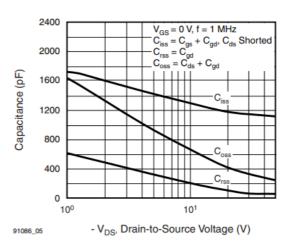


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

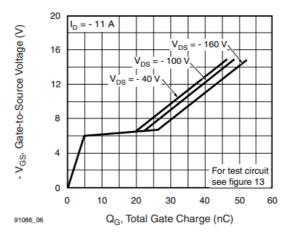


Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage

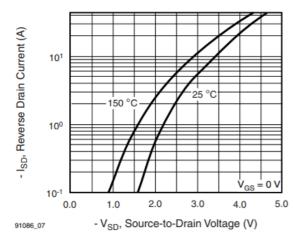


Fig. 7 - Typical Source-Drain Diode Forward Voltage

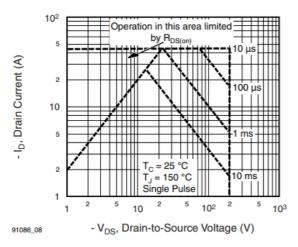


Fig. 8 - Maximum Safe Operating Area

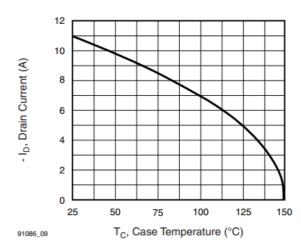


Fig. 9 - Maximum Drain Current vs. Case Temperature

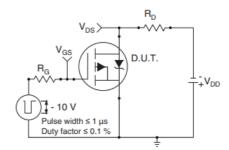


Fig. 10a - Switching Time Test Circuit

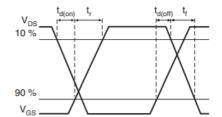


Fig. 10b - Switching Time Waveforms

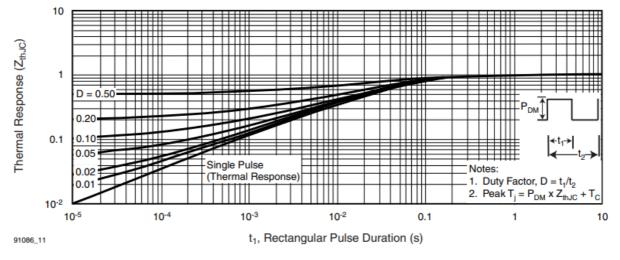
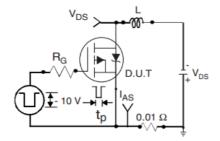


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



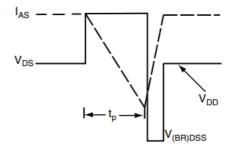


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

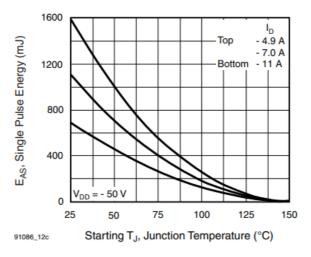


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

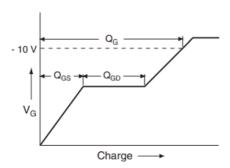


Fig. 13a - Basic Gate Charge Waveform

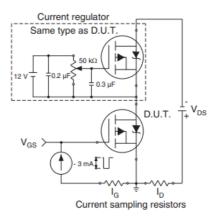
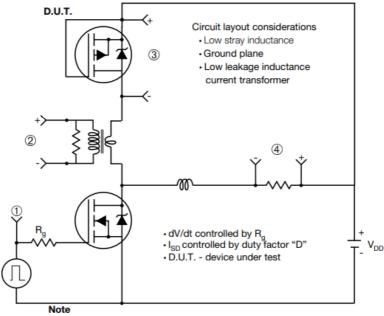


Fig. 13b - Gate Charge Test Circuit

#### Peak Diode Recovery dV/dt Test Circuit



· Compliment N-Channel of D.U.T. for driver

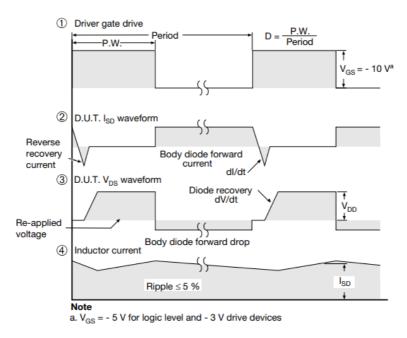


Fig. 14 - For P-Channel

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### **Documents / Resources**



VISHAY IRF9640 Channel MOSFET Transistor [pdf] Instructions

IRF9640 Channel MOSFET Transistor, IRF9640, Channel MOSFET Transistor, MOSFET Transistor, Transistor

### References

- Vishay Intertechnology: Passives & Discrete Semiconductors
- User Manual

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