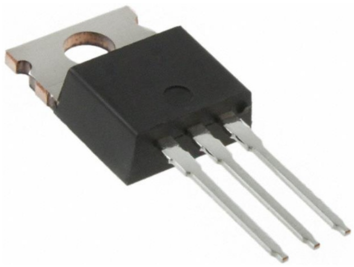
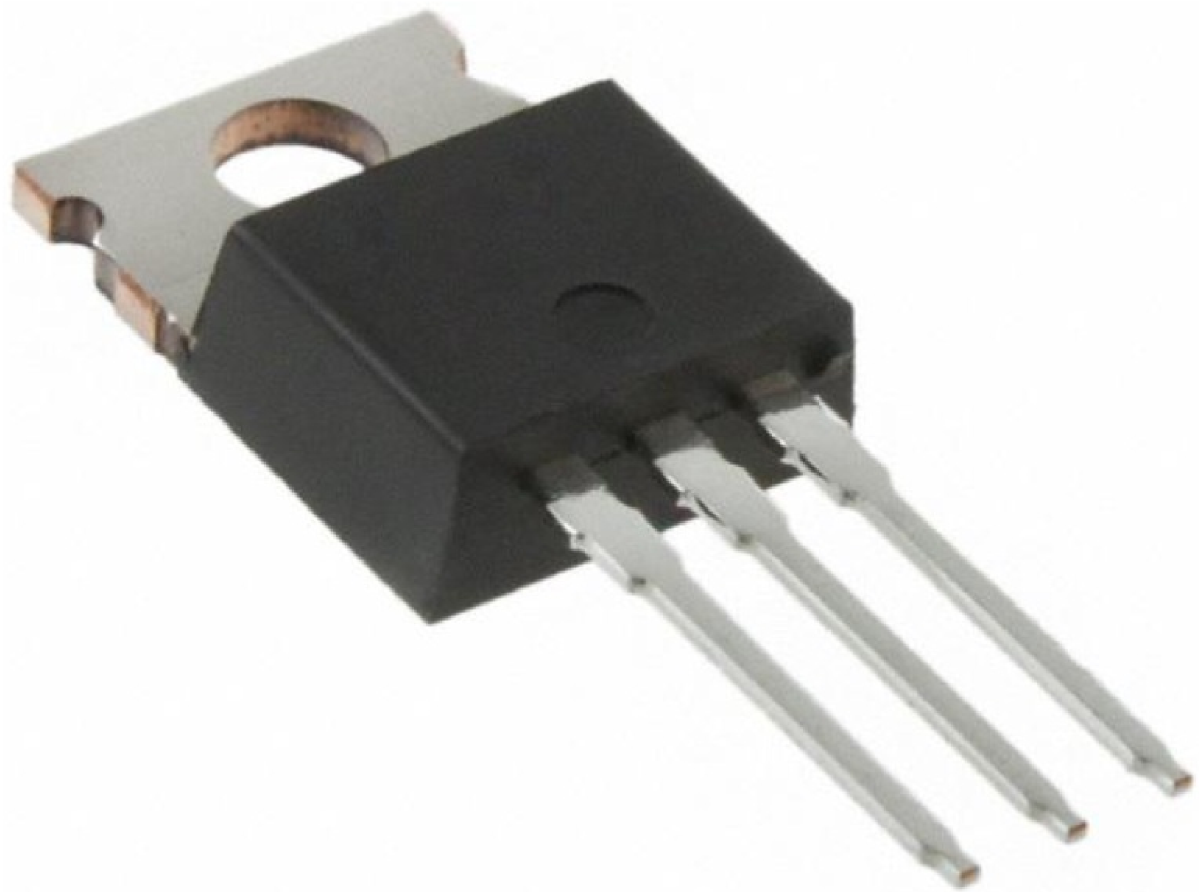


VISHAY IRF9610 Siliconix Instructions

VISHAY IRF9610 Siliconix Instructions



Contents

PRODUCT SUMMARY

V_{DS} (V)	-200	
RDS(on) (L)	V_{GS} = -10 V	3.0
Q_g max. (nC)	11	
Q_{gs} (nC)	7.0	
Q_{gd} (nC)	4.0	
Configuration	Single	

FEATURES

- Dynamic dV/dt rating
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

- This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

The power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness. The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9610PbF
Lead (Pb)-free and halogen-free	IRF9610PbF-BE3

ABSOLUTE MAXIMUM RATINGS

(S (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			VDS	-200	V
Gate-source voltage			VGS	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	-1.8	A
		T_C = 100 °C		-1.0	
Pulsed drain current a			IDM	-7.0	
Linear derating factor				0.16	W/°C
Single pulse avalanche energy b			P_D	20	W
Repetitive avalanche current a			ILM	-7.0	A
Repetitive avalanche energy a			dV/dt	-5.0	V/ns
Maximum power dissipation	T_C = 25 °C		TJ, Tstg	-55 to +150	°C
Peak diode recovery dV/dt c				300	
Operating junction and storage temperature range				10	lbf · in
Soldering recommendations (peak temperature) d	For 10 s			1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)
- Not applicable

- ISD ≤ -1.8 A, dI/dt ≤ 70 A/μs, VDD ≤ VDS, TJ ≤ 150 °C
- 1.6 mm from cas

THERMAL RESISTANCE RATINGS

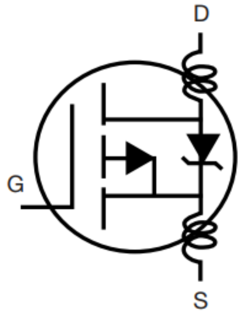
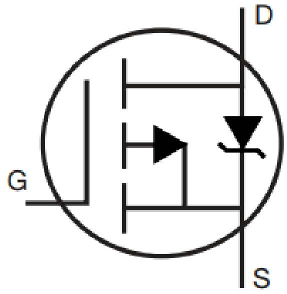
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	RthJA	–	62	°C/W
Case-to-sink, flat, greased surface	RthCS	0.50	–	
Maximum junction-to-case (drain)	RthJC	–	6.4	

SPECIFICATIONS

(TJ = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	VDS	V_{GS} = 0 V, I_D = -250 μA	-200	–	–	V
V_{DS} temperature coefficient	DV_{DS}/T_J	Reference to 25 °C, I_D = -1 mA	–	-0.23	–	V/°C
Gate-source threshold voltage	VGS(th)	V_{DS} = V_{GS}, I_D = -250 μA	-2.0	–	-4.0	V
Gate-source leakage	IGSS	V_{GS} = ± 20 V	–	–	± 100	nA
		V_{DS} = -200 V, V_{GS} = 0 V	–	–	-100	

Zero gate voltage drain current	IDSS	V_{DS} = -160 V, V_{GS} = 0 V, T_J = 125 °C		–	–	-500	µA
Drain-source on-state resistance	RDS(on)	V_{GS} = -10 V	I_D = -0.90 A b	–	–	3.0	L
Forward transconductance	gfs	V_{DS} = -50 V, I_D = -0.90 A b		0.90	–	–	S
Dynamic							
Input capacitance	Ciss	V_{GS} = 0 V, V_{DS} = -25 V,f = 1.0 MHz, see fig. 10		–	170	–	pF
Output capacitance	Coss			–	50	–	
Reverse transfer capacitance	Crss			–	15	–	
Total gate charge	Q_g	V_{GS} = -10 V	I_D = -3.5 A, V_{DS} = -160 V, see fig. 11 and 18 b	–	–	11	nC
Gate-source charge	Qgs			–	–	7.0	
Gate-drain charge	Qgd			–	–	4.0	
Turn-on delay time	td(on)	V_{DD} = -100 V, I_D = -0.90 A,R_g = 50 L, R_D = 110 L, see fig. 17 b		–	8.0	–	ns
Rise time	t_r			–	15	–	
Turn-off delay time	td(off)			–	10	–	

Fall time	t_f		–	8.0	–	
Gate input resistance	R_g	f = 1 MHz, open drain	2.5	–	14.3	L
Internal drain inductance	L_D	Between lead, D6 mm (0.25″) from package and center of Guidie contactS 	–	4.5	–	nH
Internal source inductance	L_S		–	7.5	–	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol  Showing the integral reverse G p – n junction diodeS	–	–	-1.8	A
Pulsed diode forward current a	ISM		–	–	-7.0	
Body diode voltage	VSD	T_J = 25 °C, I_S = -1.8 A, V_{GS} = 0 V b	–	–	-5.8	V

Body diode reverse recovery tim e	trr	T_J = 25 °C, I_F = -1.8 A, dI/dt = 10 0 A/μs b	–	240	360	ns
Body diode reverse recovery cha rge	Qrr		–	1.7	2.6	μC
Forward turn-on time	ton	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)
- Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS

(25 °C, unless otherwise noted)

Fig. 1 – Typical Output Characteristics

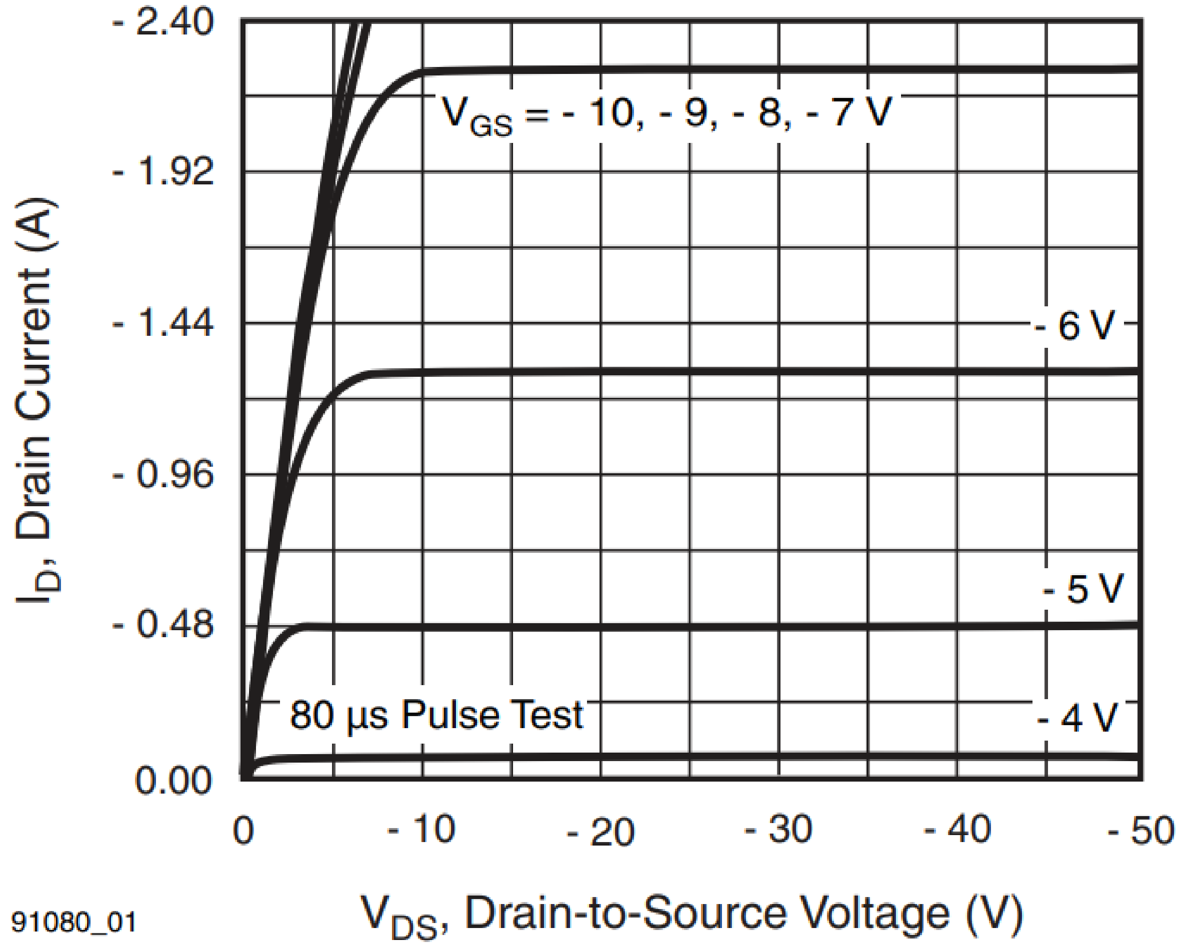


Fig. 2 – Typical Transfer Characteristics

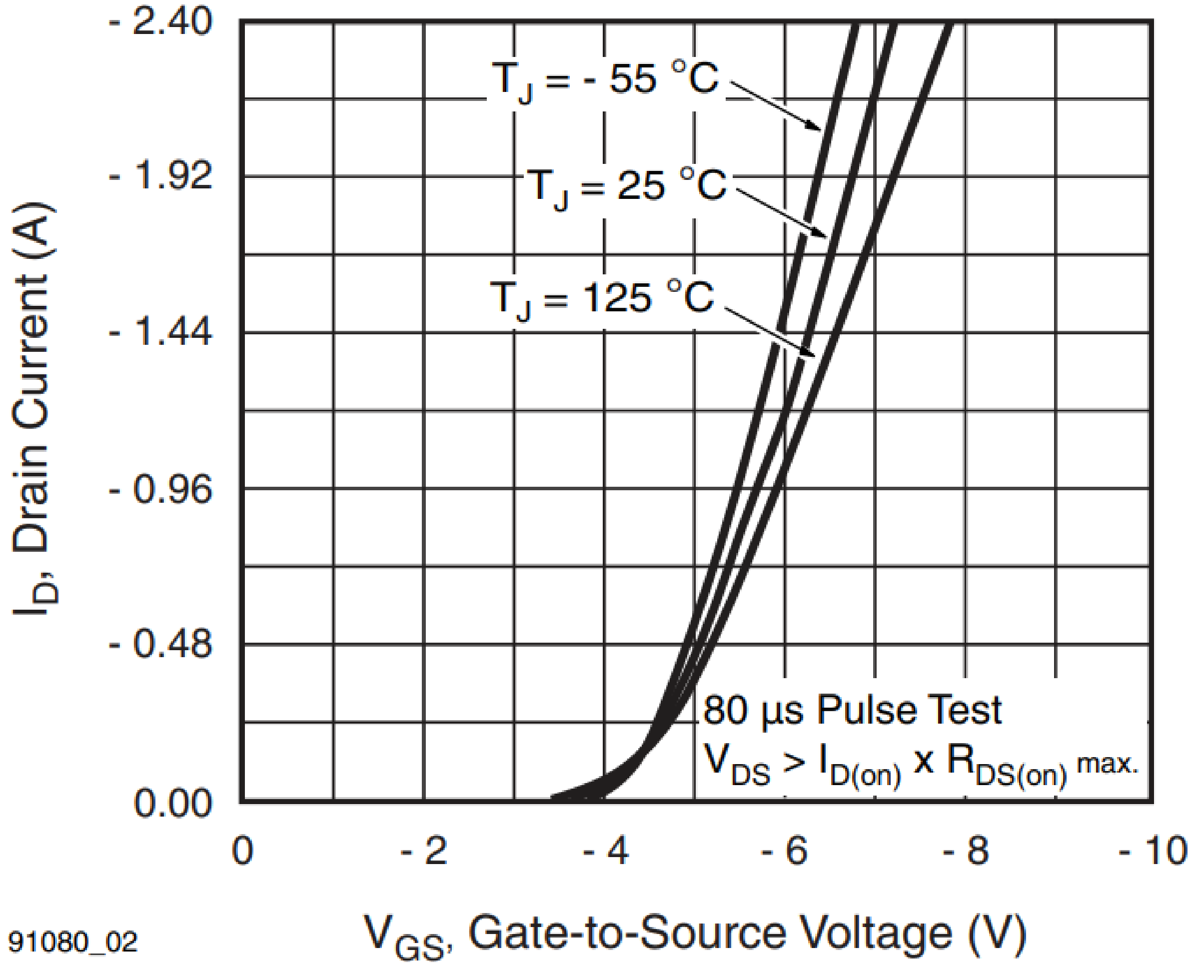


Fig. 3 – Typical Saturation Characteristics

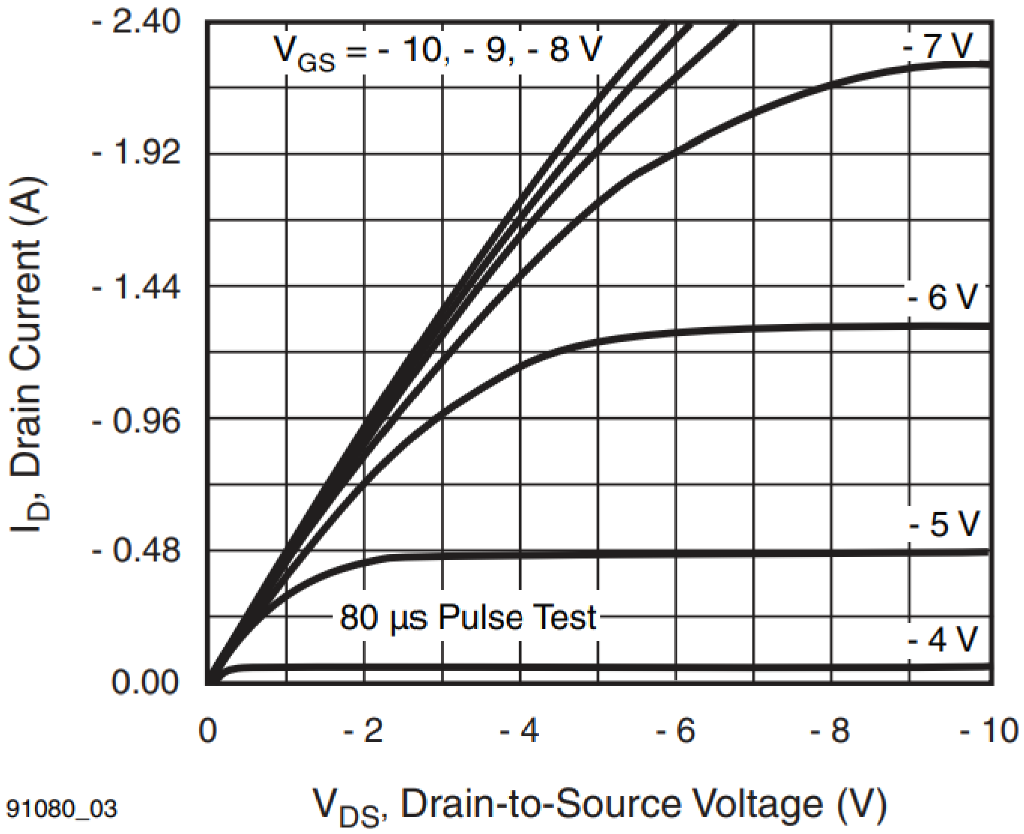


Fig. 4 – Maximum Safe Operating Area

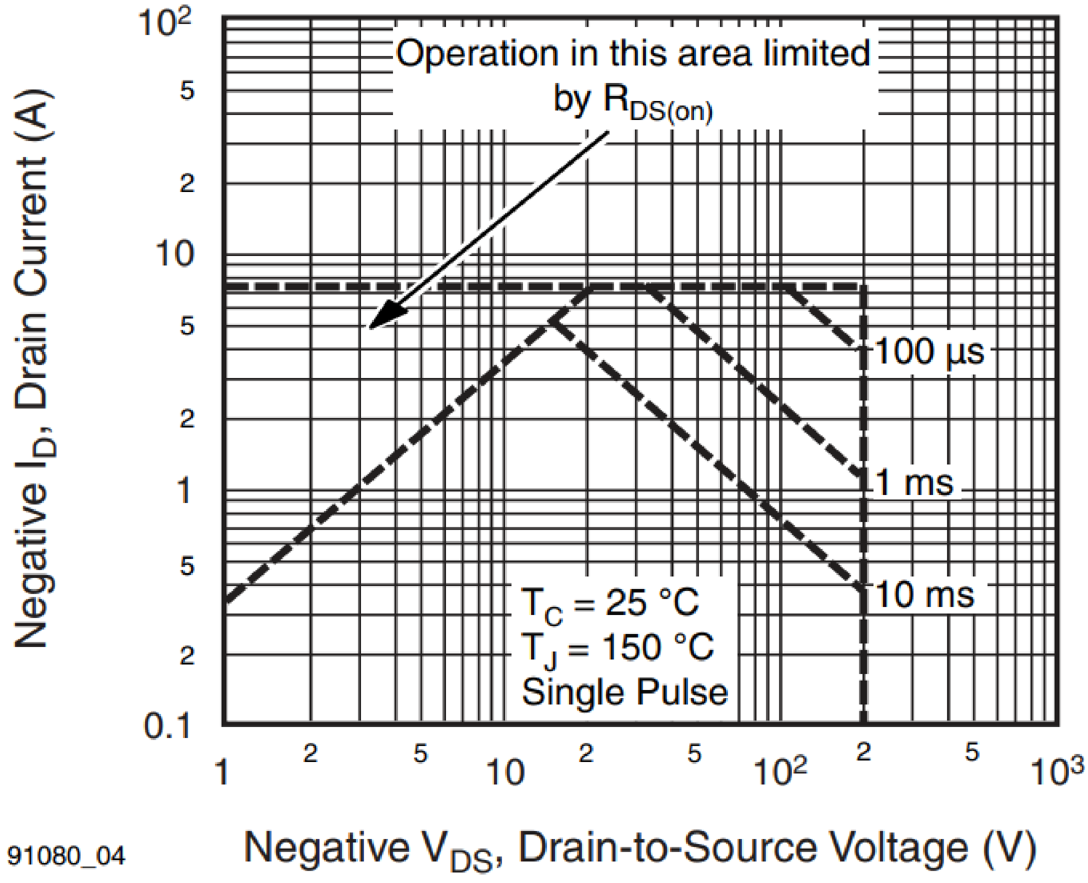


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

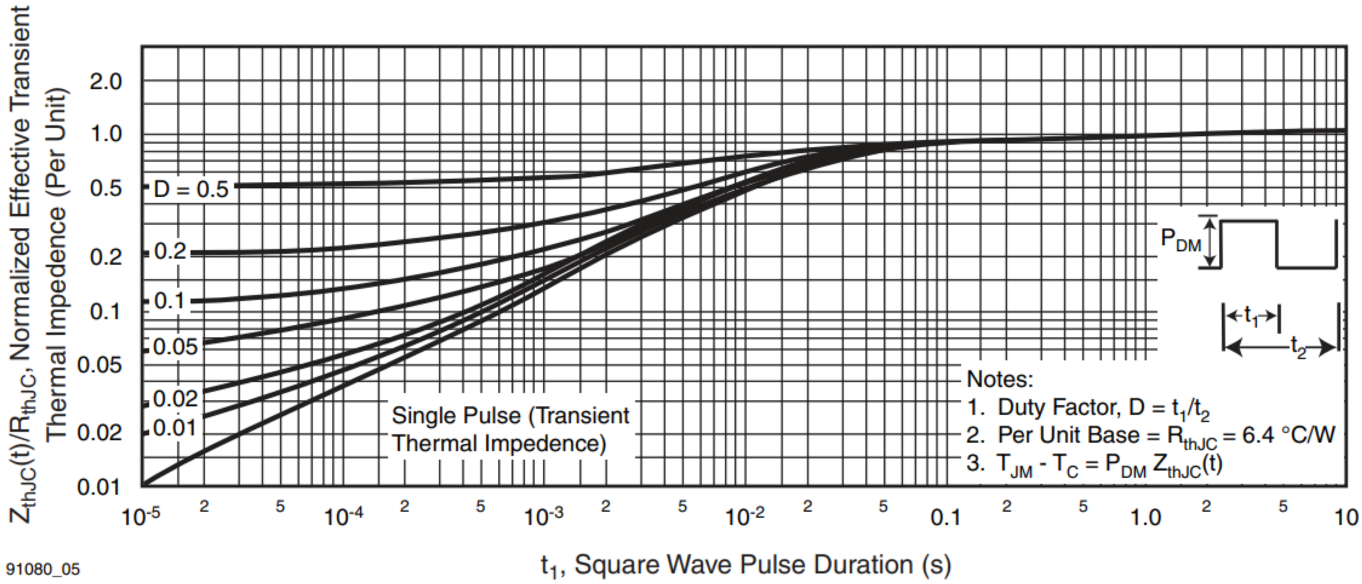


Fig. 6 – Typical Transconductance vs. Drain Current

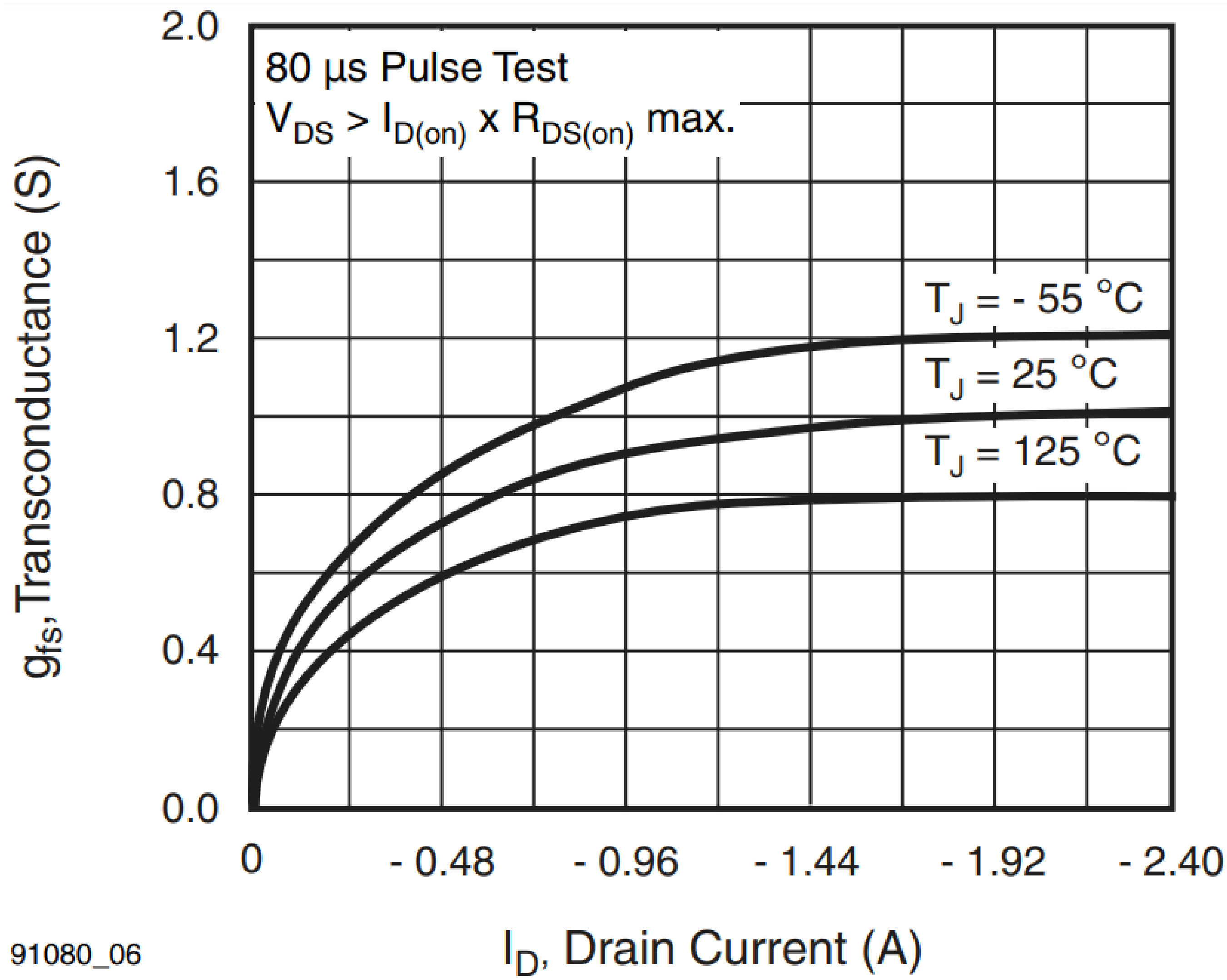


Fig. 7 – Typical Source-Drain Diode Forward Voltage

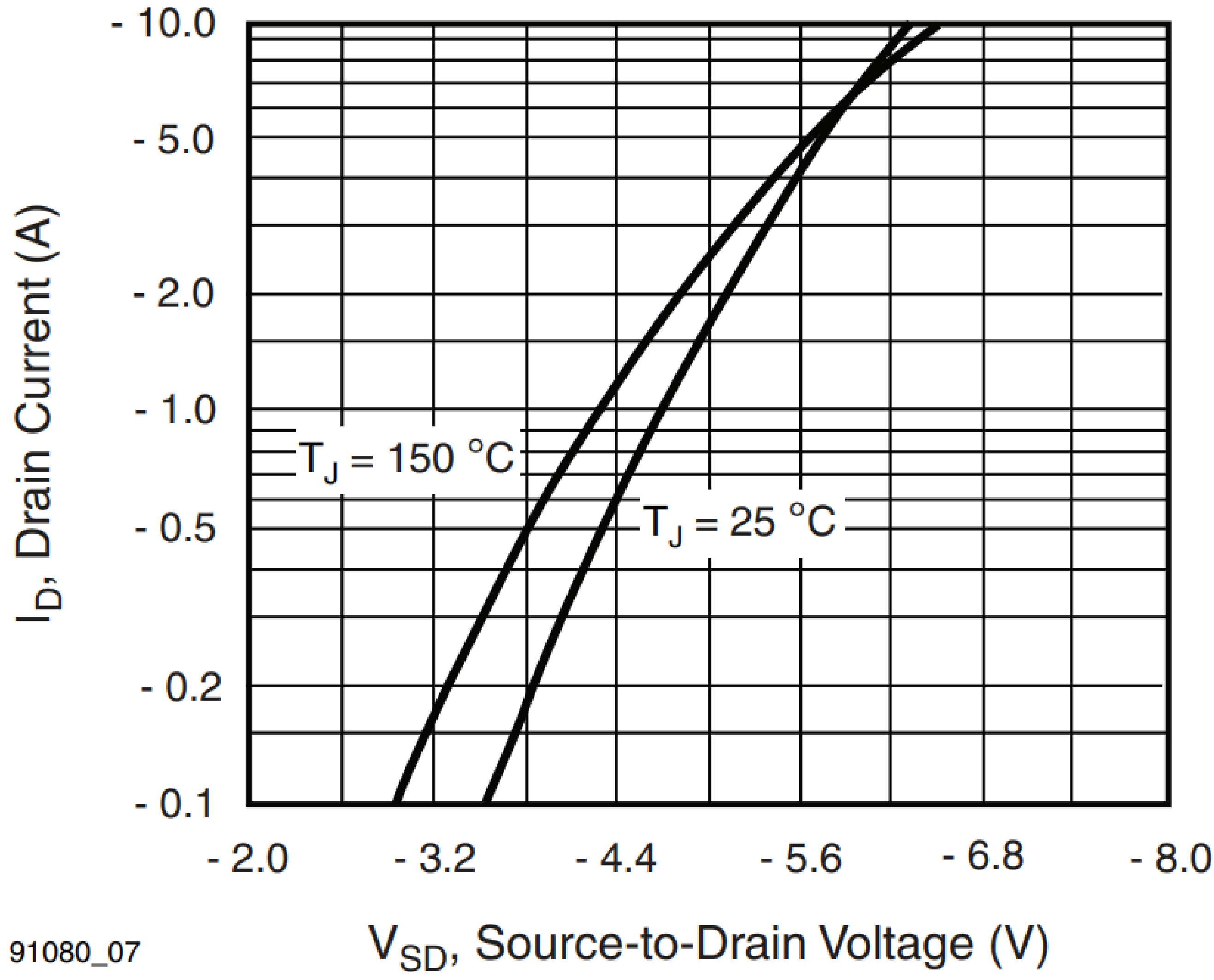


Fig. 8 – Breakdown Voltage vs. Temperature

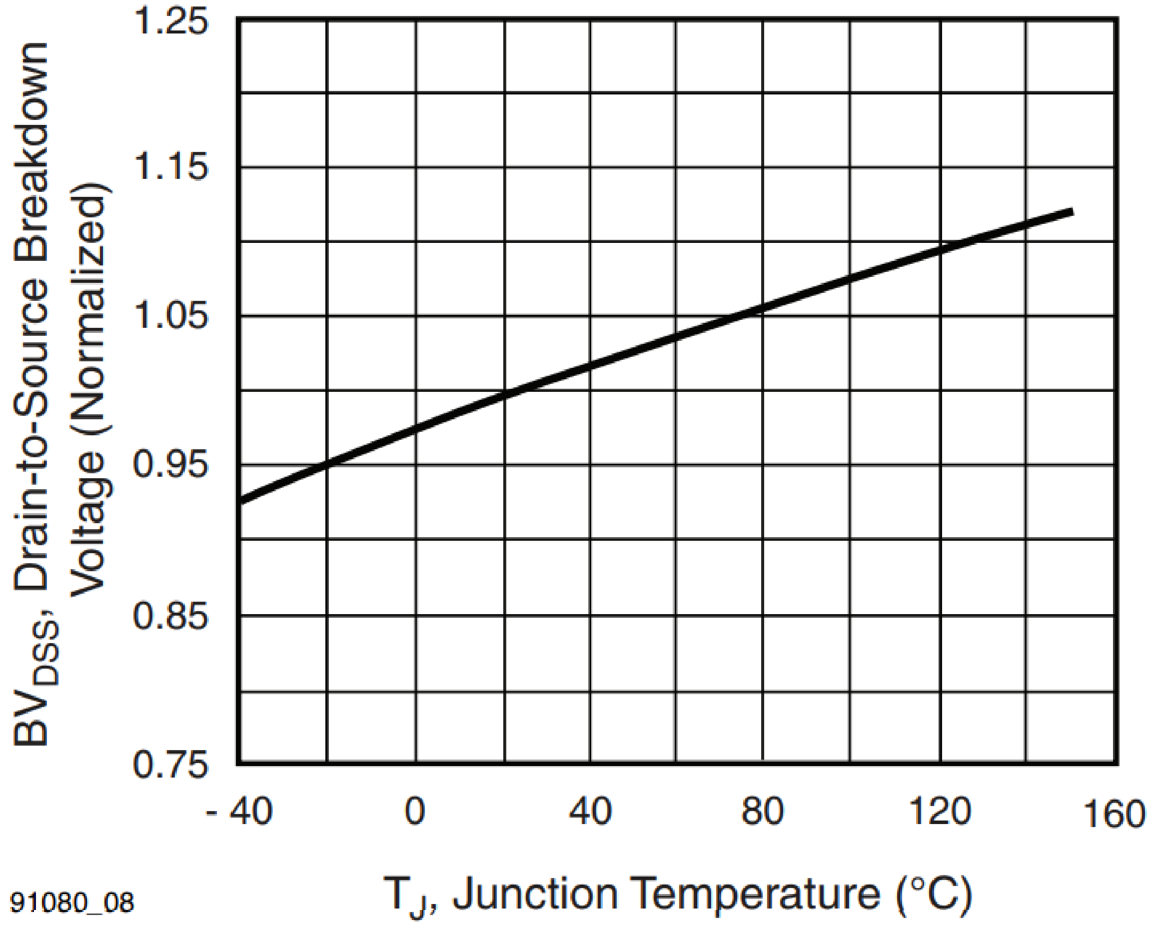


Fig. 9 – Normalized On-Resistance vs. Temperature

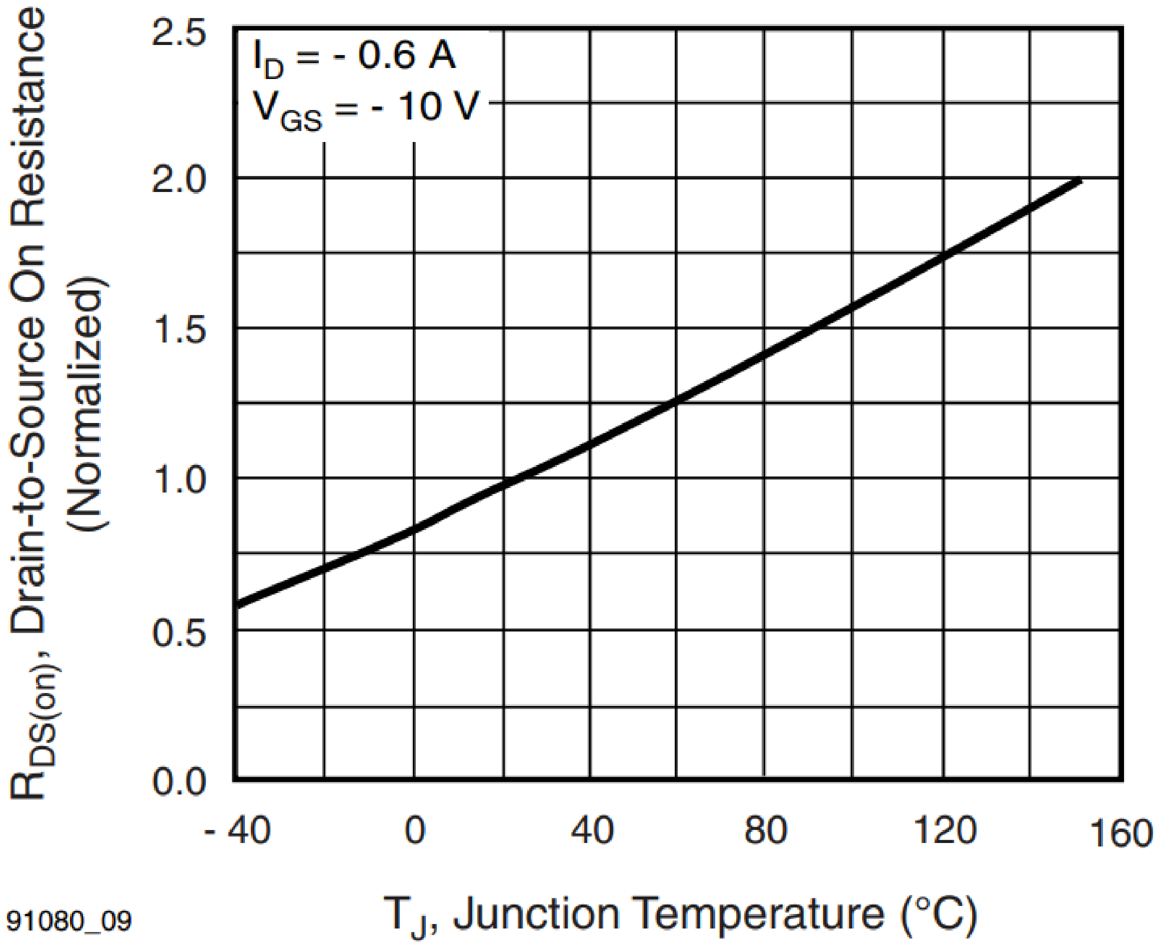


Fig. 10 – Typical Capacitance vs. Drain-to-Source Voltage

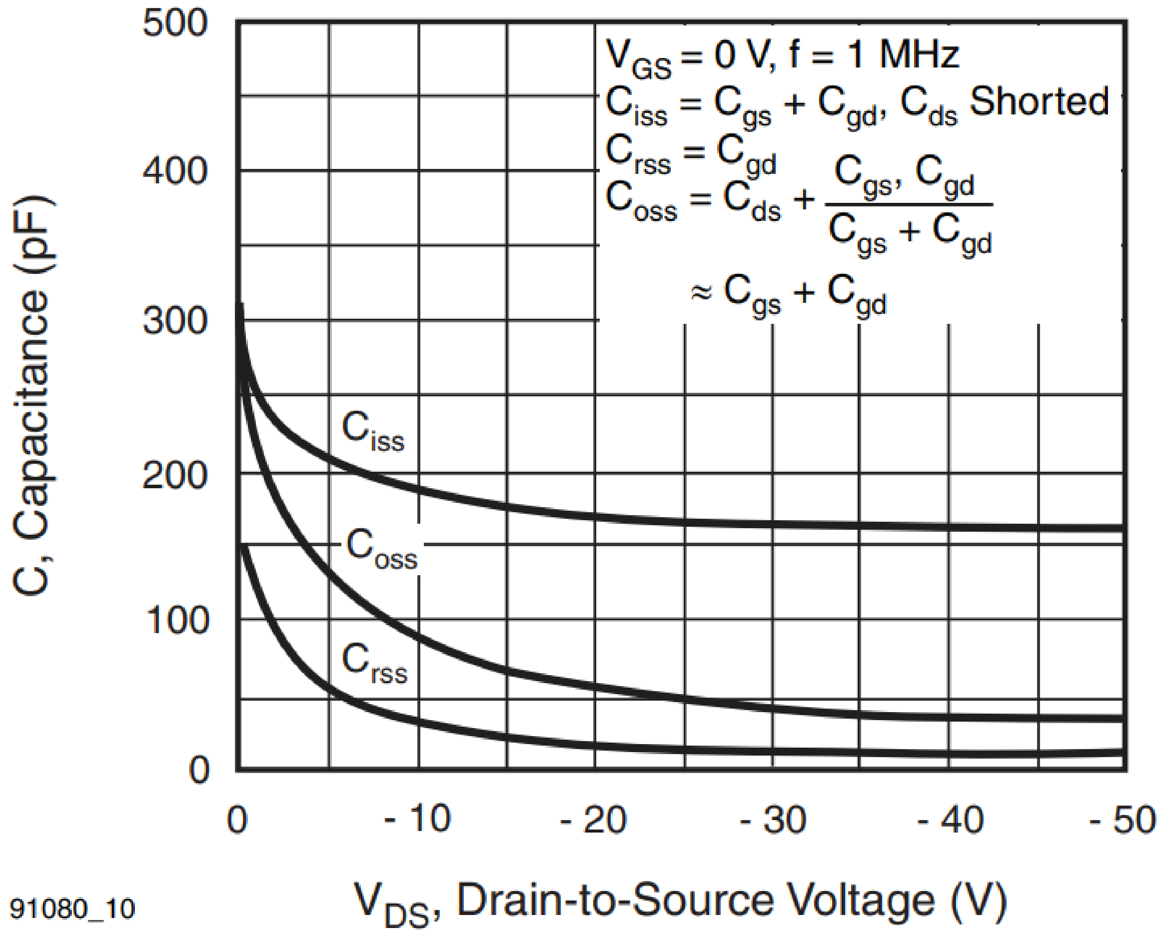


Fig. 11 – Typical Gate Charge vs. Gate-to-Source Voltage

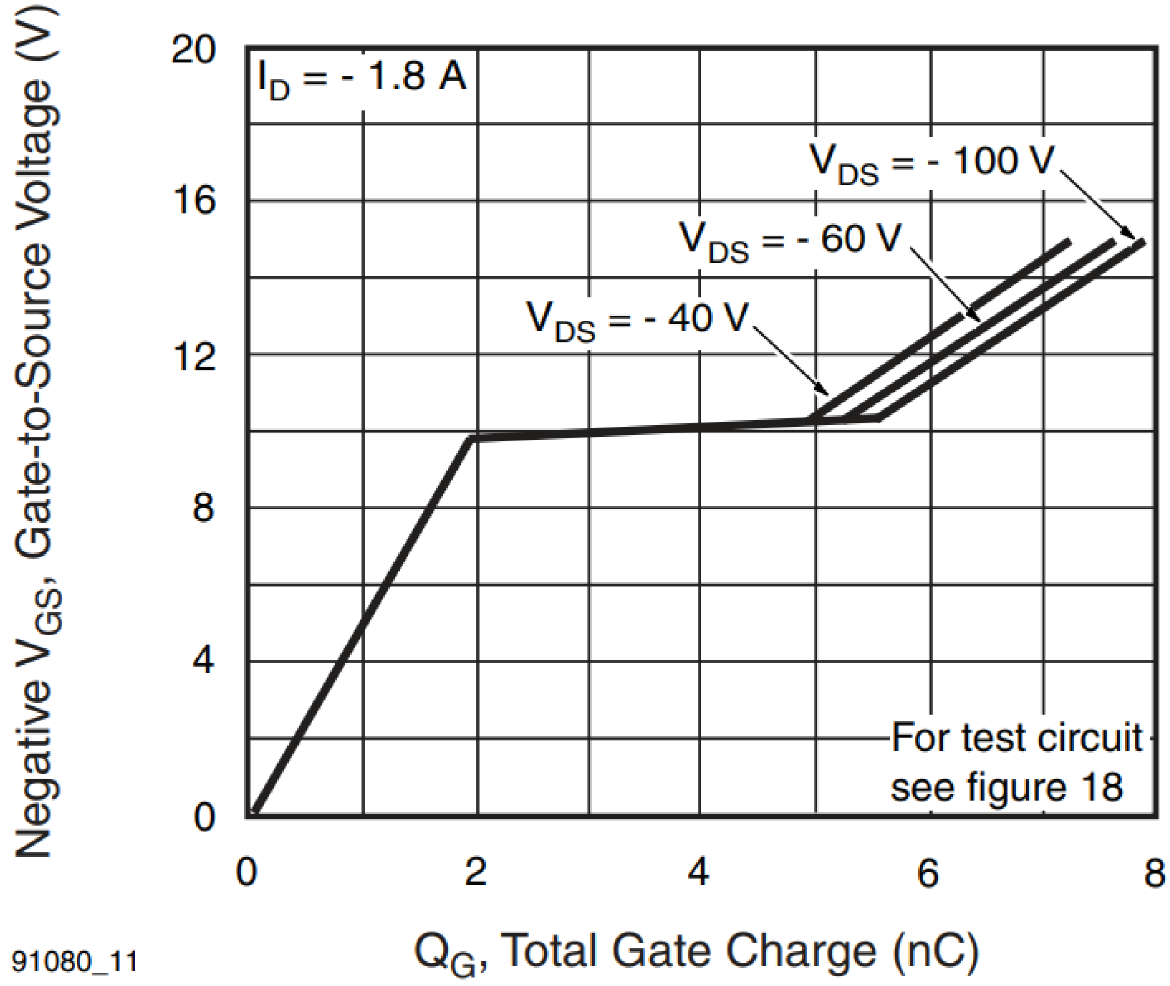


Fig. 12 – Typical On-Resistance vs. Drain Current

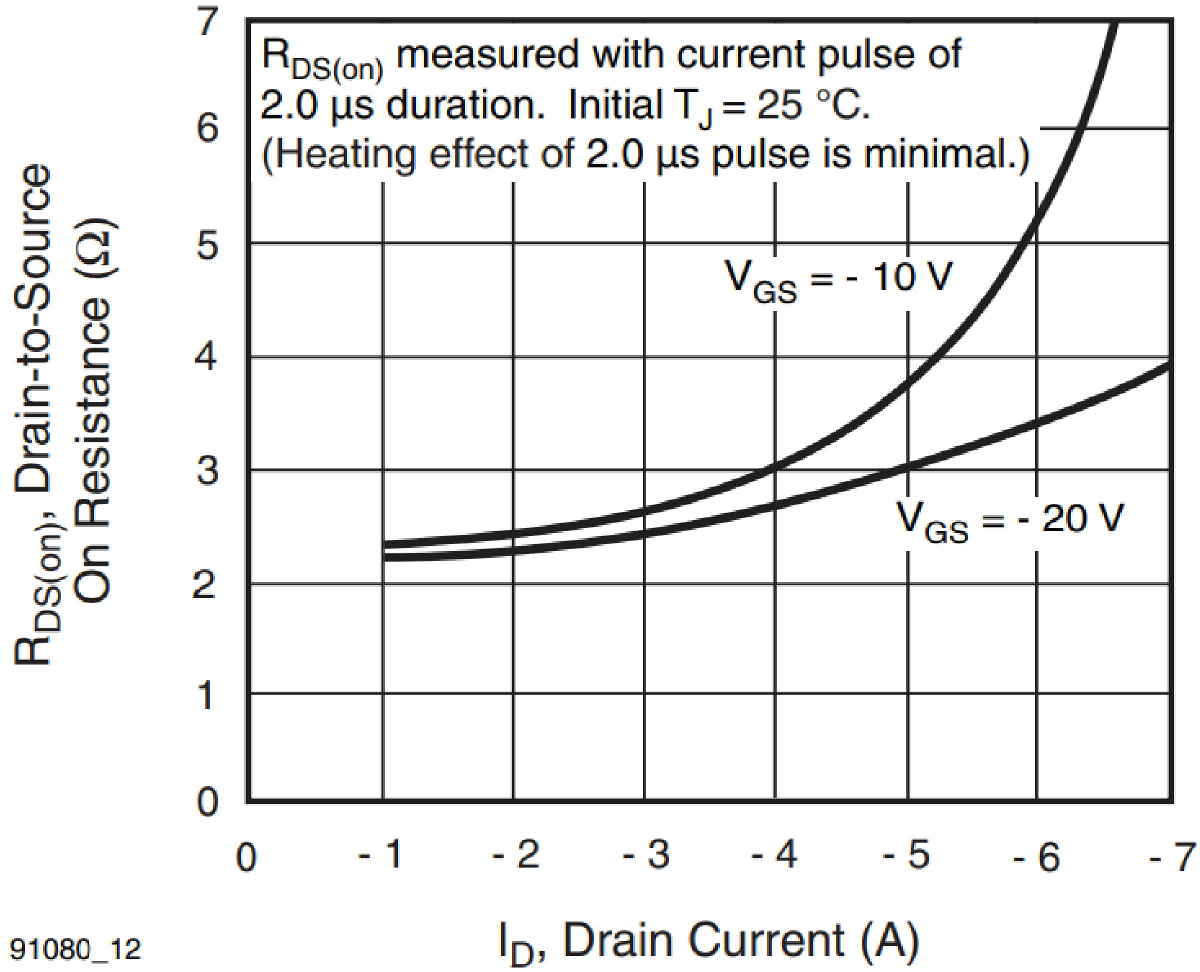


Fig. 13 – Maximum Drain Current vs. Case Temperature

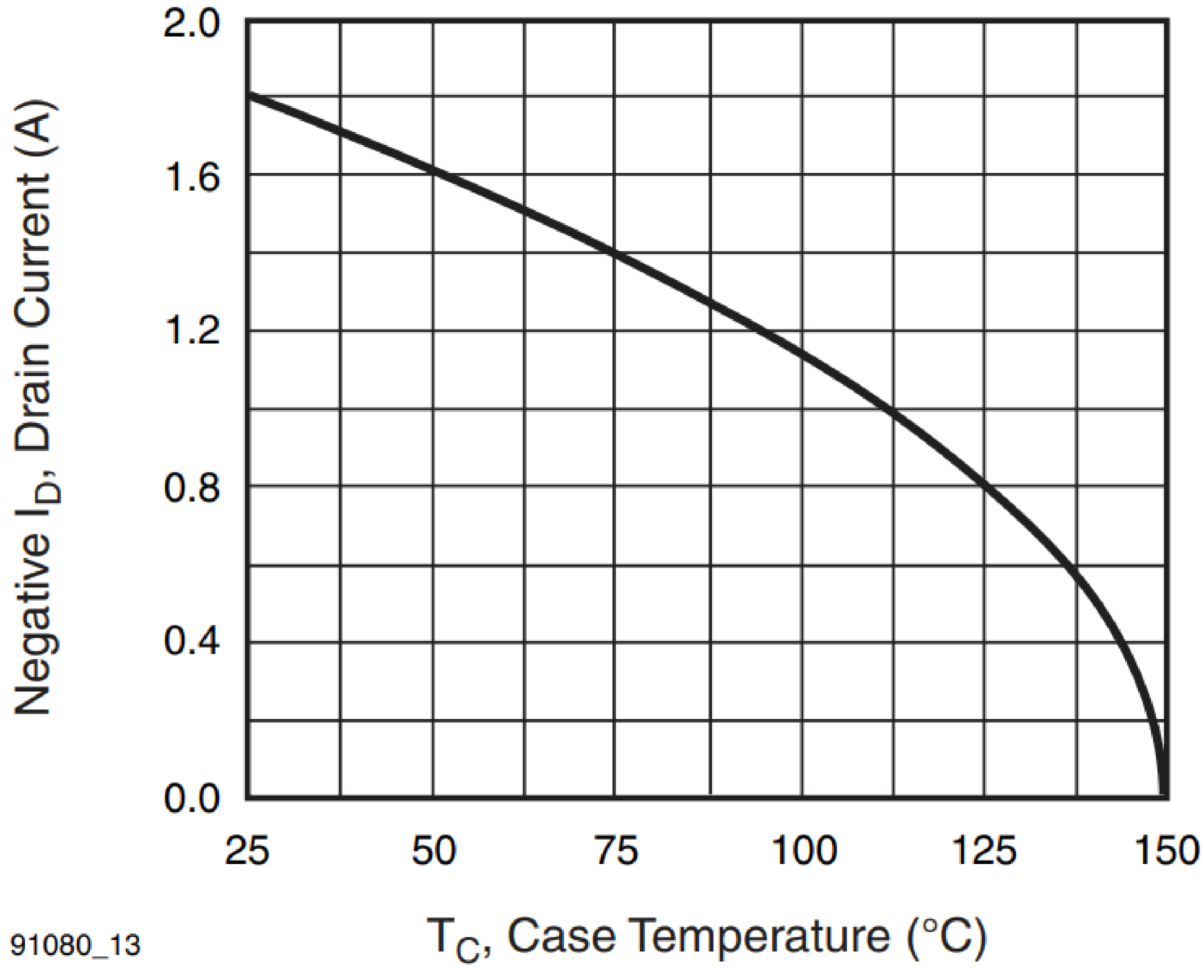


Fig. 14 – Power vs. Temperature Derating Curve

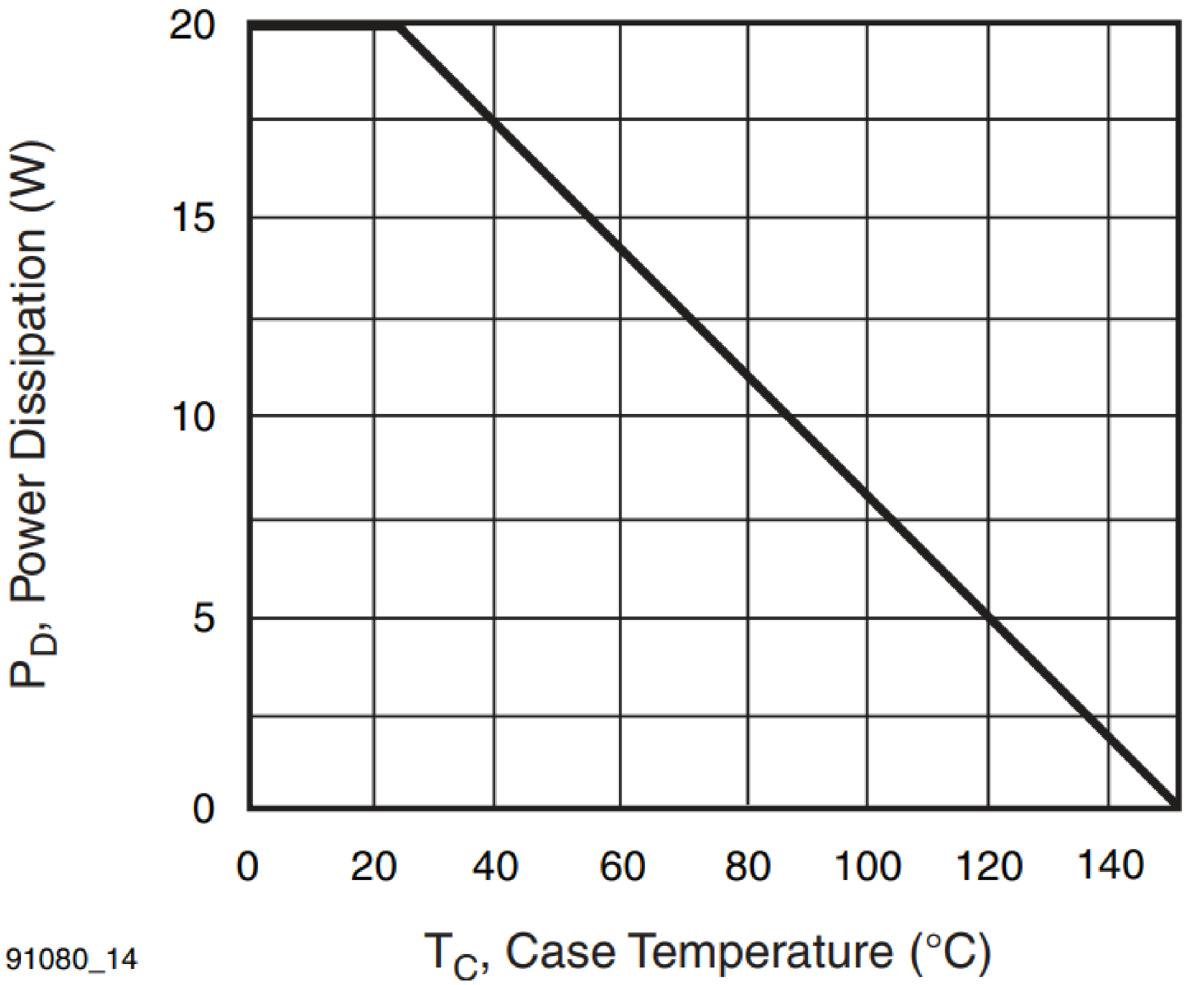


Fig. 15 – Clamped Inductive Test Circuit

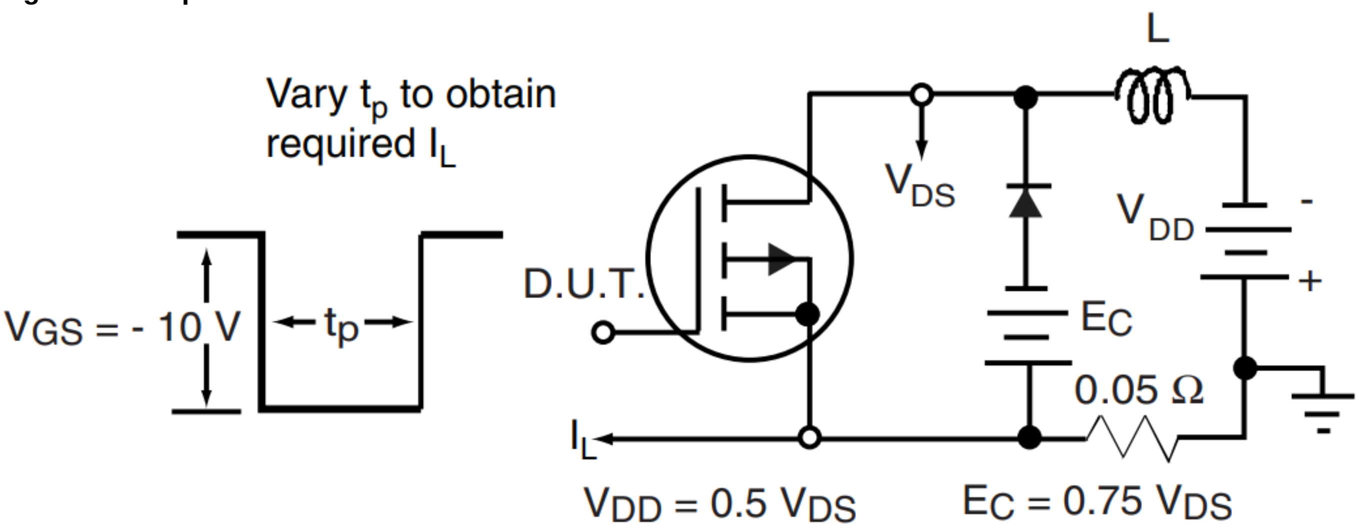


Fig. 16 – Clamped Inductive Waveforms

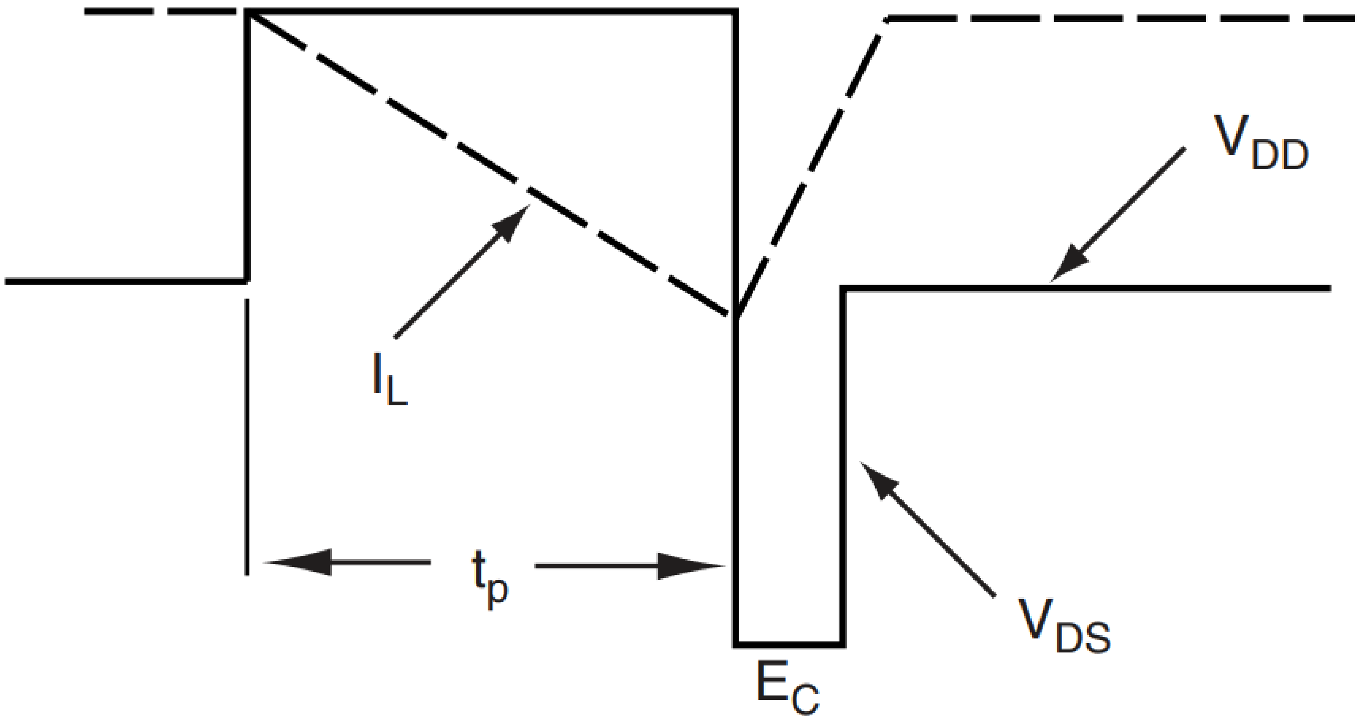


Fig. 17a – Switching Time Test Circuit

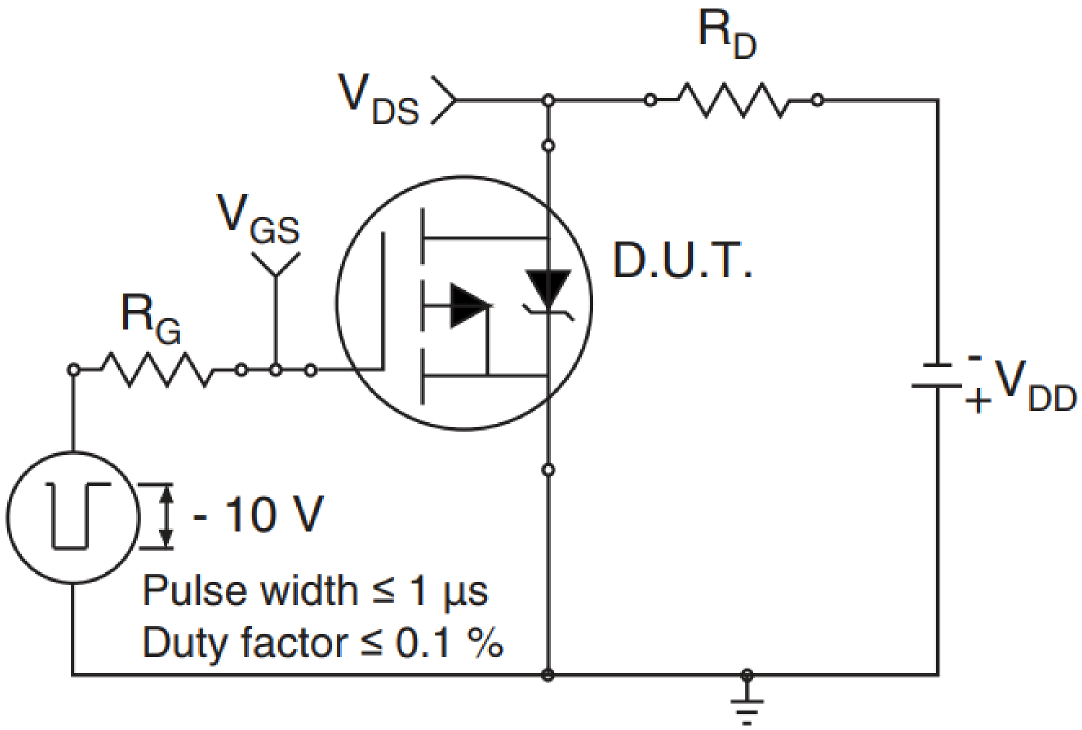


Fig. 17b – Switching Time Waveforms

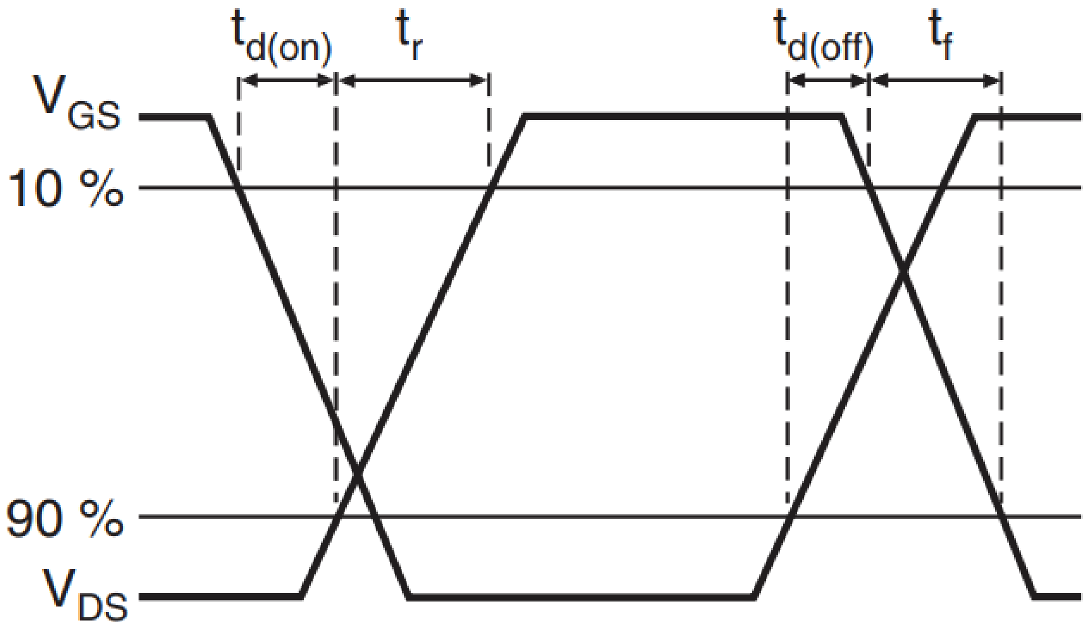


Fig. 18a – Basic Gate Charge Waveform

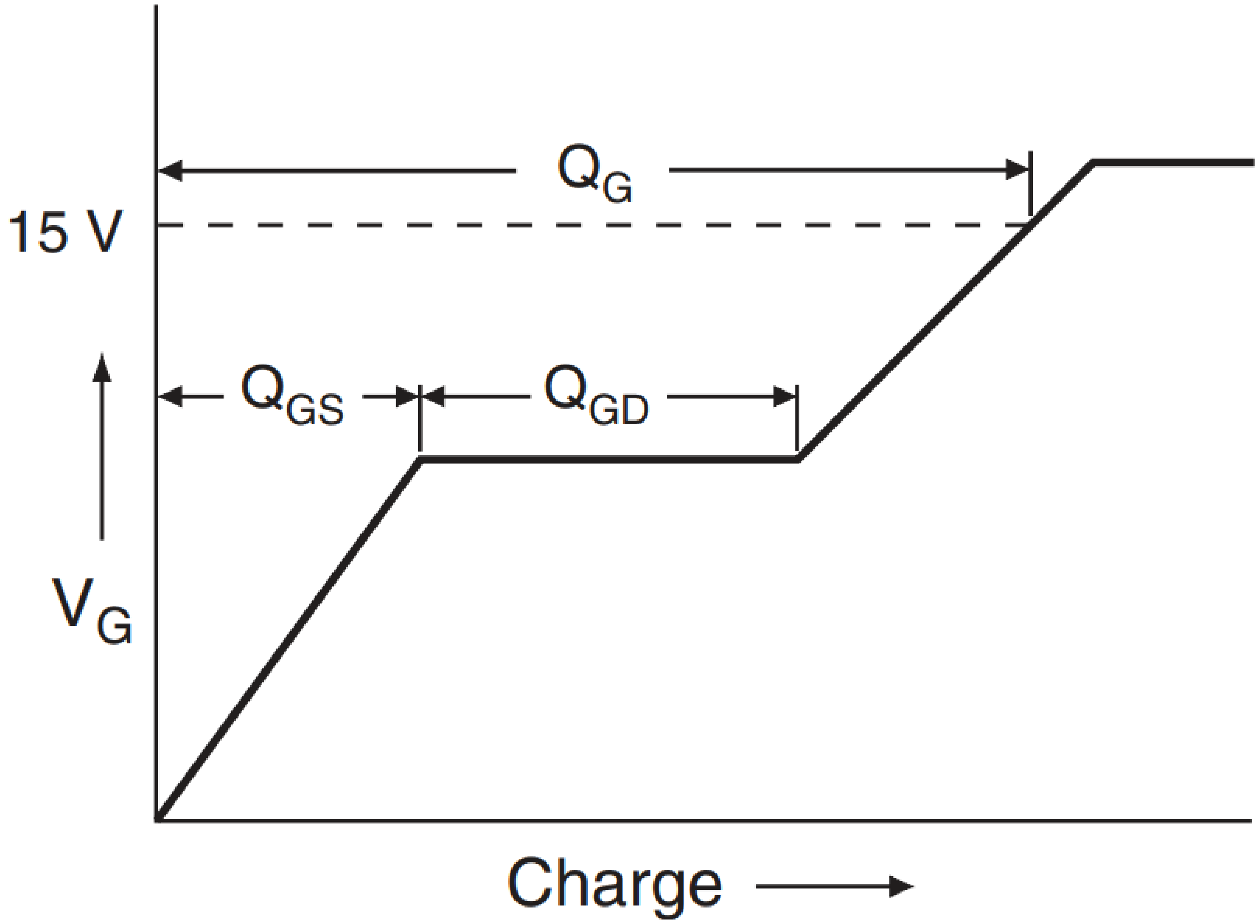
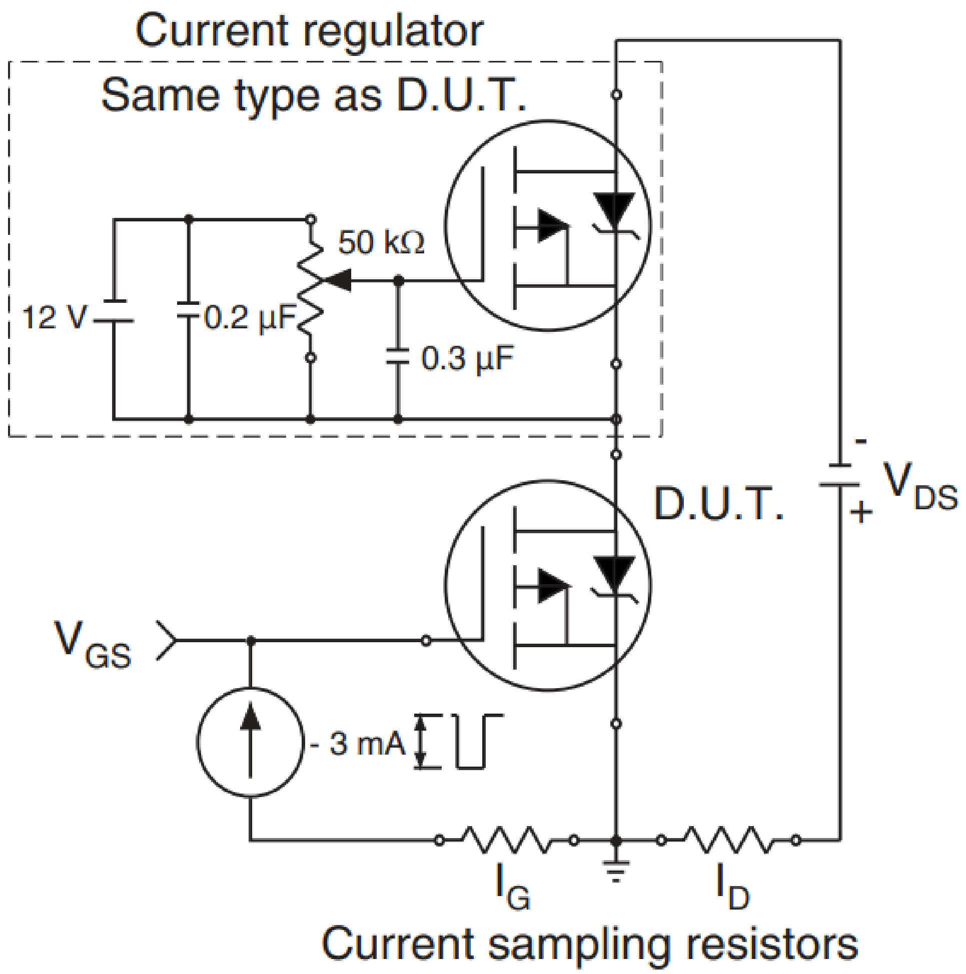
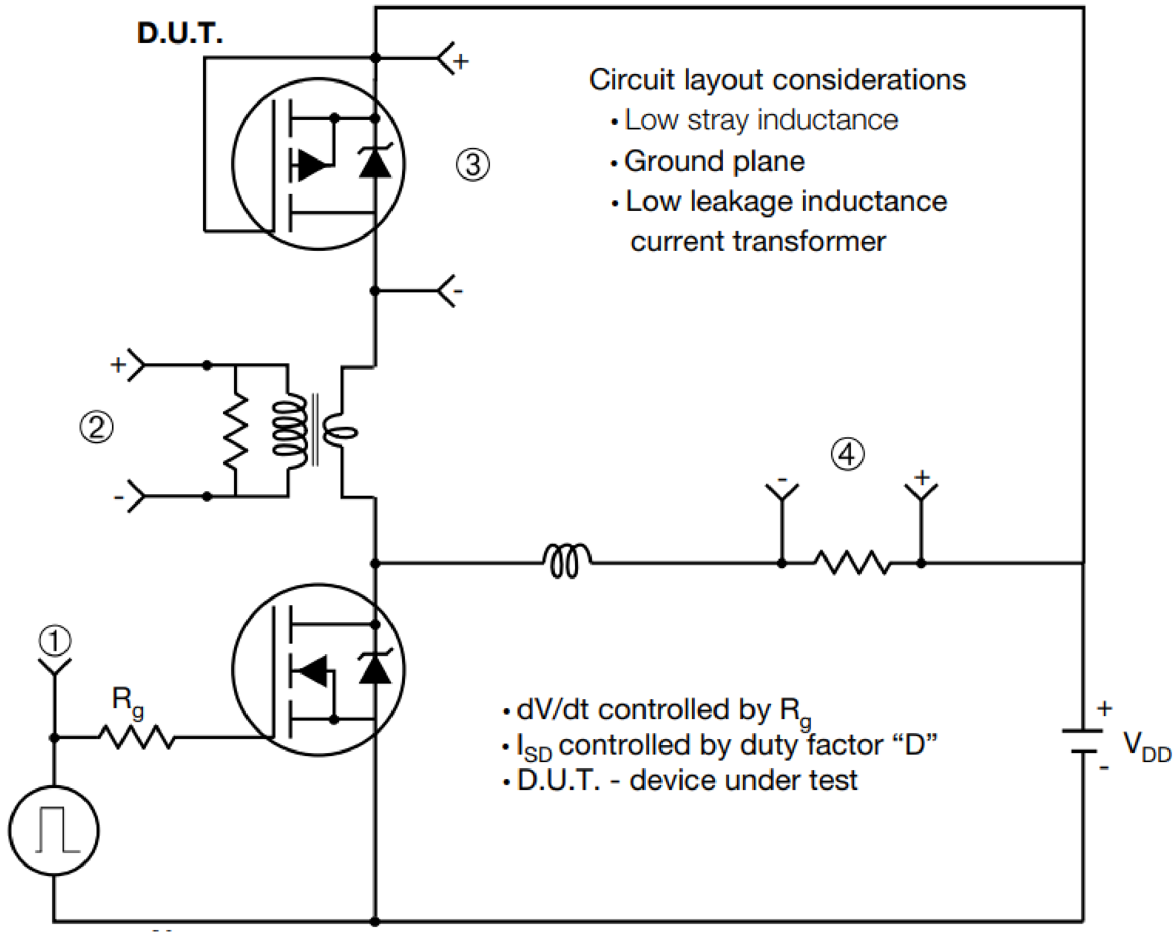


Fig. 18b – Gate Charge Test Circuit



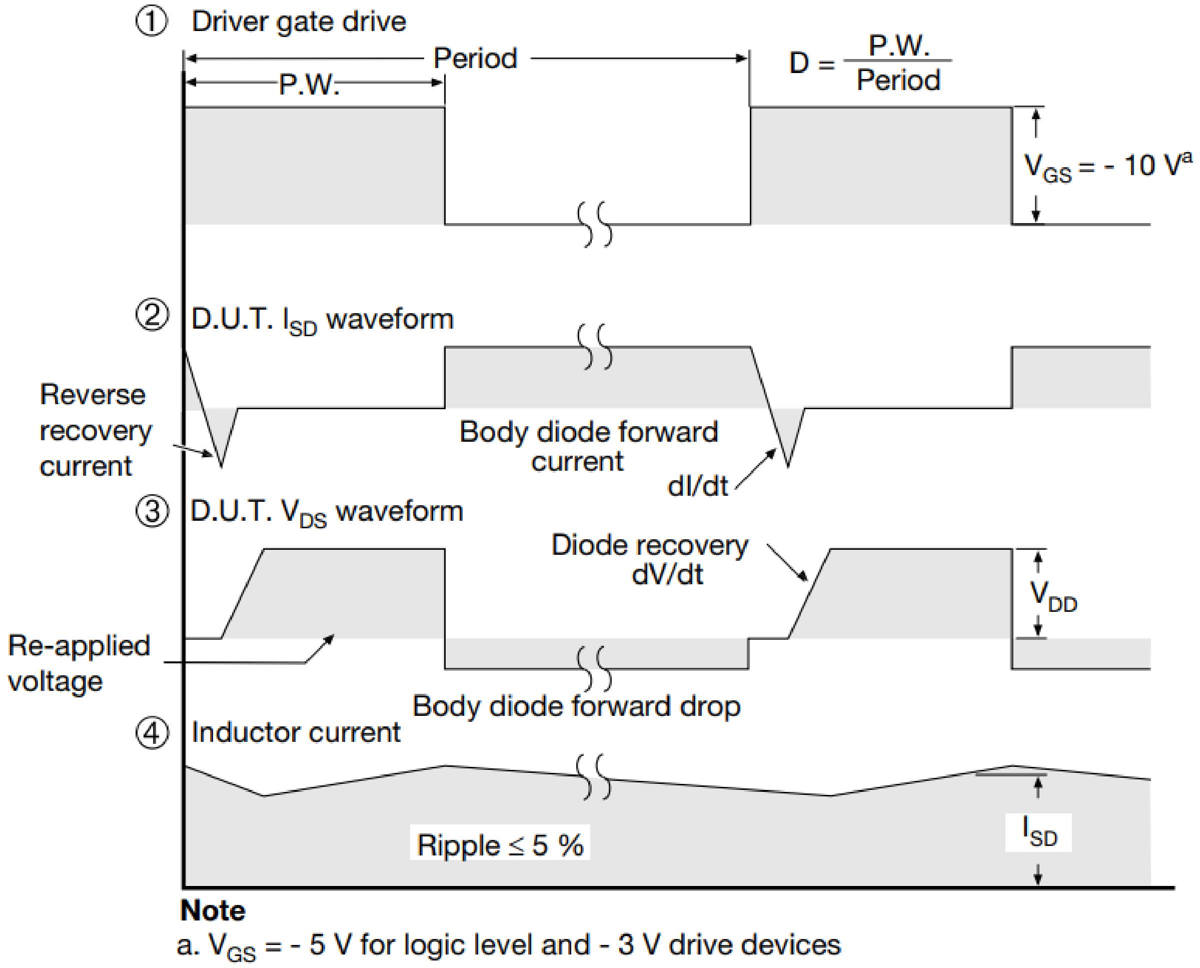
Peak Diode Recovery dV/dt Test Circuit



Note

- Compliment N-Channel of D.U.T. for driver

Fig. 19 – For P-Channel



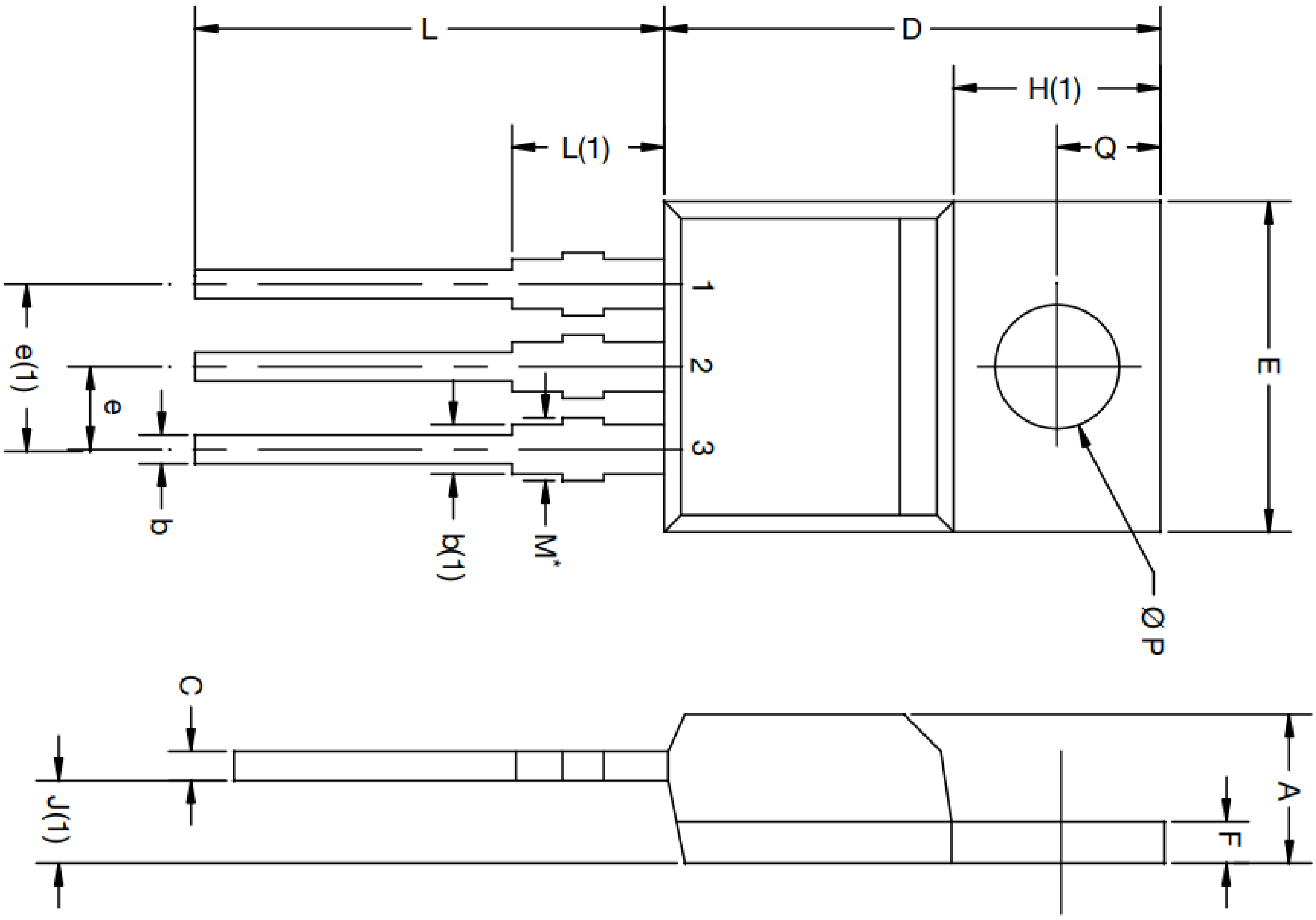
Note

- VGS = – 5 V for logic level and – 3 V drive devices

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see **www.vishay.com/ppg?91080**.

Package Information

TO-220-1

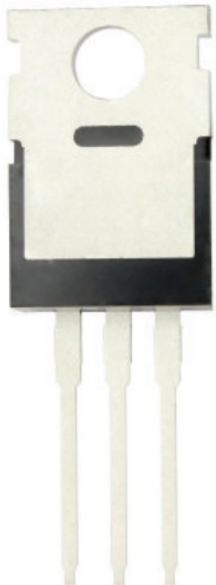
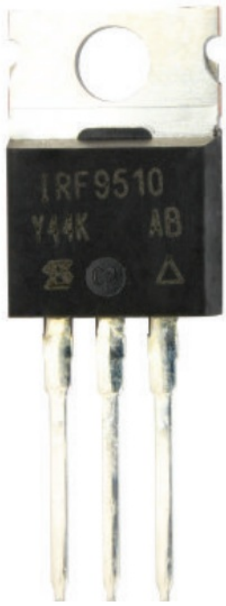
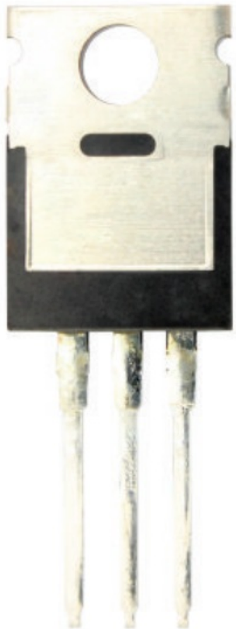

L
D
H(1)
L(1)
Q
E
1
2
3
e(1)
e
b
b(1)
M*
ØP
C
J(1)
A
F

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031				

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture

ASE		Xi'an	
			

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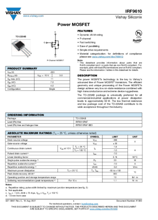	VISHAY IRF9610 Siliconix [pdf] Instructions IRF9610 Siliconix, IRF9610, Siliconix

References

- Vishay Intertechnology
- vishay.com/doc?91000
- vishay.com/doc?99912