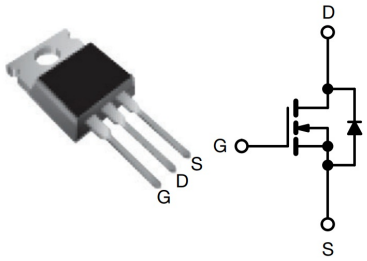
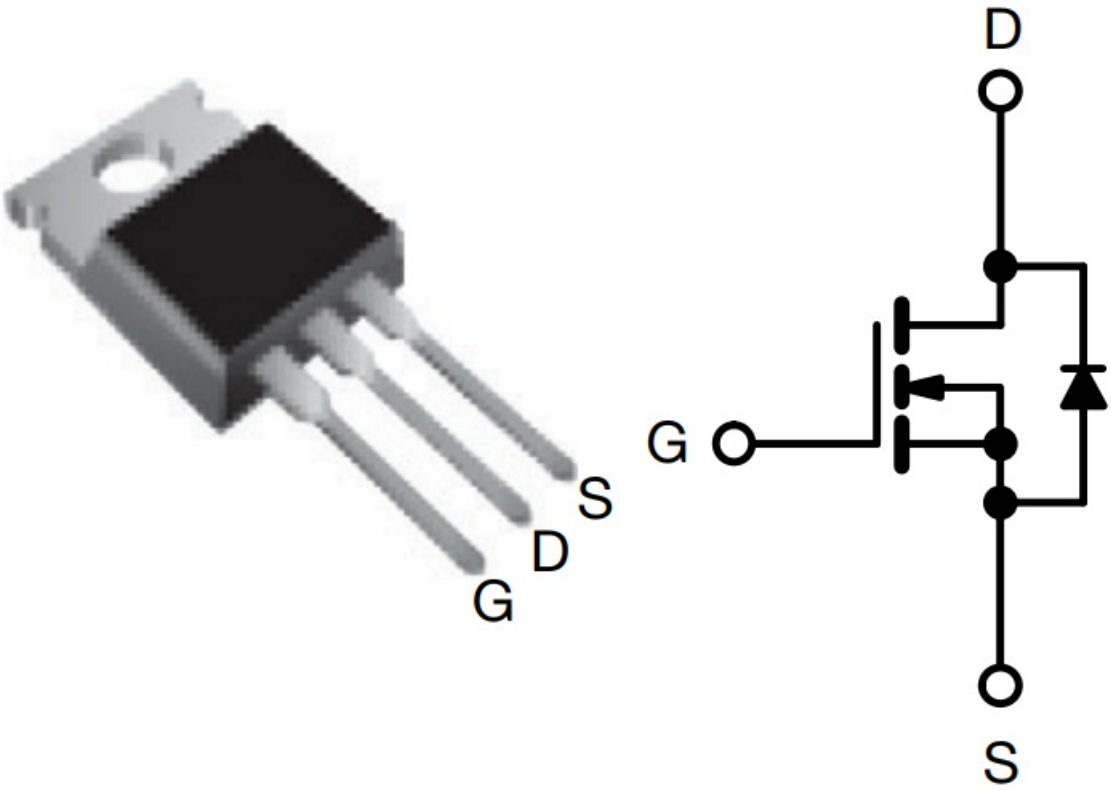


VISHAY IRF830B D Series Power MOSFET Owner's Manual

VISHAY IRF830B D Series Power MOSFET



Contents

FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance (Ciss)
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): Ron x Qg
  - Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- Battery chargers

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. (Ù) at 25 °C	V_{GS} = 10 V	1.5
Q_g max. (nC)	20	
Q_{gs} (nC)	3	
Q_{gd} (nC)	5	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF830BPbF
Lead (Pb)-free and halogen-free	IRF830BPbF-BE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-source voltage			VDS	500	V
Gate-source Voltage			VGS	± 30	
Gate-source voltage AC (f > 1 Hz)				30	
Continuous drain current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	5.3	A
		T_C = 100 °C		3.4	
Pulsed drain current a			IDM	10	
Linear derating factor				0.83	W/°C
Single pulse avalanche energy b			EAS	28.8	mJ
Maximum power dissipation			P_D	104	W
Operating junction and storage temperature range			TJ, Tstg	-55 to +150	°C
Drain-source voltage slope	T_J = 125 °C		dV/dt	24	V/ns
Reverse diode dV/dt d				0.28	
Soldering recommendations (peak temperature) c	For 10 s			300	°C

Notes

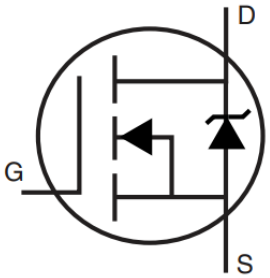
- **a.** Repetitive rating; pulse width limited by maximum junction temperature
- **b.** VDD = 50 V, starting TJ = 25 °C, L = 2.3 mH, Rg = 25 Ω, IAS = 5 A
- **c.** 1.6 mm from case
- **d.** ISD ≤ ID, starting TJ = 25 °C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	RthJA	–	62	°C/W
Maximum junction-to-case (drain)	RthJC	–	1.2	

SPECIFICATIONS

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	VDS	V_{GS} = 0 V, I_D = 250 µA	500	–	–	V
V_{DS} temperature coefficient	ÄV_{DS}/T_J	Reference to 25 °C, I_D = 250 µA	–	0.58	–	V/°C
Gate-source threshold voltage (N)	VGS(th)	V_{DS} = V_{GS}, I_D = 250 µA	3	–	5	V
Gate-source leakage	IGSS	V_{GS} = ± 30 V	–	–	± 100	nA
Zero gate boltage drain current	IDSS	V_{DS} = 500 V, V_{GS} = 0 V	–	–	1	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	–	–	10	
Drain-source on-state resistance	RDS(on)	V_{GS} = 10 V, I_D = 2.5 A	–	1.2	1.5	Ù
Forward transconductance a	gfs	V_{DS} = 20 V, I_D = 2.5 A	–	1.8	–	S
Dynamic						
Input capacitance	Ciss	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	–	325	–	pF
Output capacitance	Coss		–	34	–	
Reverse transfer capacitance	Crss		–	6	–	
Effective output capacitance, en ergy related b	Co(er)	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	31	–	
Effective output capacitance, tim e related c	Co(tr)		–	41	–	
Total gate charge	Q_g	V_{GS} = 10 V, I_D = 2.5 A, V_{DS} = 400 V	–	10	20	nC
Gate-source charge	Qgs		–	3	–	
Gate-drain charge	Qgd		–	5	–	
Turn-on delay time	td(on)	V_{DD} = 400 V, I_D = 2.5 A R_g = 9.1	–	12	24	
Rise time	t_r		–	11	22	

Turn-off delay time	td(off)	U, V_{GS} = 10 V	–	14	28	ns
Fall time	t_f		–	11	22	
Gate input resistance	R_g	f = 1 MHz, open drain	0.8	1.7	3.4	Ù
Drain-Source Body Diode Characteristics						
Continuous source-drain diode c urrent	I_S	MOSFET symbol showing the int egral reverse P – N junction diod e 	–	–	5	A
Pulsed diode forward current	ISM		–	–	20	
Diode forward voltage	VSD	T_J = 25 °C, I_S = 4 A, V_{GS} = 0 V	–	–	1.2	V
Reverse recovery time	trr	T_J = 25 °C, I_F = I_S = 2.5 A, dI/dt = 100 A/µs, V_R = 20 V	–	320	–	ns
Reverse recovery charge	Qrr		–	1.2	–	µC
Reverse recovery current	IRRM		–	8	–	A

TYPICAL CHARACTERISTICS

(25 °C, unless otherwise noted)

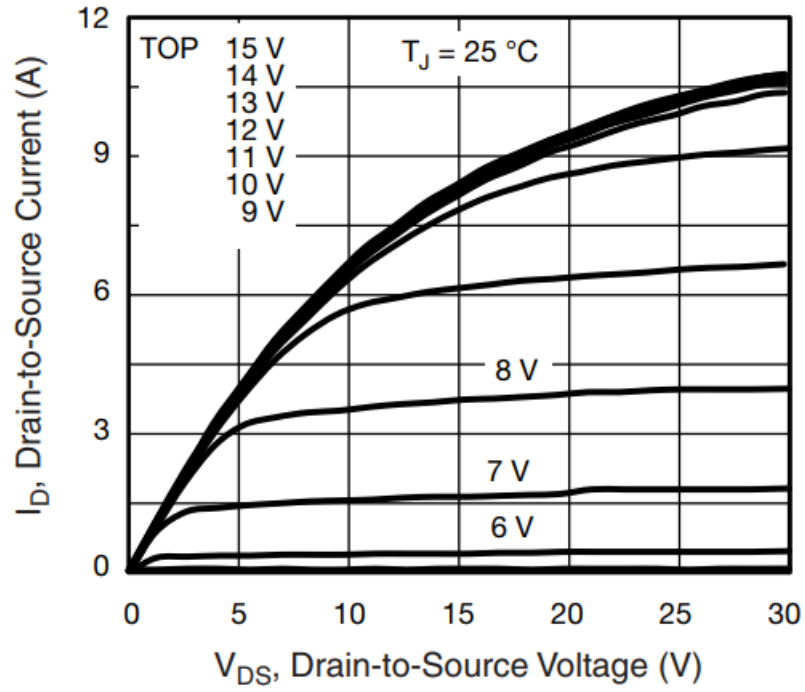


Fig. 1 - Typical Output Characteristics

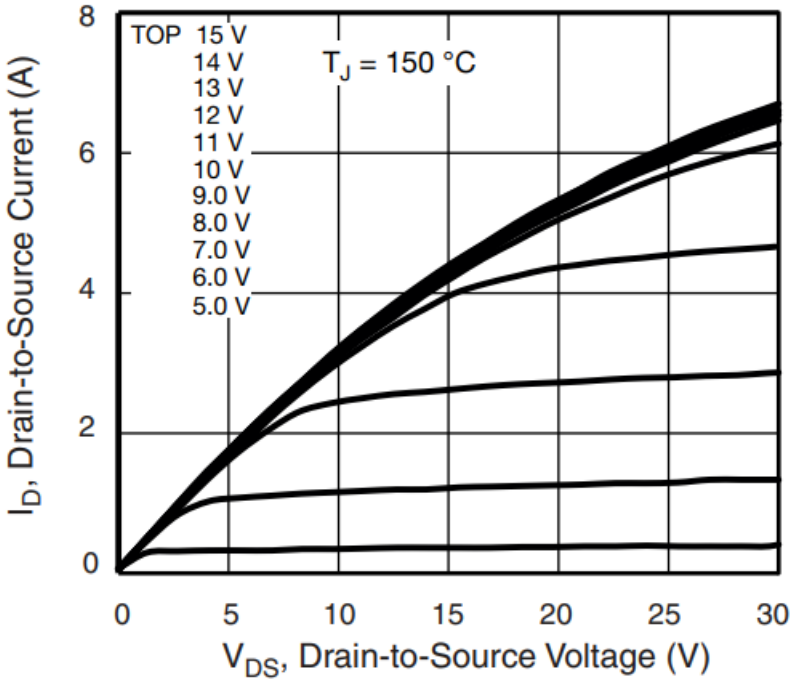


Fig. 2 - Typical Output Characteristics

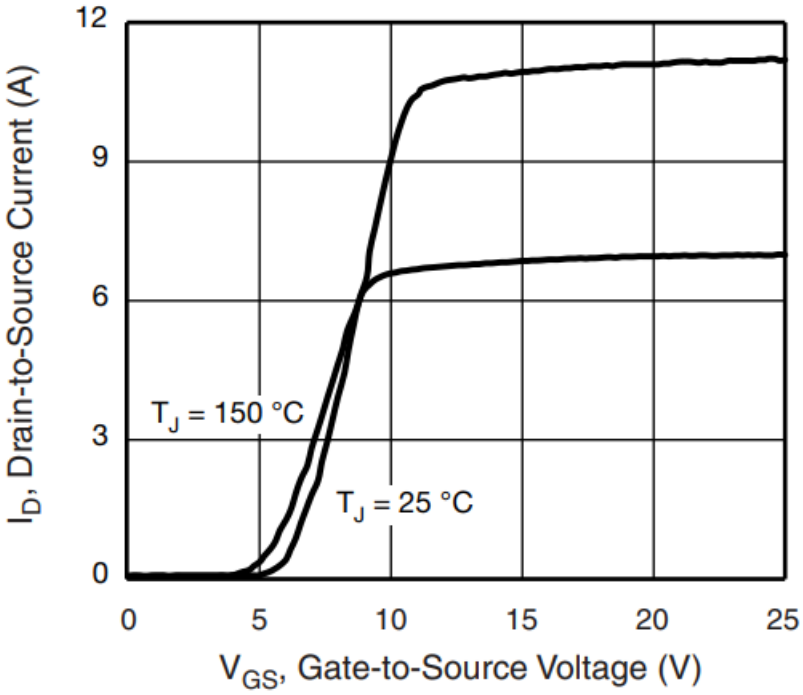


Fig. 3 - Typical Transfer Characteristics

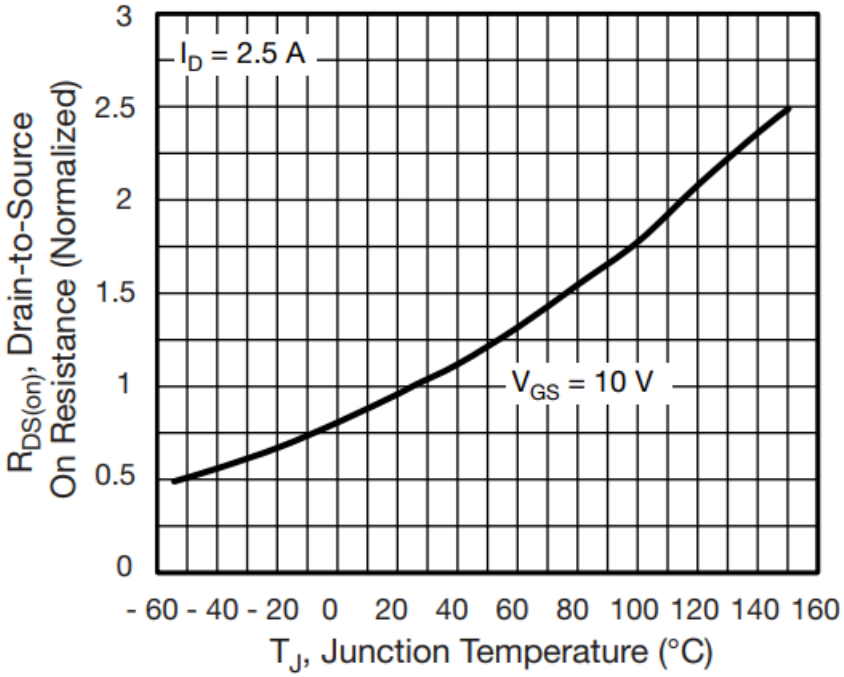


Fig. 4 - Normalized On-Resistance vs. Temperature

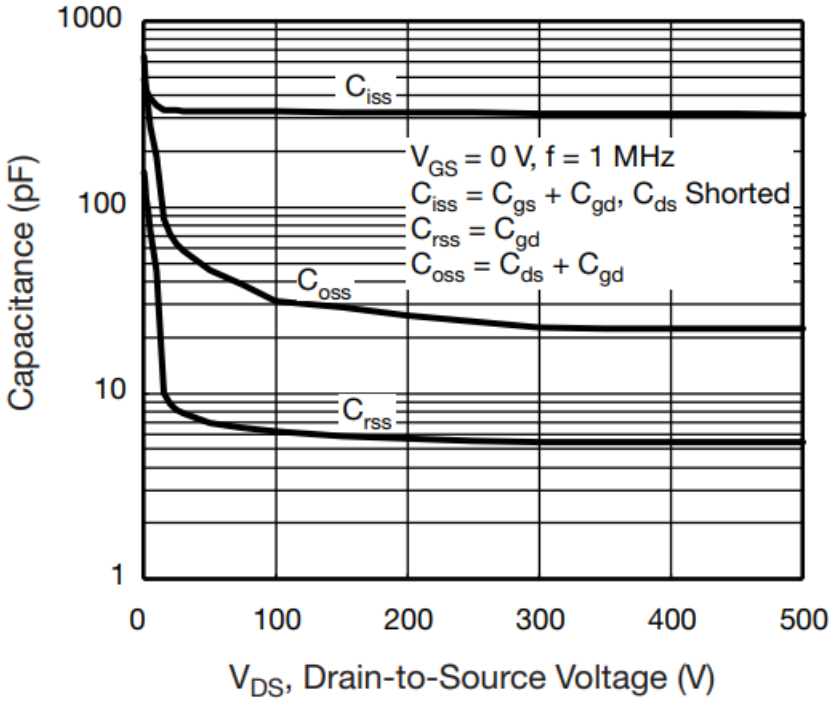


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

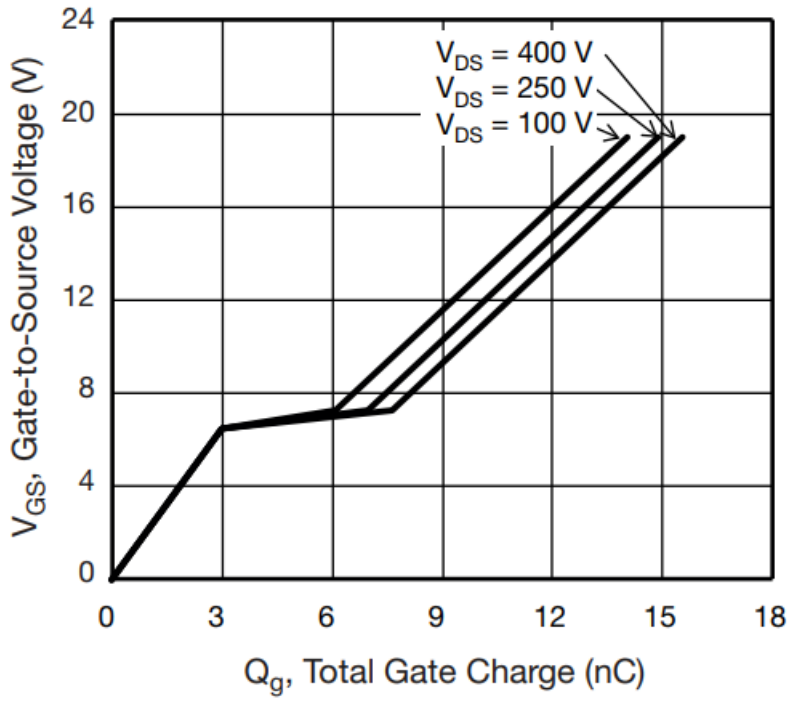


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

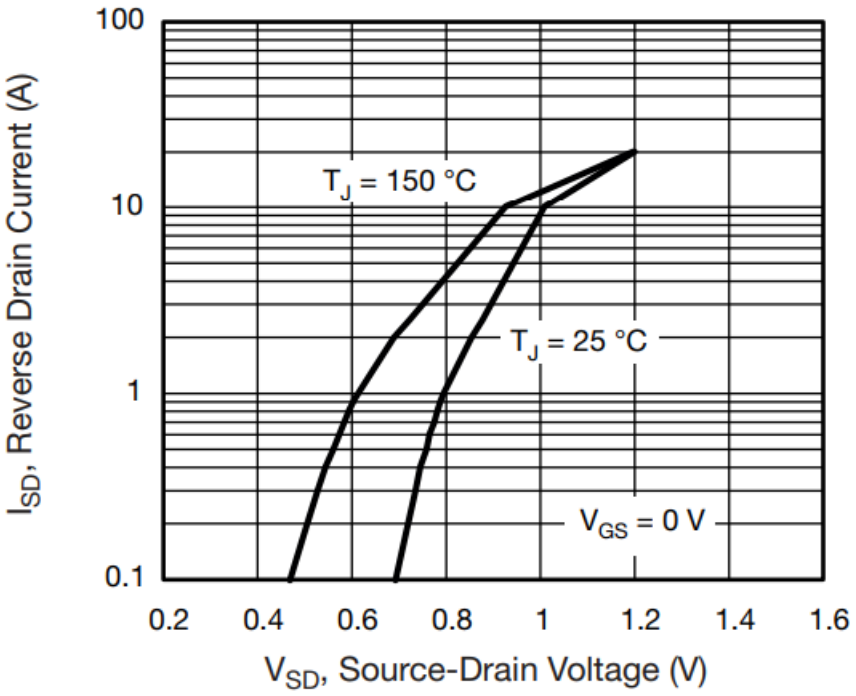


Fig. 7 - Typical Source-Drain Diode Forward Voltage

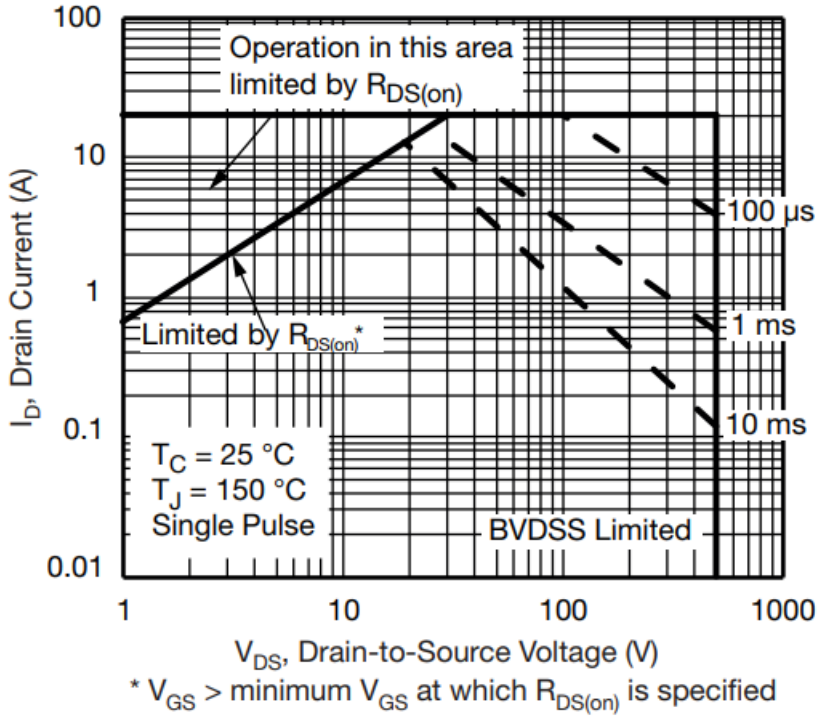


Fig. 8 - Maximum Safe Operating Area

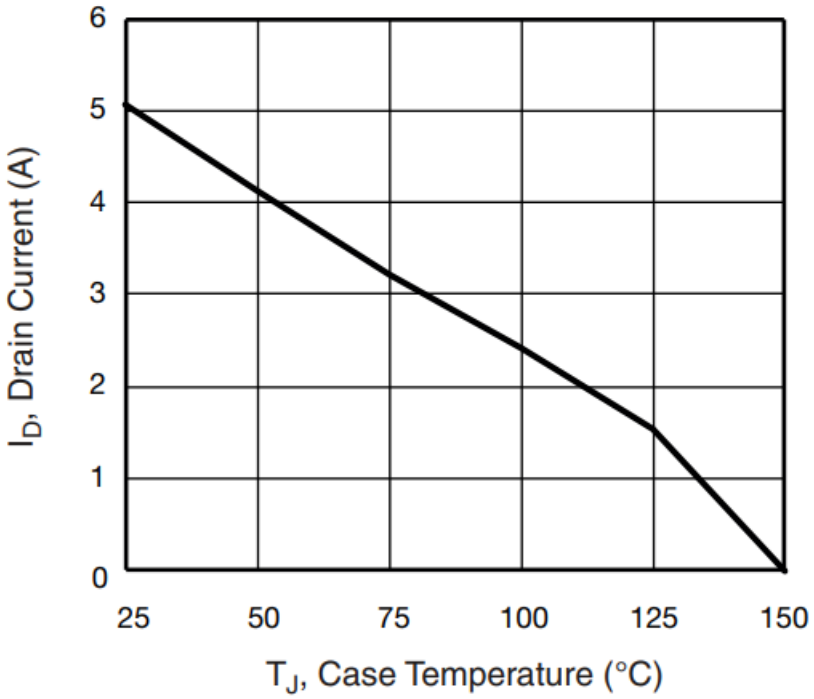


Fig. 9 - Maximum Drain Current vs. Case Temperature

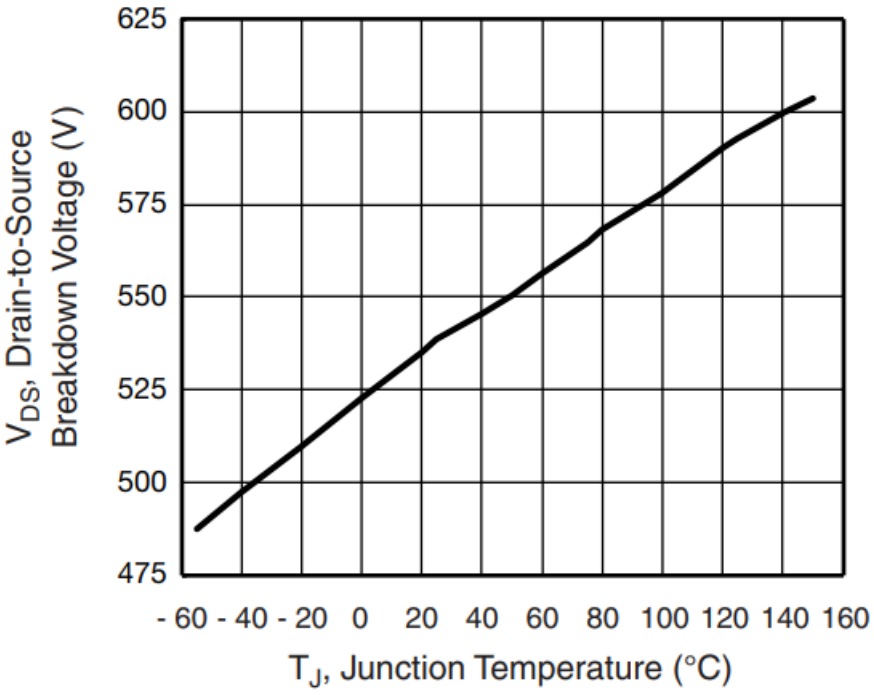


Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

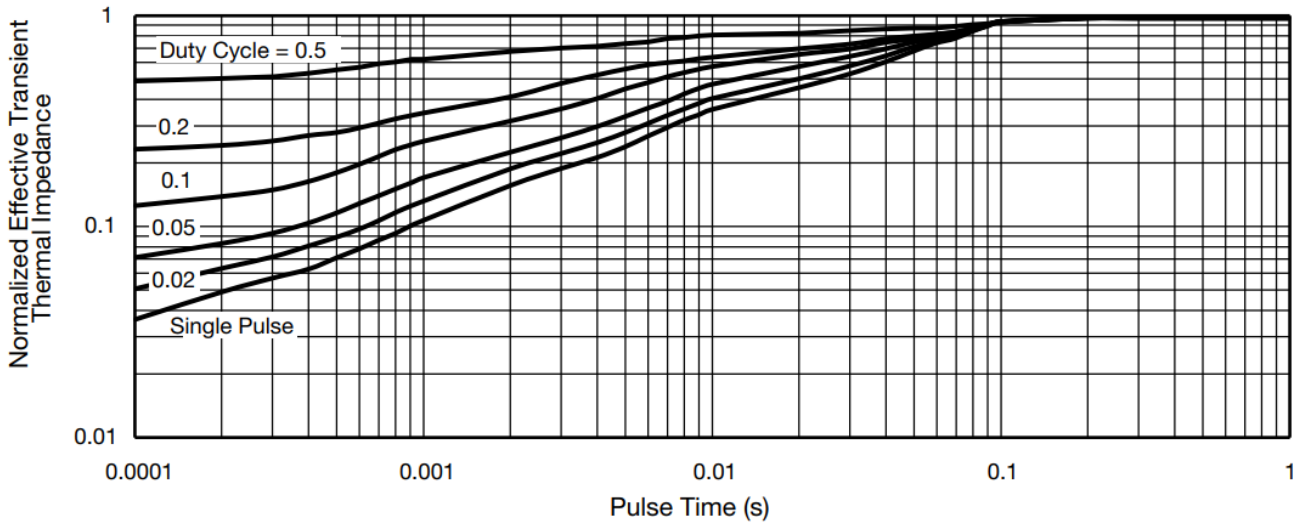


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

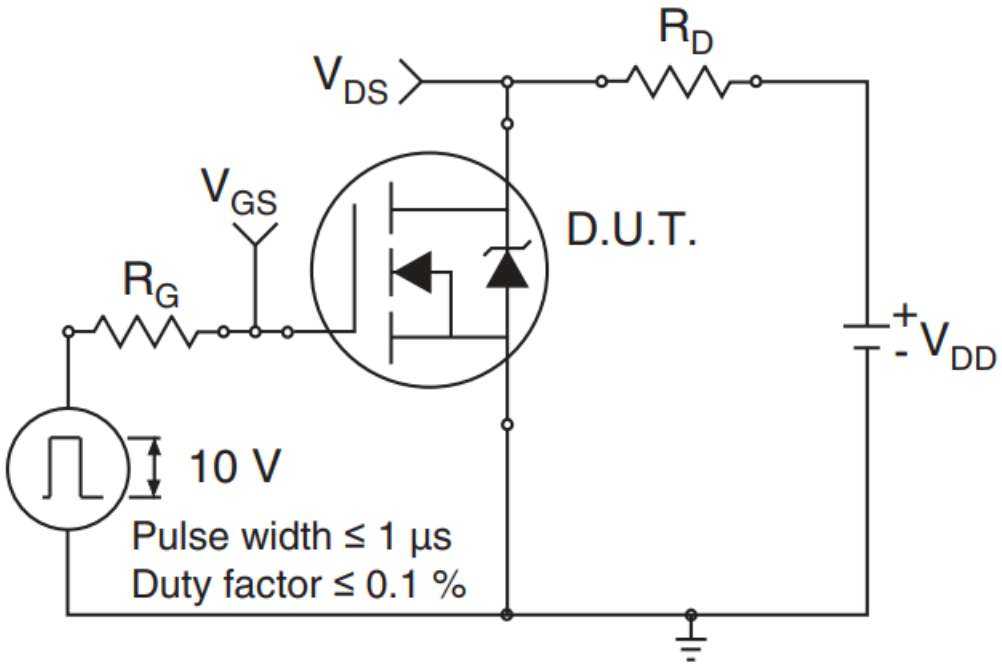


Fig. 12 - Switching Time Test Circuit

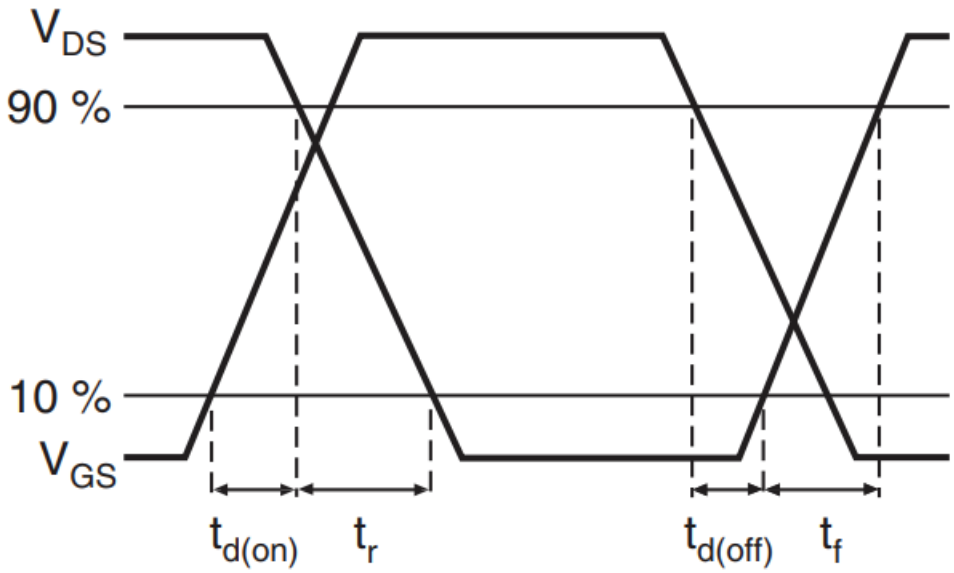


Fig. 13 - Switching Time Waveforms

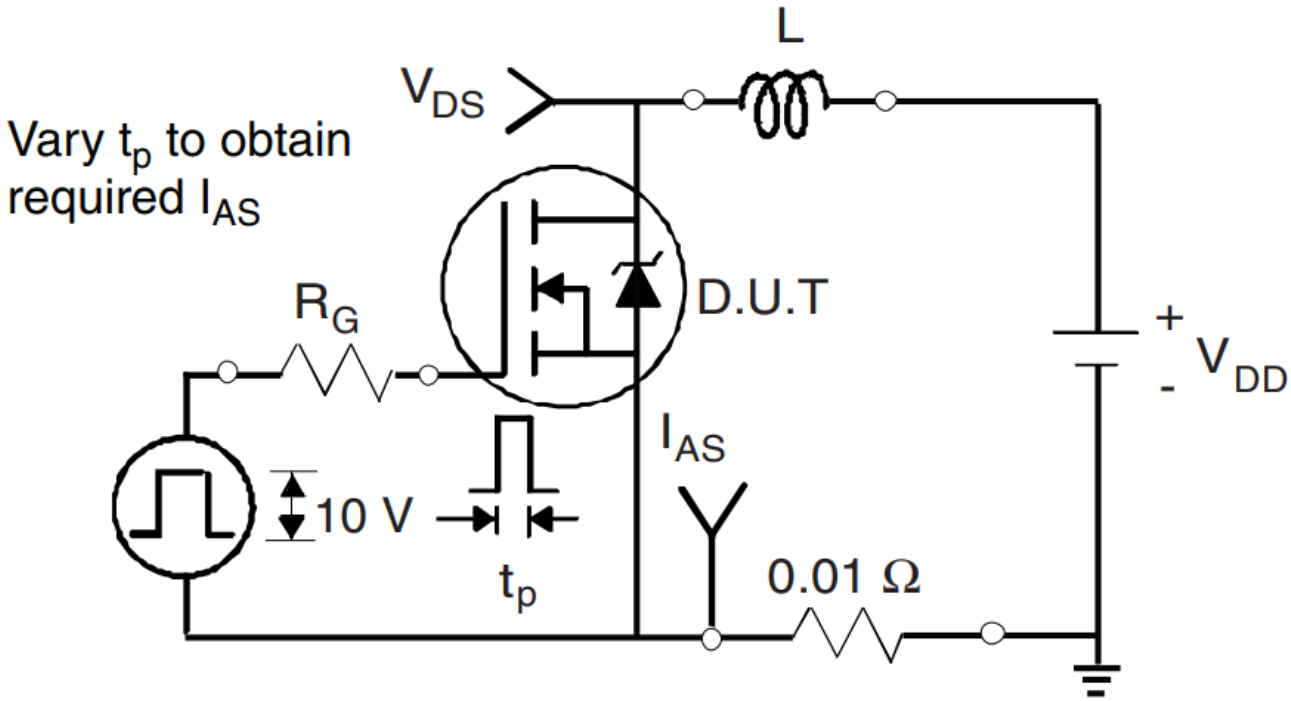


Fig. 14 - Unclamped Inductive Test Circuit

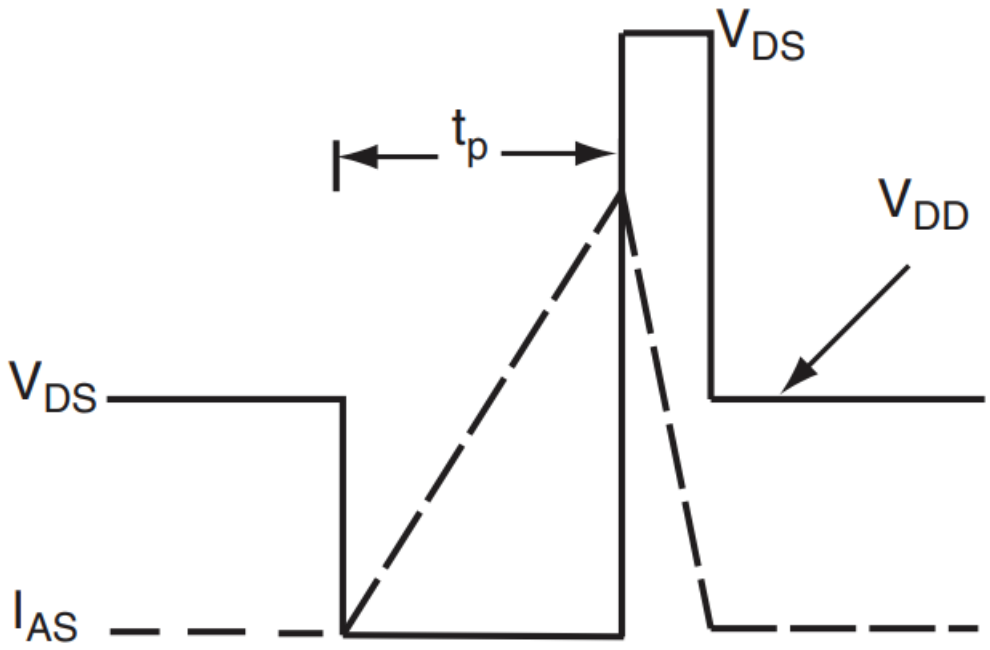


Fig. 15 - Unclamped Inductive Waveforms

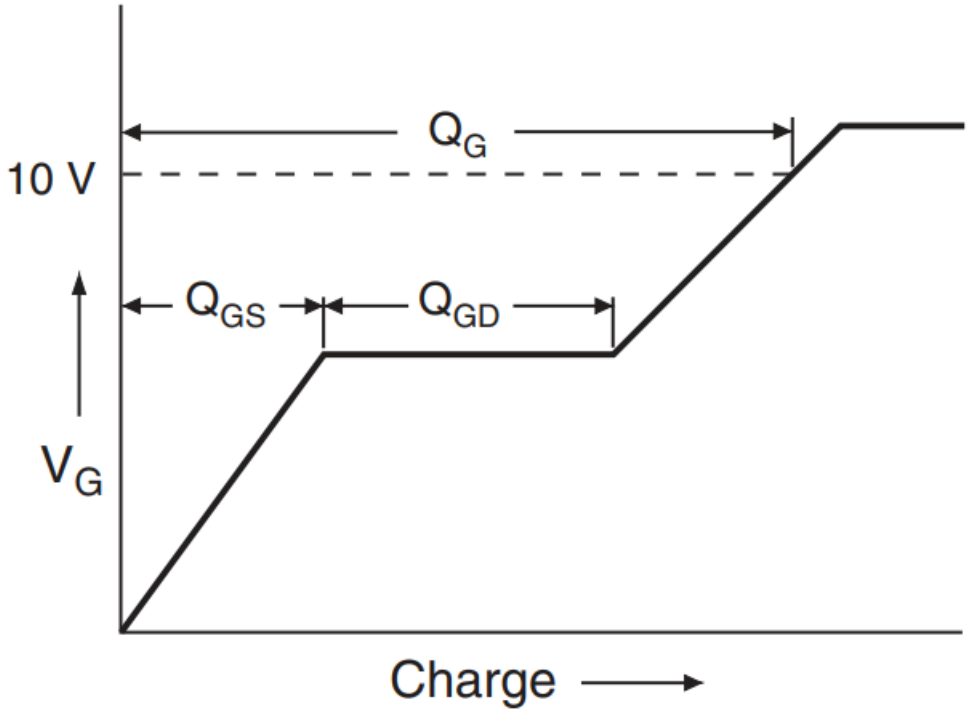


Fig. 16 - Basic Gate Charge Waveform

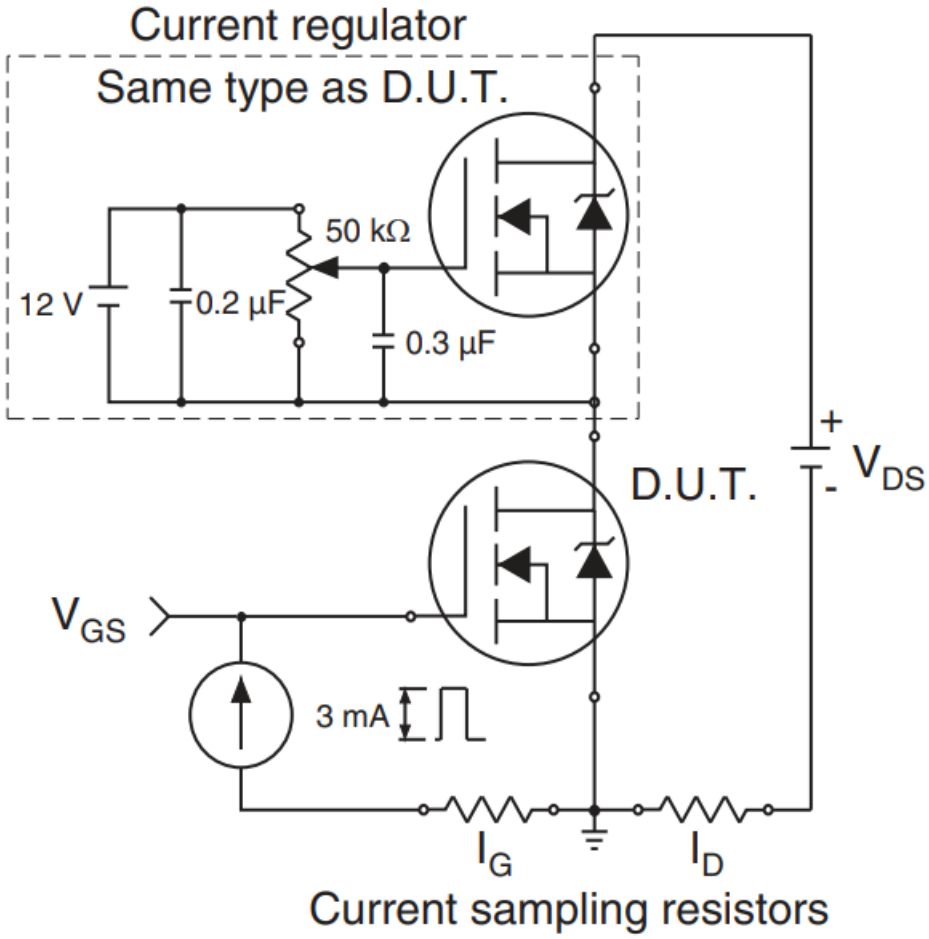
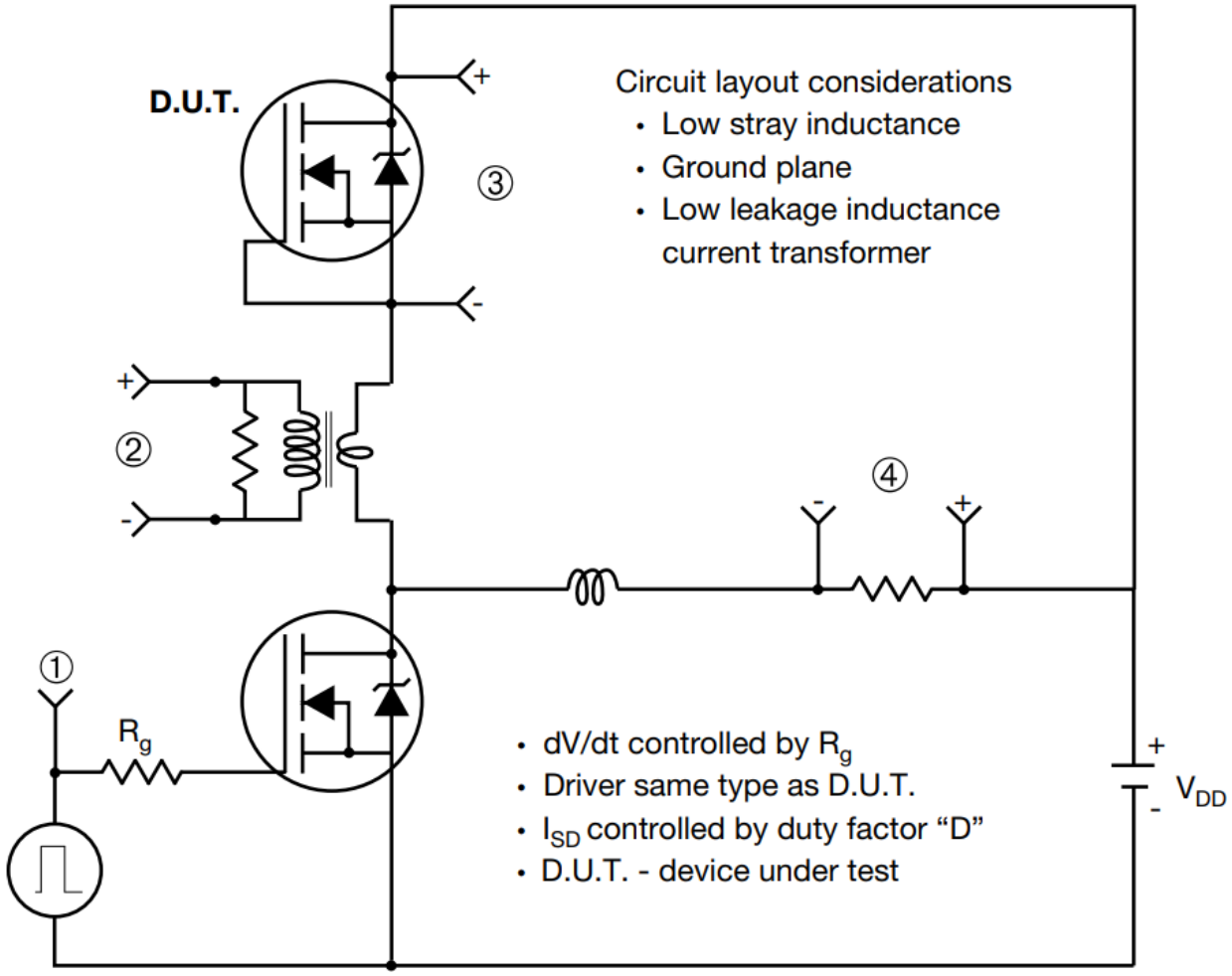
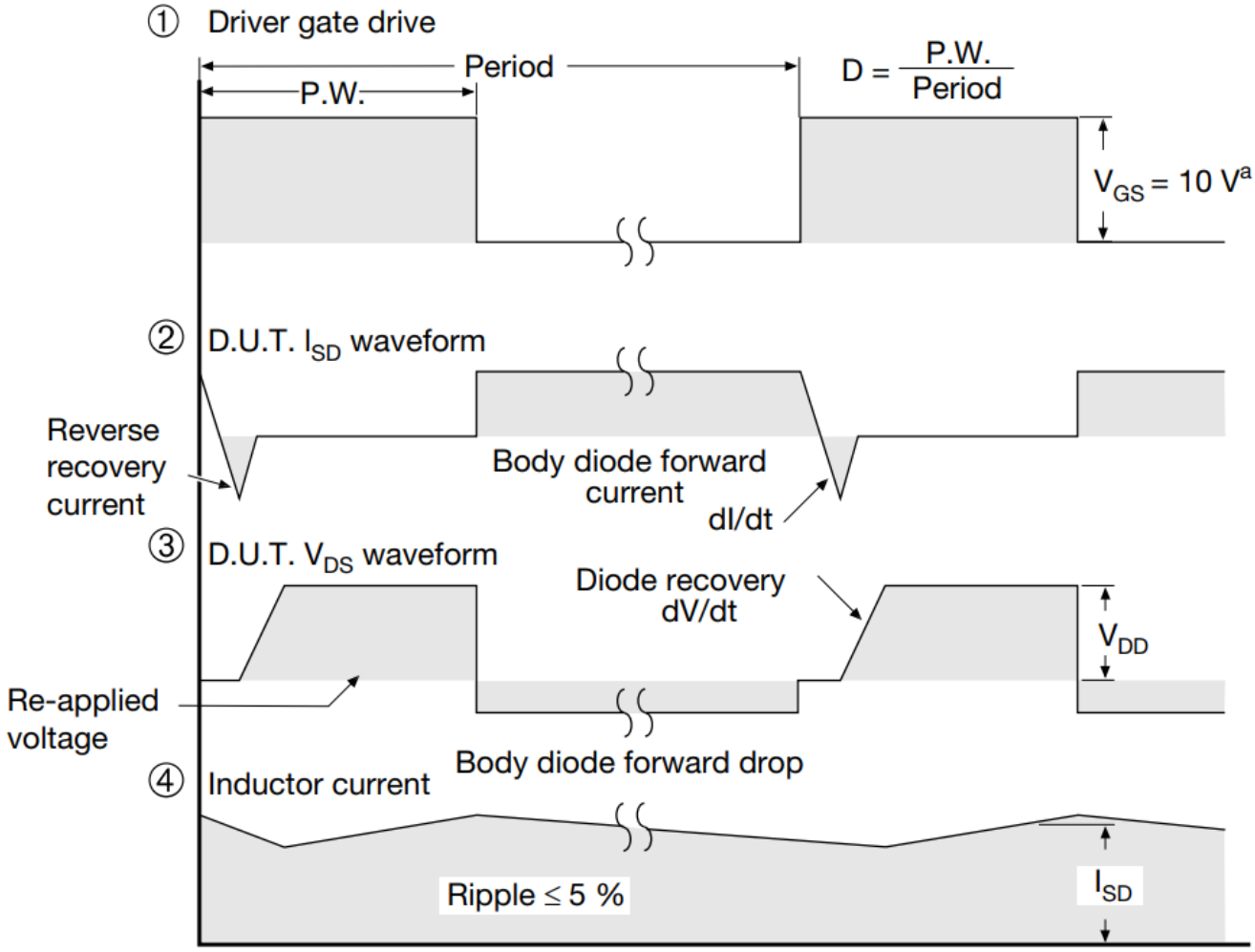


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit


D.U.T.
+
③
-
Circuit layout considerations
• Low stray inductance
• Ground plane
• Low leakage inductance current transformer
+
②
-
④
-
+
①
R_g
• dV/dt controlled by R_g
• Driver same type as D.U.T.
• I_{SD} controlled by duty factor "D"
• D.U.T. - device under test
+
-
V_{DD}



Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

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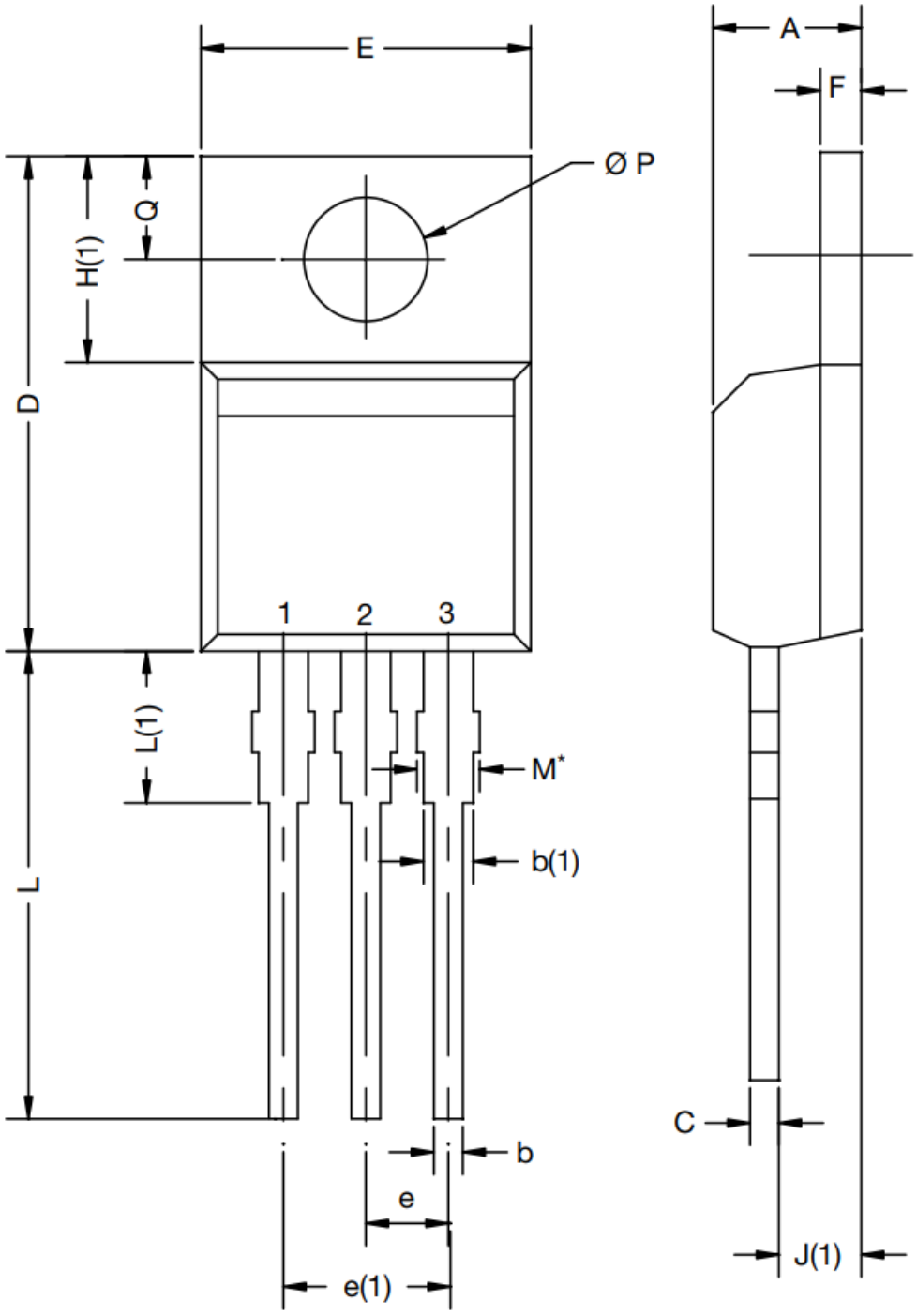
Package Information


E
Ø P
Q
H(1)
D
1
2
3
L(1)
M*
b(1)
L
b
e
e(1)
A
F
C
J(1)

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118
ECN: E21-0621-Rev. D, 04-Nov-2021 DWG: 6031				

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

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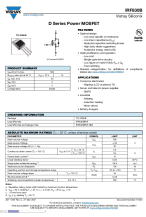	VISHAY IRF830B D Series Power MOSFET [pdf] Owner's Manual IRF830B D Series Power MOSFET, IRF830B, D Series Power MOSFET, Power MOSFET, MOSFET

References

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