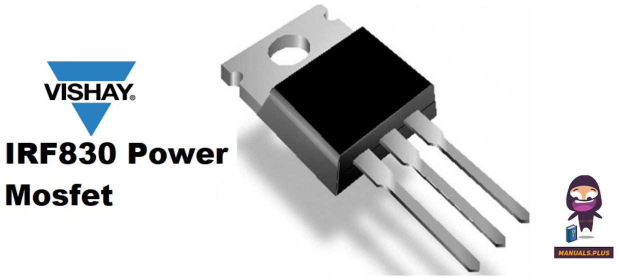

VISHAY IRF830 Power Mosfet Owner’s Manual

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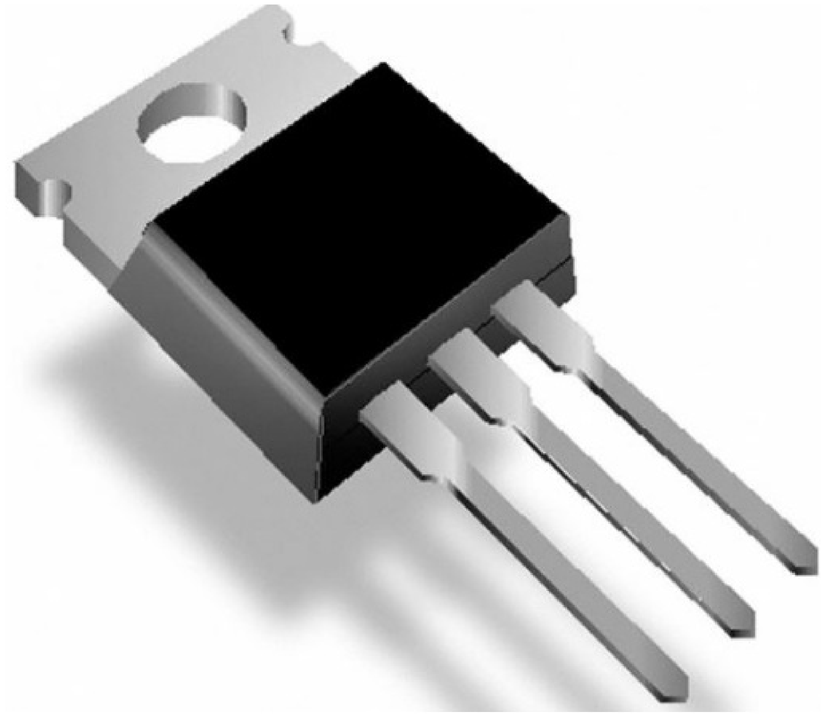


Frequently Asked Questions

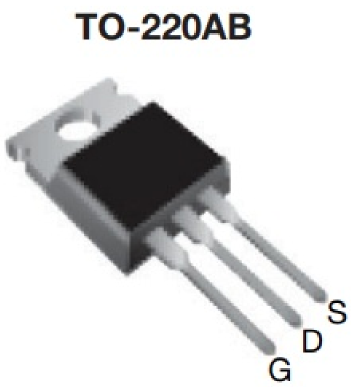
Q: Is the IRF830 RoHS compliant?

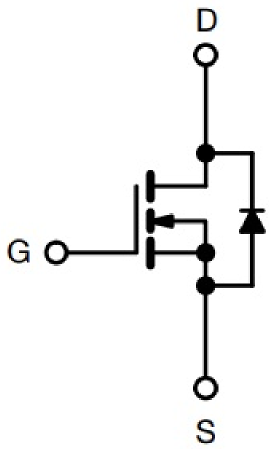
A: The datasheet provides information on RoHS-compliant and non-RoHS-compliant parts, including lead (Pb) terminations. Please refer to the datasheet for details.

Q: What are the key features of the IRF830?

A: The IRF830 offers fast switching, rugged design, low on-resistance, and cost-effectiveness.

Power MOSFET





N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated

- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see **www.vishay.com/doc?99912**

  Note

  This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY		
V_{DS} (V)	500	
RDS(on) (W)	V_{GS} = 10 V	1.5
Q_g max. (nC)	38	
Q_{gs} (nC)	5.0	
Q_{gd} (nC)	22	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF830PbF
Lead (Pb)-free and halogen-free	IRF830PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-source voltage			VDS	500	V
Gate-source voltage			VGS	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	4.5	A
		T_C = 100 °C		2.9	
Pulsed drain current a			IDM	18	
Linear derating factor				0.59	W/°C
Single pulse avalanche energy b			EAS	280	mJ
Repetitive avalanche current a			IAR	4.5	A
Repetitive avalanche energy a			EAR	7.4	mJ
Maximum power dissipation	T_C = 25 °C		P_D	74	W
Peak diode recovery dV/dt c			dV/dt	3.5	V/ns
Operating junction and storage temperature range			TJ, Tstg	-55 to +150	°C
Soldering recommendations (peak temperature) d	For 10 s			300	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. VDD = 50 V, starting TJ = 25 °C, L = 24 mH, Rg = 25 Ω, IAS = 4.5 A (see fig. 12)
- c. ISD ≤ 4.5 A, dI/dt ≤ 75 A/μs, VDD ≤ VDS, TJ ≤ 150 °C
- d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	RthJA	–	62	°C/W
Case-to-sink, flat, greased surface	RthCS	0.50	–	
Maximum junction-to-case (drain)	RthJC	–	1.7	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)	

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	VDS	V_{GS} = 0 V, I_D = 250 μA	500	–	–	V
V_{DS} temperature coefficient	DV_{DS}/T_J	Reference to 25 °C, I_D = 1 mA	–	0.61	–	V/°C
Gate-source threshold voltage	VGS(th)	V_{DS} = V_{GS}, I_D = 250 μA	2.0	–	4.0	V
Gate-source leakage	IGSS	V_{GS} = ± 20 V	–	–	± 100	nA
Zero gate voltage drain current	IDSS	V_{DS} = 500 V, V_{GS} = 0 V	–	–	25	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	–	–	250	
Drain-source on-state resistance	RDS(on)	V_{GS} = 10 V, I_D = 2.7 A b	–	–	1.5	W
Forward transconductance	gfs	V_{DS} = 50 V, I_D = 2.7 A b	2.5	–	–	S
Dynamic						
Input capacitance	Ciss	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	–	610	–	pF
Output capacitance	Coss		–	160	–	
Reverse transfer capacitance	Crss		–	68	–	
Total gate charge	Q_g	V_{GS} = 10 V, I_D = 3.1 A, V_{DS} = 400 V, see fig. 6 and 13 b	–	–	38	nC
Gate-source charge	Qgs		–	–	5.0	
Gate-drain charge	Qgd		–	–	22	
Turn-on delay Time	td(on)	V_{DD} = 250 V, I_D = 3.1 A R_g = 12 W, R_D = 79 W, see fig. 10 b	–	8.2	–	ns
Rise time	t_r		–	16	–	
Turn-off delay time	td(off)		–	42	–	
Fall time	t_f		–	16	–	
Internal drain inductance	L_D	Between lead, 6 mm (0.25″) from	–	4.5	–	

Internal source inductance	L_S	package and center of die contact	–	7.5	–	nH	
Gate input resistance	R_g	f = 1 MHz, open drain	0.5	–	2.7	W	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p – n junction diode	–	–	4.5	A	
Pulsed diode forward current a	ISM		–	–	18	A	
Body diode voltage	VSD	T_J = 25 °C, I_S = 4.5 A, V_{GS} = 0 V b	–	–	1.6	V	
Body diode reverse recovery time	trr	T_J = 25 °C, I_F = 3.1 A, dI/dt = 100 A/μs b	–	320	640	ns	
Body diode reverse recovery charge	Qrr	T_J = 25 °C, I_F = 3.1 A, dI/dt = 100 A/μs b	–	1.0	2.0	μC	
Forward turn-on time	ton	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS

(25 °C, unless otherwise noted)

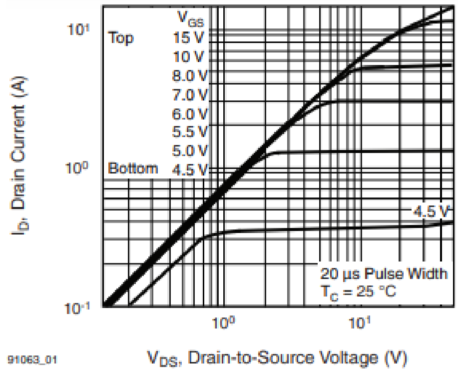


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

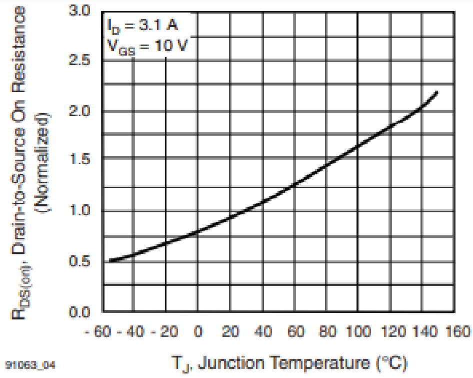


Fig. 4 - Normalized On-Resistance vs. Temperature

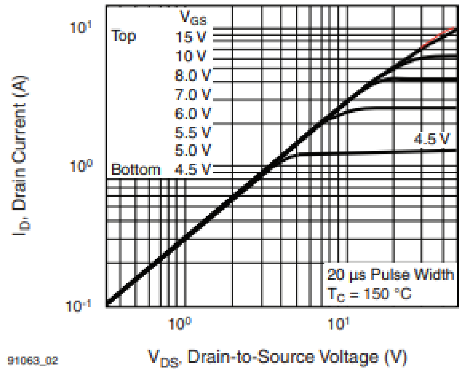


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

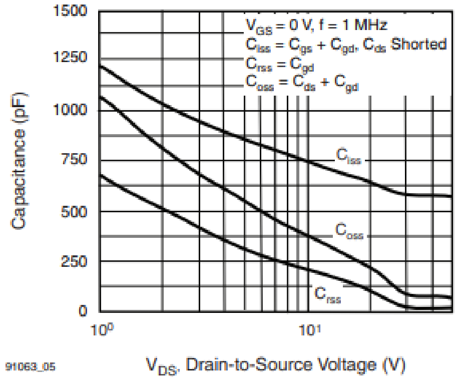


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

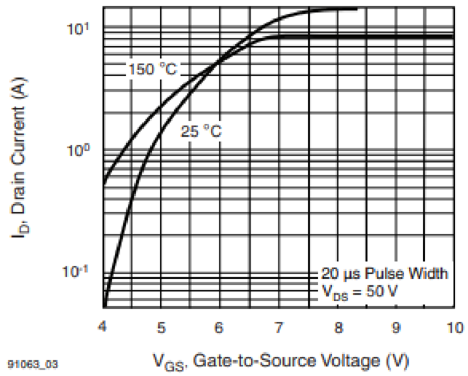


Fig. 3 - Typical Transfer Characteristics

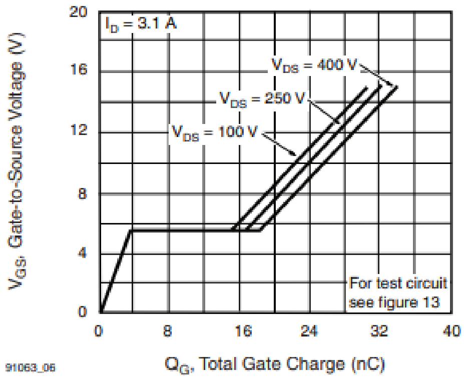


Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage

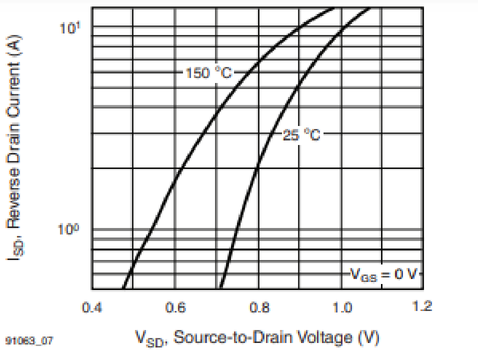


Fig. 7 - Typical Source-Drain Diode Forward Voltage

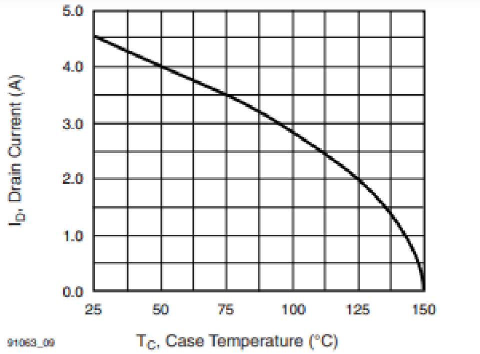


Fig. 9 - Maximum Drain Current vs. Case Temperature

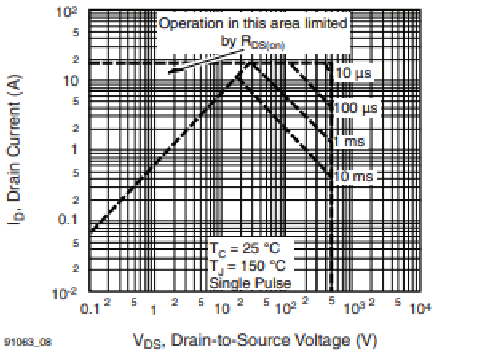


Fig. 8 - Maximum Safe Operating Area

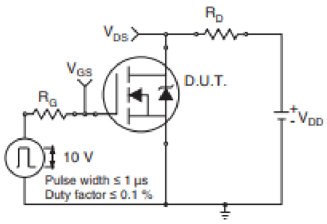


Fig. 10a - Switching Time Test Circuit

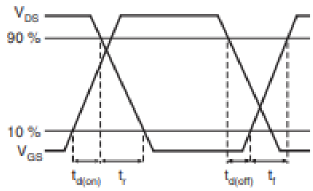


Fig. 10b - Switching Time Waveforms

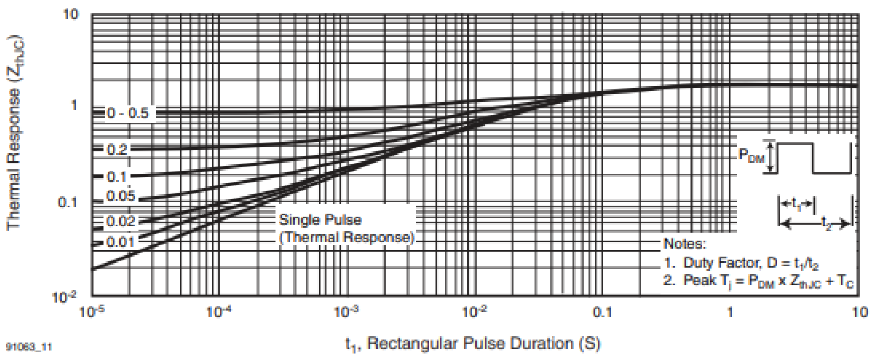


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

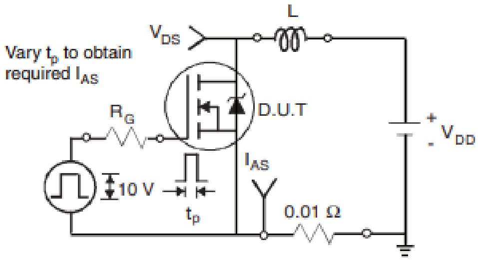


Fig. 12a - Unclamped Inductive Test Circuit

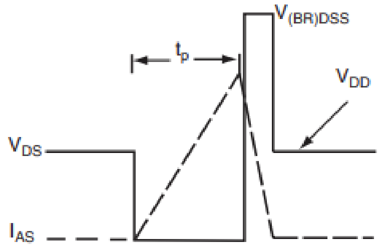


Fig. 12b - Unclamped Inductive Waveforms

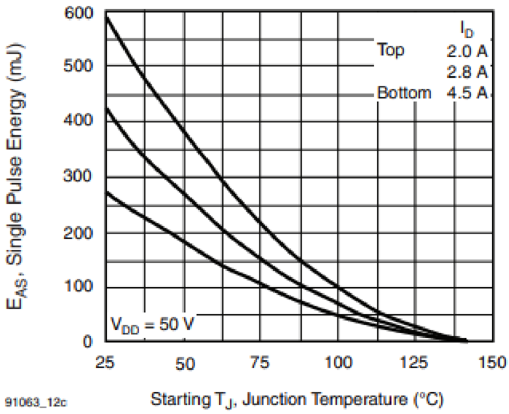


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

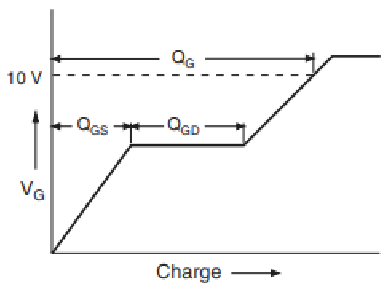


Fig. 13a - Basic Gate Charge Waveform

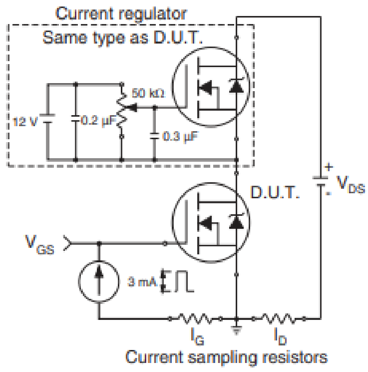


Fig. 13b - Gate Charge Test Circuit

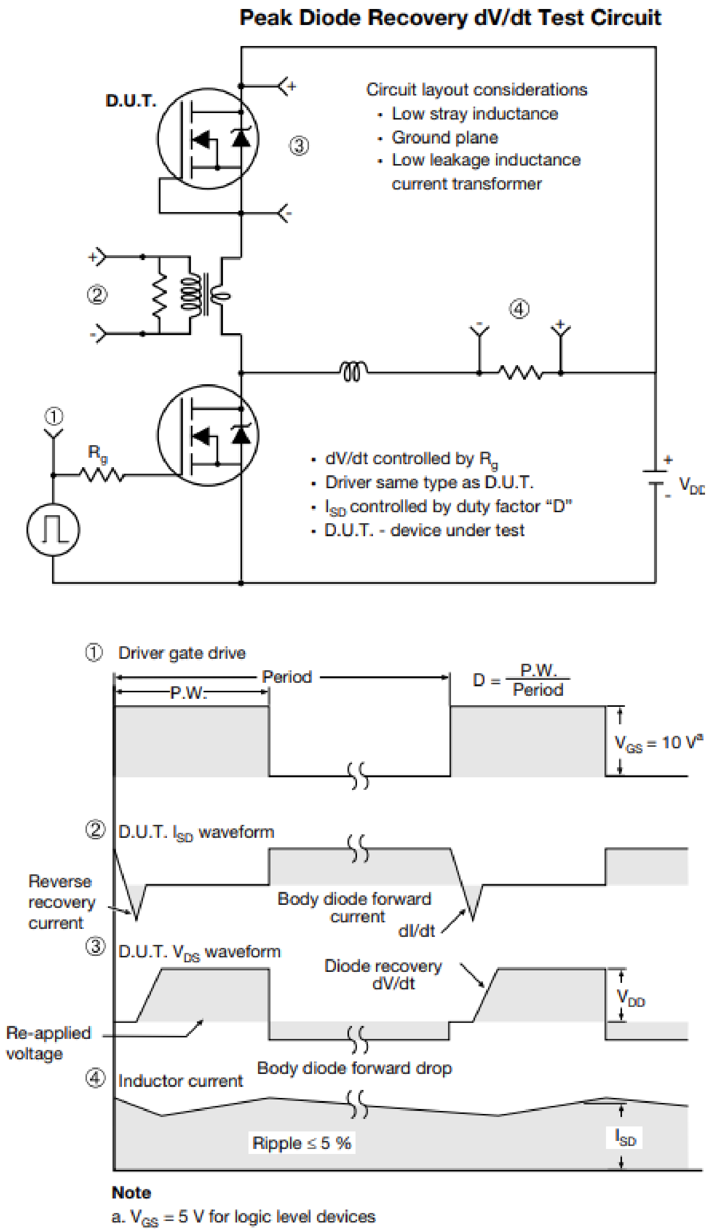


Fig. 14 - For N-Channel

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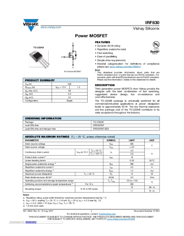	**VISHAY IRF830 Power Mosfet** [pdf] Owner's Manual IRF830, IRF830PBF, IRF830PbF, IRF830PbF-BE3, IRF830 Power Mosfet, IRF830, Power Mosf et, Mosfet

References

- **Vishay Intertechnology: Passives & Discrete Semiconductors**
- **User Manual**