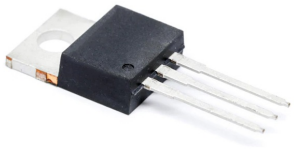
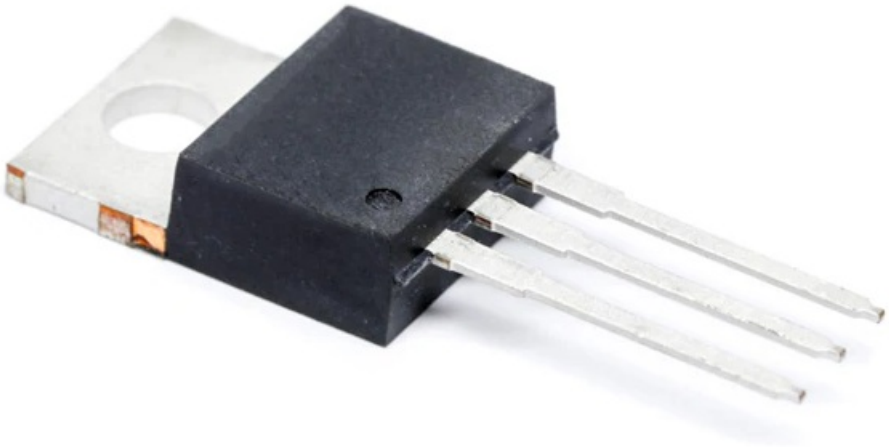


VISHAY D Series Power MOSFET Owner's Manual

Contents

VISHAY D Series Power MOSFET



Product Information

Product Name	SiHF18N50D
Brand	Vishay Siliconix
Product Type	D Series Power MOSFET
Package Type	D TO-220 FULLPAK
Channel Type	N-Channel MOSFET
Drain-Source Voltage (VDS)	550 VGS = 10 V

Product Usage Instructions

1. Make sure to handle the SiHF18N50D MOSFET with care.
2. Ensure that the MOSFET is properly connected in the circuit according to the provided pin configuration.
3. Provide a suitable gate drive circuitry to control the MOSFET's switching behavior.
4. Ensure that the drain-source voltage (VDS) does not exceed the specified maximum voltage of 550 VGS = 10 V.
5. Observe the specified maximum drain current (ID) and pulsed drain current (IDM) to prevent damage to the MOSFET.
6. Take into account the specified maximum power dissipation (PD) to avoid overheating of the MOSFET.
7. Operate the MOSFET within the specified temperature range of -55°C to +150°C.
8. Follow the recommended soldering recommendations, including peak temperature and mounting torque, for proper installation. Refer to the provided thermal resistance ratings (RthJA, RthJC) for understanding the heat dissipation characteristics of the
   MOSFET.
9. Refer to the datasheet for detailed electrical characteristics and performance specifications of the SiHF18N50D MOSFET.
10. For any technical questions or assistance, contact hvm@vishay.com.

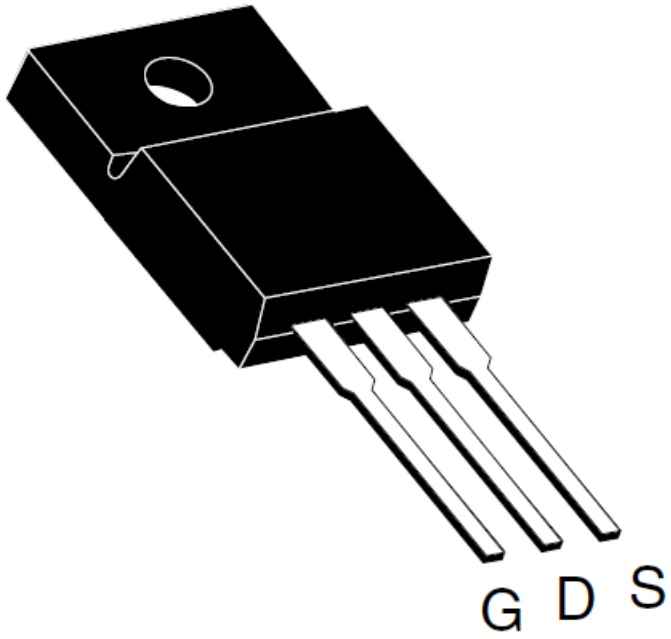
FEATURES

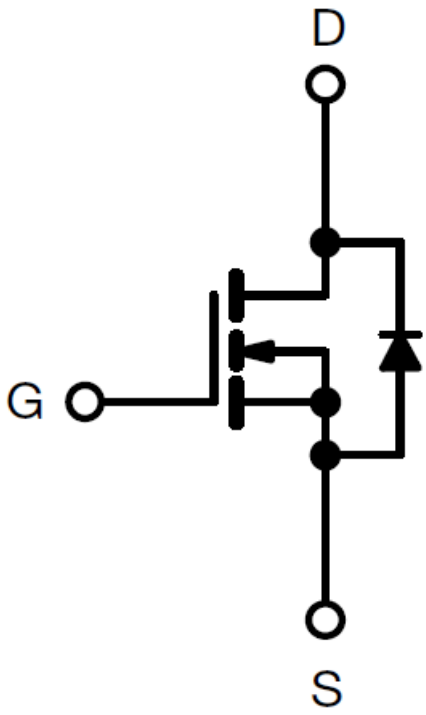
- Optimal design
  - Low area specific on-resistance
  - Low input capacitance (Ciss)
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): Ron x Qg
  - Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

- This datasheet provides information about parts that are
- RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant.
- Please see the information / tables in this datasheet for details

TO-220 FULLPAK





N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. (W) at 25 °C	V_{GS} = 10 V	0.28
Q_g max. (nC)	76	
Q_{gs} (nC)	11	
Q_{gd} (nC)	17	
Configuration	Single	

APPLICATIONS

- Consumer electronics
  - Displays (LCD or Plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- Battery chargers

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF18N50D-E3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-source voltage			VDS	500	V
Gate-source voltage			VGS	± 30	
Gate-source voltage AC (f > 1 Hz)				30	
Continuous drain current (T_J = 150 °C) e	V_{GS} at 10 V	T_C = 25 °C	I_D	18	A
		T_C = 100 °C		11	
Pulsed drain current a			IDM	53	
Linear derating factor				0.3	W/°C
Single pulse avalanche energy b			EAS	115	mJ
Maximum power dissipation			P_D	39	W
Operating junction and storage temperature range			TJ, Tstg	-55 to +150	°C
Drain-source voltage slope	T_J = 125 °C		dV/dt	24	V/ns
Reverse diode dV/dt d				0.4	
Soldering recommendations (peak temperature) c	For 10 s			300	°C
Mounting torque	M3 screw			0.6	Nm

THERMAL RESISTANCE RATINGS

PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	RthJA	–	65	°C/W
Maximum junction-to-case (drain)	RthJC	–	3.2	

SPECIFICATIONS

(TJ = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	VDS	V_{GS} = 0 V, I_D = 250 µA		500	–	–	V
V_{DS} temperature coefficient	DV_{DS}/T_J	Reference to 25 °C, I_D = 250 µA		–	0.58	–	V/°C
Gate threshold voltage (N)	VGS(th)	V_{DS} = V_{GS}, I_D = 250 µA		3.0	–	5.0	V
Gate-source leakage	IGSS	V_{GS} = ± 30 V		–	–	± 100	nA
Zero gate voltage drain current	IDSS	V_{DS} = 500 V, V_{GS} = 0 V		–	–	1	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C		–	–	10	
Drain-source on-state resistance	RDS(on)	V_{GS} = 10 V	I_D = 9 A	–	0.23	0.28	W
Forward transconductance	gfs	V_{DS} = 50 V, I_D = 9 A		–	6.4	–	S
Dynamic							
Input capacitance	Ciss	V_{GS} = 0 V, V_{DS} = 100 V, f = 1.0 MHz		–	1500	–	pF
Output capacitance	Coss			–	131	–	
Reverse transfer capacitance	Crss			–	14	–	
Effective output capacitance, energy related a	Co(er)	V_{GS} = 0 V, V_{DS} = 0 V to 400 V		–	113	–	
Effective output capacitance, time related b	Co(tr)			–	164	–	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 9 A, V_{DS} = 400 V	–	38	76	nC
Gate-source charge	Qgs			–	11	–	
Gate-drain charge	Qgd			–	17	–	
Turn-on delay time	td(on)	V_{DD} = 400 V, I_D = 9 A, V_{GS} = 10 V, R_g = 9.1 W		–	19	38	ns
Rise time	t_r			–	36	72	
Turn-off delay time	td(off)			–	36	72	
Fall time	t_f			–	30	60	
Gate input resistance	R_g	f = 1 MHz, open drain		–	1.7	–	W
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse G D		–	–	18	A

Pulsed diode forward current	ISM	P – N junction diode S	–	–	72	
Diode forward voltage	VSD	T_J = 25 °C, I_S = 9 A, V_{GS} = 0 V	–	–	1.2	V
Reverse recovery time	trr	T_J = 25 °C, I_F = I_S = 9 A, dI/dt = 100 A/μs, V_R = 20 V	–	354	–	ns
Reverse recovery charge	Qrr		–	3.9	–	μC
Reverse recovery current	IRRM		–	21	–	A

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- VDD = 50 V, starting TJ = 25 °C, L = 2.3 mH, Rg = 25 , IAS = 10 A
- 1.6 mm from case
- ISD ID, starting TJ = 25 °C e. Limited by maximum junction temperature

Notes

- Coss(er) is a fixed capacitance that gives the same energy as Coss while VDS is rising from 0 % to 80 % VDSS
- Coss(tr) is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 % to 80 % VDSS

TYPICAL CHARACTERISTICS

(25 °C, unless otherwise noted)

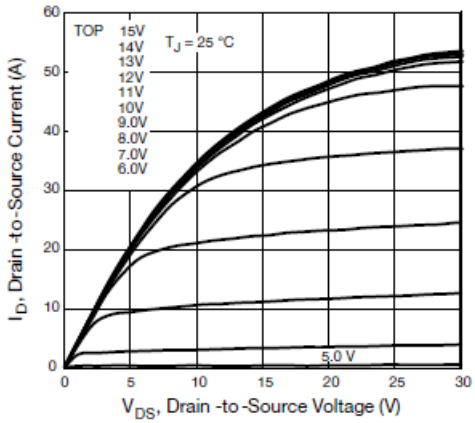


Fig. 1 - Typical Output Characteristics

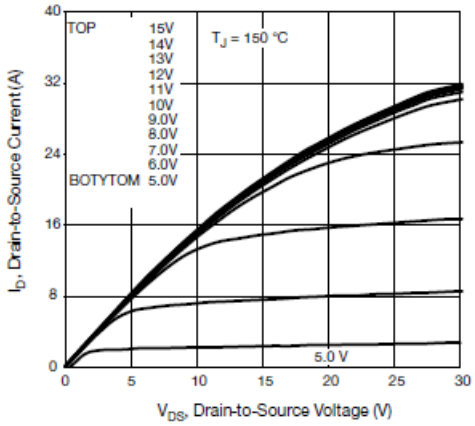


Fig. 2 - Typical Output Characteristics

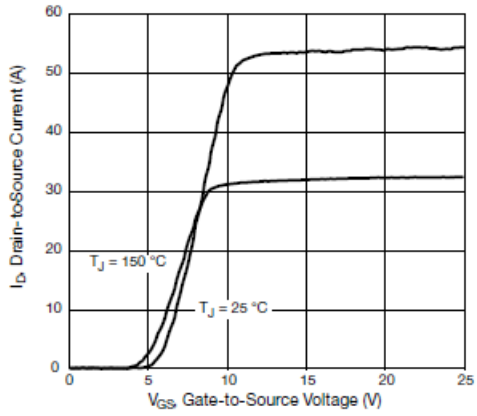


Fig. 3 - Typical Transfer Characteristics

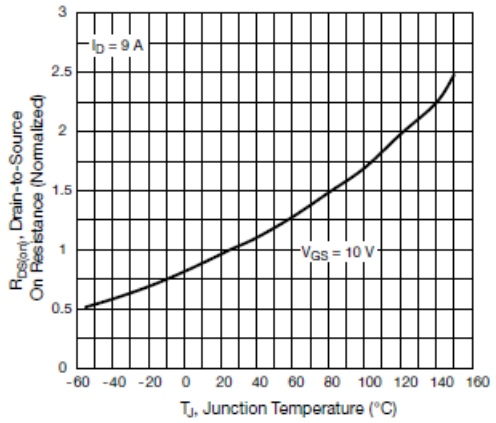


Fig. 4 - Normalized On-Resistance vs. Temperature

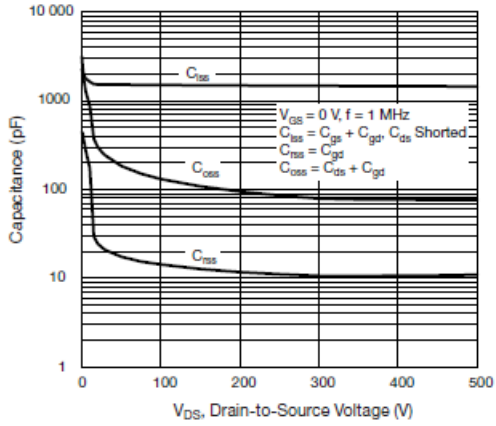


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

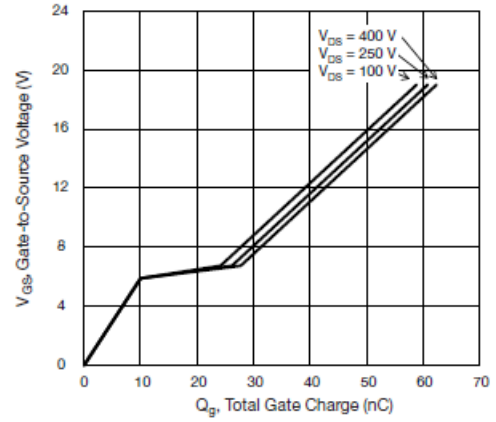


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

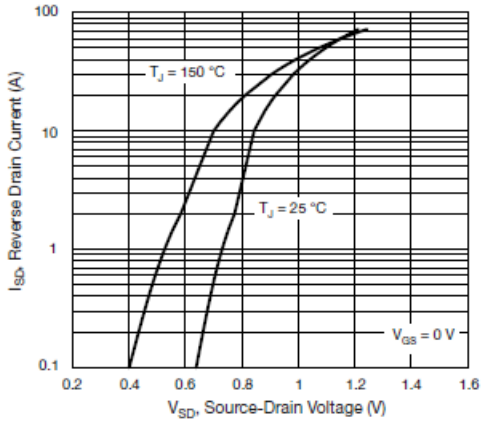


Fig. 7 - Typical Source-Drain Diode Forward Voltage

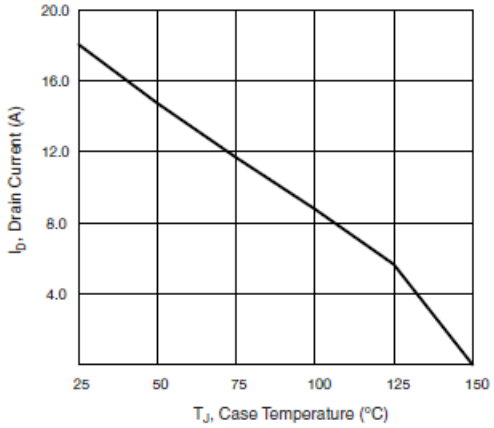


Fig. 9 - Maximum Drain Current vs. Case Temperature

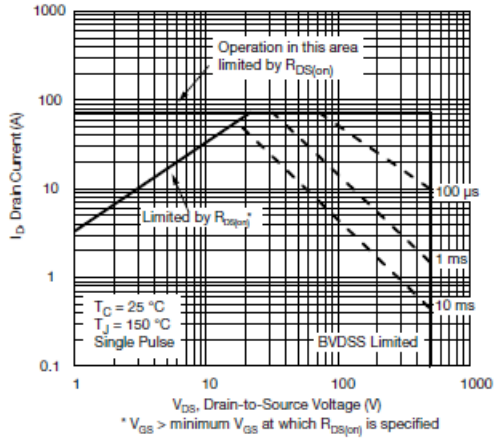


Fig. 8 - Maximum Safe Operating Area

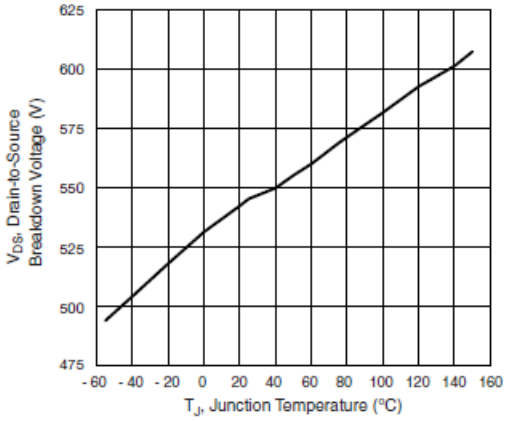


Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

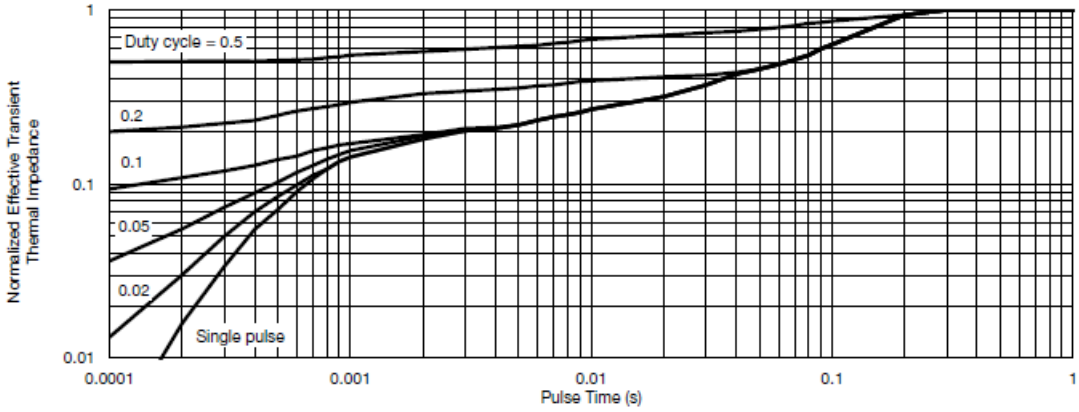


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

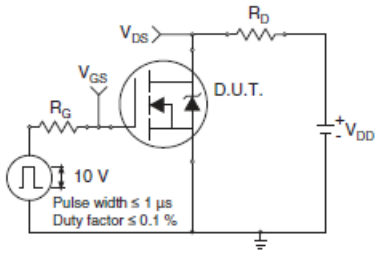


Fig. 12 - Switching Time Test Circuit

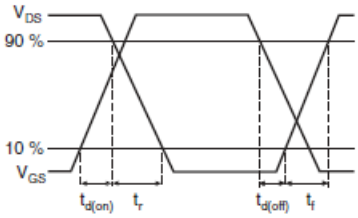


Fig. 13 - Switching Time Waveforms

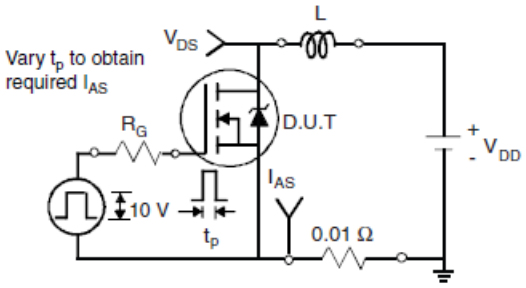


Fig. 14 - Unclamped Inductive Test Circuit

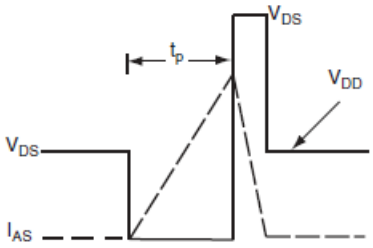


Fig. 15 - Unclamped Inductive Waveforms

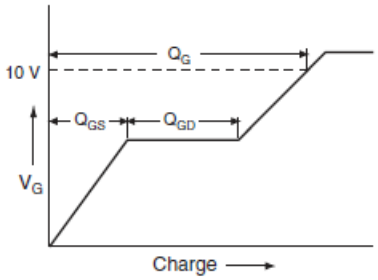


Fig. 16 - Basic Gate Charge Waveform

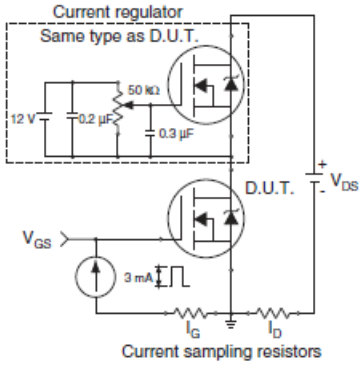


Fig. 17 - Gate Charge Test Circuit

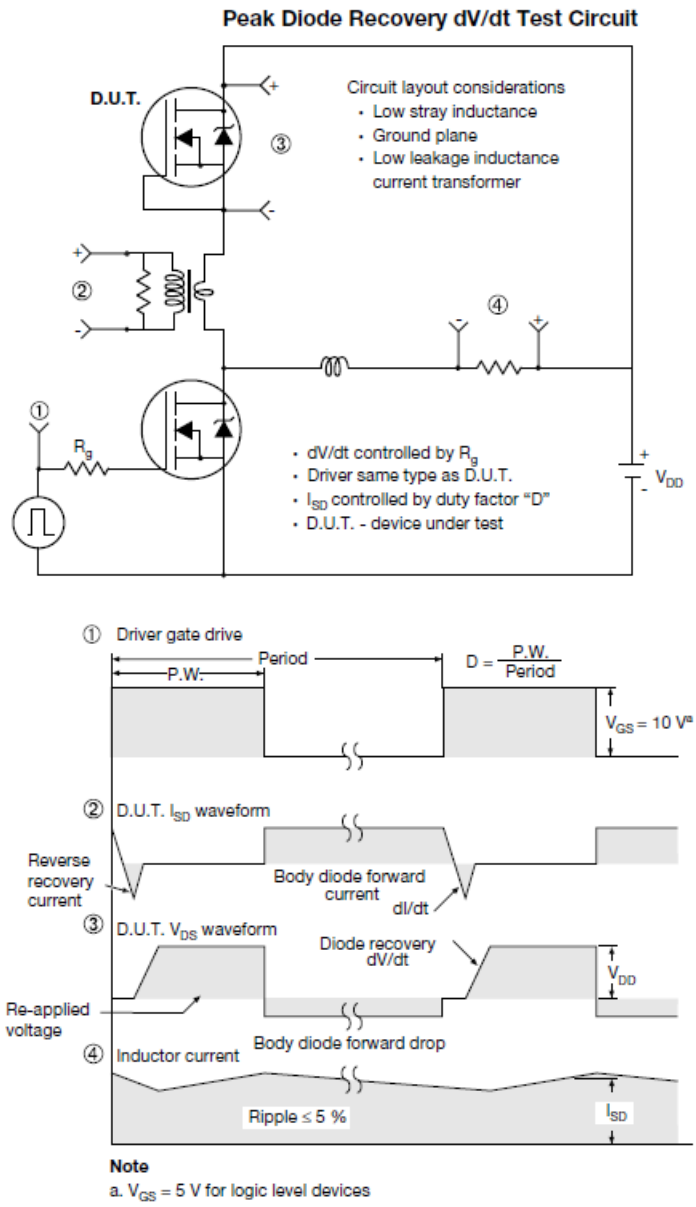
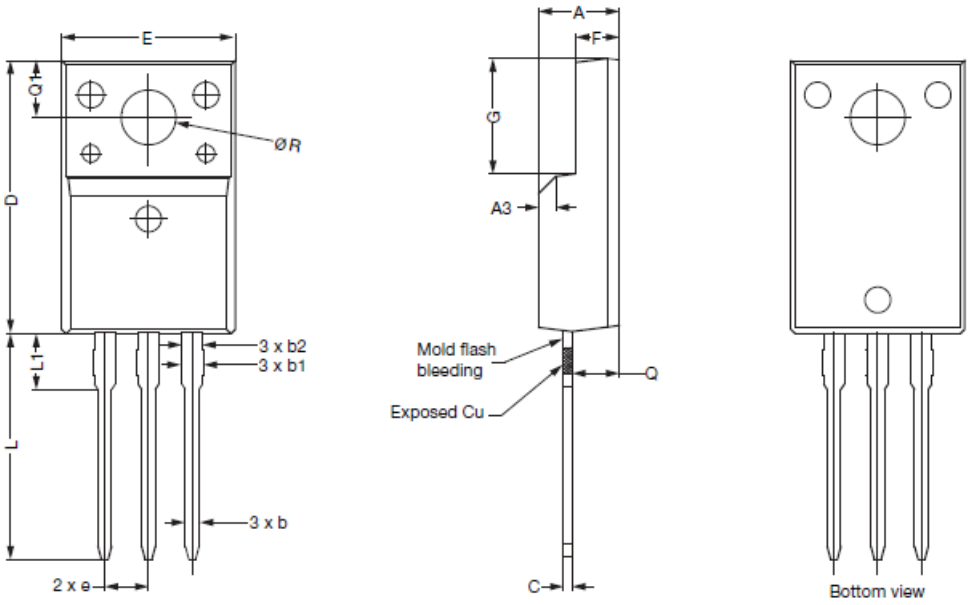


Fig. 18 - For N-Channel

TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



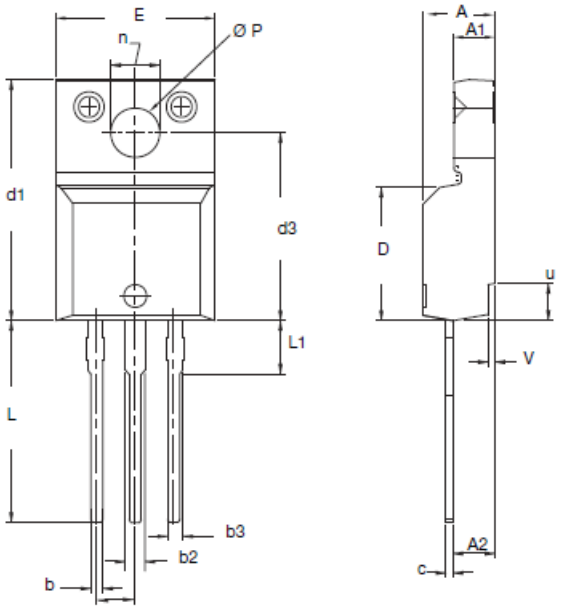
	MILLIMETERS		
DIM.	**MIN.**	**NOM.**	**MAX.**
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet Cpk > 1.33
4. All dimensions include burrs and plating thickness

5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

OPTION 2: FACILITY CODE = Y



	MILLIMETERS		INCHES	
DIM.	**MIN.**	**MAX.**	**MIN.**	**MAX.**
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020
ECN: E19-0180-Rev. D, 08-Apr-2019 DWG: 5972				

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet Cpk > 1.33
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

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Revision: 01-Jan-2023
Document Number: 91000
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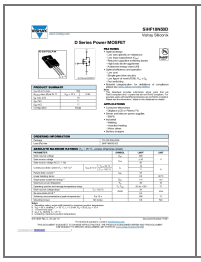	**VISHAY D Series Power MOSFET** [pdf] Owner's Manual SiHF18N50D, D Series Power MOSFET, Power MOSFET, MOSFET

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