

u-blox LARA-R2/R6 Migration Guide User Guide

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u-blox LARA-R2/R6 Migration



Abstract

This document provides hardware guidelines to migrate from u-blox LARA-R2 series region-specific LTE Cat 1 / 3G / 2G modules to LARA-R6 series global and multi-region LTE Cat 1 / 3G / 2G modules, all which are designed in the compact LARA form factor.

Document information

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Product statu	Corresponding conter	nt status							
Functional sa mple	Draft	For functional testing. Revised and supplementary data will be publis hed later.							
In developme nt / Prototype	Objective specification	Target values. Revised and supplementary data will be published late r.							
Engineering s ample	Advance information	Data based on early testing. Revised and supplementary data will be published later.							
Initial product ion	Early production infor mation	Data from product verification. Revised and supplementary data may be published later.							
Mass product ion / End of life	Production information	Document contains the final product specification.							

This document applies to the following products:

Product name	Ordering code	Product Status
LARA-R202	LARA-R202-02B	End of life
	LARA-R202-82B	End of life
	LARA-R202-03B	End of life
LARA-R203	LARA-R203-02B	End of life
	LARA-R203-03B	End of life
LARA-R204	LARA-R204-02B	End of life
LARA-R211	LARA-R211-02B	End of life
	LARA-R211-03B	End of life
LARA-R220	LARA-R220-62B	End of life
LARA-R280	LARA-R280-02B	End of life
LARA-R281	LARA-R281-02B	End of life
LARA-R6001	LARA-R6001-00B	Prototype
LARA-R6001D	LARA-R6001D-00B	Initial production
LARA-R6401	LARA-R6401-00B	Prototype
LARA-R6401D	LARA-R6401D-00B	Engineering sample
LARA-R6801	LARA-R6801-00B	Functional sample

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LARA-R2 / LARA-R6 modules description

- The u-blox LARA-R2 series comprises single-mode and multi-mode modules supporting LTE Cat 1 in FDD multi-band, 3G UMTS/HSPA in FDD multi-band, 2G GSM/GPRS/EGPRS in dual-band, providing the ideal solution for region-specific coverage.
- The u-blox LARA-R6 series comprises single-mode and multi-mode modules supporting LTE Cat 1 in FDD / TDD multi-band, 3G UMTS/HSPA in FDD multi-band, 2G GSM/GPRS/EGPRS in quad-band, providing the ideal solution for global and multi-regional coverage.
- All the LARA-R2 and LARA-R6 series modules are available in the same small LARA LGA form-factor (26.0 x 24.0 mm, 100-pin), easy to integrate in compact designs.
- LARA series modules are form-factor compatible with the u-blox SARA, LISA and TOBY cellular module families, facilitating a seamless drop-in migration from other u-blox LPWA, GSM/GPRS, CDMA, UMTS/HSPA and LTE modules.
- **Table 1** summarizes the main features and interfaces of LARA-R2 and LARA-R6 series modules. Some features are not supported by older product versions of the corresponding LARA-R2 series product variant. For more details, see LARA-R2 series data sheet [1].

M o d el	R e g i o n	1		Aco		Po	sitio	onir	ng	Int	terfa	aces	3		Fe	atu	res												
		L T E F D D b a n d s	L T E T D D b a n d s	UMTS/HSPAFDDbands	GSM/GPRS/EGPRSbands	IntegratedGNSSreceiver	E xt e r n al G N S S c o n tr ol	A s si s t N o w S o ft w a r e	C el IL o c a t e ®	C A R T	U S B 2 . 0	1 2 C	G P I O s	D i g it a l a u d i o	V o L T E	C S F B	R x D iv e r si t y	DualstackIPv4/IPv6	T C P I P , U D P / I P , H T T P / F T P	T S L / D T L S	M Q T T	L W M 2 M	FOAT/FOTA/uFOTA	D e vi c e a n d D a t a S e c u ri t y	3 G P P P o w e r S a vi n g M o d e	e D R X	L a s t g a s p	N e t w o r k i n d ic a ti o n	A n e n n a a n d e e e c ic n

L A R A - R 2 2	L A R A - R 2 1	L A R A - R 2 0 4	L A R A - R 2 0 3	L A R A - R 2 0 2
J a p a n	E M E A	N o rt h A m e ri c a	N o rt h A m e ri c a	N o rt h A m e ri c a
1,1	3 , 7 , 2 0	4,-	2,4	2,4,5,12
19		13	1,12	
				2, 5
	D u al			
•	•		•	•
•	•		•	•
•	•		•	•
1	2	1	2	2
1	1	1	1	1
1	1	1	1	1
9	9	9	9	9
	•		•	•
	•		•	•
	•			•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•

L A R A - R 6 0 0 1	L A R A - R 2 8 1	L A R A - R 2 8
G lo b al	E M E A	A P A C
1, 2, 3, 4, 5, 7, 8 12, 13, 18, 19 20, 26, 28	1 , 3 , 8 2 0 , 2 8	3,8,28
3 8 , 3 9 4 0 , 4 1		
1, 2 5, 8	1	1
Q u a d		
•	•	•
•	•	•
•	•	•
2	1	1
1	1	1
1	1	1
9	9	9
•	•	•
•		
•	•	•
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0		
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LARA - R6001D	G lo b al	1 2 3 4 5 7 8 12 13 18 19 20 26 28	3 8 , 3 9 4 0 , 4 1	1, 2 5, 8	Q u a d	•	•	•	2	1	1	9				•	•	•	•		•		0			•	
L A R A - R 6 4 0	N o rt h A m e ri c a	2, ² 4 66		12,13	3,1	•	•	•	2	1	1	9	•	•	•	•	•	•	•	•	•	•	0	•	•	•	•
L A R A - R 6 4 0 1 D	N o rt h A m e ri c a	2, ² 4 66		12,13	3,1	•	•	•	2	1	1	9			•	•	•	•	•	•	•	•	0	•	•	•	•

L A R A - R 6 8 0 1	M ul ti R e gi o n	1 , 2 , 3 , 4 , 5 , 7 , 8 1 8 , 1 9 , 2 0 , 2 6 , 2 8		1, 2 5, 8	Quad		•	•	•	2	1	1	9	•	•	•	•	•	•	•	•	•	•	•	0	•	•	•		
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Table 1: LARA-R2 and LARA-R6 series main features summary (● = supported, ○ = planned)

- LARA-R2 series region-specific LTE Cat 1 / 3G / 2G modules:
 - LARA-R202, designed mainly for operation in America, supporting four LTE Cat 1 FDD bands plus two
 3G bands
 - LARA-R203, designed for operation in North America, supporting three LTE Cat 1 FDD bands
 - LARA-R204, designed for operation in USA, supporting two Verizon LTE Cat 1 FDD bands
 - LARA-R211, designed mainly for operation in EMEA, supporting three LTE Cat 1 FDD bands plus two 2G bands
 - LARA-R220, designed for operation in Japan, supporting two DoCoMo LTE Cat 1 FDD bands
 - LARA-R280, designed mainly for operation in APAC, supporting three LTE Cat 1 FDD bands plus one 3G band
 - LARA-R281, designed mainly for operation in EMEA, supporting five LTE Cat 1 FDD bands plus one 3G band

LARA-R6 series global and multi-region LTE Cat 1 / 3G / 2G modules:

- LARA-R6001, designed for world-wide operation, supporting eighteen LTE Cat 1 FDD / TDD bands plus four 3G bands and four 2G bands for global coverage
- LARA-R6001D, data-only variant of LARA-R6001. Designed for world-wide operation, supporting eighteen LTE Cat 1 FDD / TDD bands plus four 3G bands and four 2G bands for global coverage

- LARA-R6401, designed mainly for operation in America, supporting eight LTE Cat 1 FDD bands
- LARA-R6401D, data-only varaint of LARA-R6401. Designed mainly for operation in America, supporting eight LTE Cat 1 FDD bands
- LARA-R6801, designed for multi-regional operation, in EMEA, APAC, Japan and Latin America, supporting twelve LTE Cat 1 FDD bands plus four 3G bands and four 2G bands
- Table 2 summarizes the LTE, 3G and 2G characteristics of LARA-R2 and LARA-R6 modules.

4G LTE	3G UMTS/HSDPA/HSUPA 1	2G GSM/GPRS/EDGE 2
Long Term Evolution (LTE) Evolved UTRA (E-UTRA) Frequency Division Duplex (FDD) Time Division Duplex (TDD)3 DL Rx diversity	High Speed Packet Access (HSPA) UMTS Terrestrial Radio Access (UTR A) Frequency Division Duplex (FDD) DL Rx diversity	Enhanced Data rate GSM Evolution (E DGE) GSM EGPRS Radio Access (GE RA) Time Division Multiple Access (TDMA) DL Advanced Rx Performance Phase 1
LTE Power Class Power Class 3 (23 dBm)	UMTS/HSDPA/HSUPA Power Class Class 3 (24 dBm)	GSM/GPRS (GMSK) Power Class Class 4 (33 dBm) for 850/900 band Class 1 (30 dBm) for 1800/1900 ba nd EDGE (8-PSK) Power Class Class E2 (27 dBm) for 850/900 ban d Class E2 (26 dBm) for 1800/1900 b and
Data rate LTE category 1: up to 10.3 Mbit/s DL, up to 5.2 Mbit/s UL	Data rate HSDPA category 8: up to 7.2 Mbit/s DL HSUPA category 6: up to 5.76 Mbit/s UL	Data rate GPRS multi-slot class 33, CS1-CS4, up to 107 kbit/s DL, 85.6 kbit/s UL EDGE multi-slot class 33, MCS1-MCS9, up to 296 kbit/s DL, 236.8 kbit/s UL

Table 2: LARA-R2 and LARA-R6 modules LTE, 3G and 2G characteristics summary

- 1. 3G RAT is not supported by LARA-R203, LARA-R204, LARA-R211, LARA-R220, LARA-R6401 or LARA-R6401D modules.
- 2G RAT is not supported by LARA-R202, LARA-R203, LARA-R204, LARA-R220, LARA-R280, LARA-R281, LARA-R6401 or LARA-R6401D modules.
- LTE TDD radio access technology is not supported by LARA-R2 series, LARA-R6401, or LARA-R6801 modules.

Table 3 summarizes LARA-R2, and LARA-R6 series modules cellular RF bands.

Module	Region	LTE FDD band s	LTE TDD band s	3G bands	2G bands
LARA- R202	North America	12 (700 MHz) 5 (850 MHz) 4 (1700 MHz) 2 (1900 MHz)		5 (850 MHz) 2 (1900 MHz)	
LARA- R203	North America	12 (700 MHz) 4 (1700 MHz) 2 (1900 MHz)			

LARA- R204	North America	13 (700 MHz) 4 (1700 MHz)		
LARA- R211	Europe, Middle East, A frica	20 (800 MHz) 3 (1800 MHz) 7 (2600 MHz)		GSM 850 DCS 1800
LARA- R220	Japan	19 (800 MHz) 1 (2100 MHz)		

LARA- R280	Asia-Pacific	28 (700 MHz) 8 (900 MHz) 3 (1800 MHz)	1 (2100 MHz)	
LARA- R281	Europe, Middle East, A frica	28 (700 MHz) 20 (800 MHz) 8 (900 MHz) 3 (1800 MHz) 1 (2100 MHz)	1 (2100 MHz)	

LARA- R6001 LAR A-R6001D	Global	12 (700 MHz) 28 (700 MHz) 13 (700 MHz) 20 (800 MHz) 18 (800 MHz) 19 (800 MHz) 26 (850 MHz) 5 (850 MHz) 8 (900 MHz) 4 (1700 MHz) 3 (1800 MHz) 2 (1900 MHz) 1 (2100 MHz) 7 (2600 MHz)	39 (1900 MHz) 40 (2300 MHz) 41 (2600 MHz) 38 (2600 MHz)	5 (850 MHz) 8 (900 MHz) 2 (1900 MHz) 1 (2100 MHz)	GSM 850 E-GSM 900 DCS 1800 PCS 1900
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LARA- R6401 LAR A-R6401D	North America	71 (600 MHz) 12 (700 MHz) 13 (700 MHz) 14 (700 MHz) 5 (850 MHz) 4 (1700 MHz) 66 (1700 MHz) 2 (1900 MHz)				
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LARA- R6801	Europe, Middle East, A frica Asia-Pacific Japan Latin America	28 (750 MHz) 20 (800 MHz) 18 (800 MHz) 19 (800 MHz) 26 (850 MHz) 5 (850 MHz) 8 (900 MHz) 4 (1700 MHz) 3 (1800 MHz) 2 (1900 MHz) 1 (2100 MHz) 7 (2600 MHz)		5 (850 MHz) 8 (900 MHz) 2 (1900 MHz) 1 (2100 MHz)	GSM 850 E-GSM 900 DCS 1800 PCS 1900
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Table 3: LARA-R2 and LARA-R6 series modules cellular RF bands summary

Migration between LARA modules

Overview

The u-blox LARA form factor (26.0 x 24.0 mm, 100-pin LGA) includes the following series of modules, with compatible pin assignments as described in Figure 1, so that the modules can be alternatively mounted on a single application PCB using exactly the same copper, solder resist and paste mask.

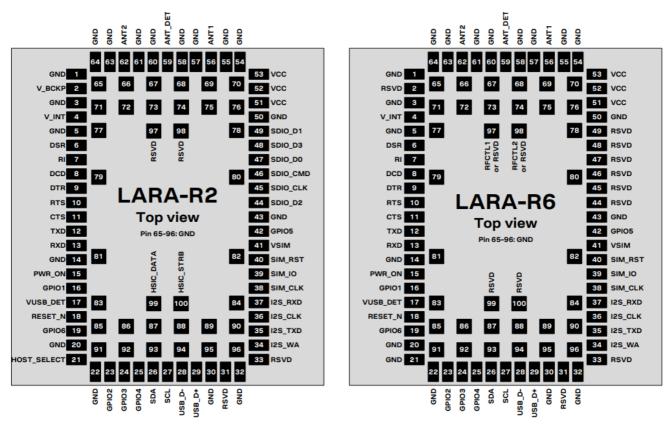


Figure 1: LARA-R2 and LARA-R6 series modules' layout and pinout

Table 4 summarizes the interfaces supported by LARA series modules:

	LARA-R2 series	LARA-R6 series
VCC module supply input	•	•
V_INT 1.8V supply output	•	•
V_BCKP RTC supply input/output	•	
ANT1 main RF input/output	•	•
ANT2 RF Rx diversity input	•	•
ANT_DET antenna detection input	•	•

Antenna dynamic tuning (RFCTL1 / RFCTL2)		•	4
PWR_ON input	•	•	
RESET_N input	•	•	
SIM interface	•	•	
SIM detection	•	•	
Main primary 8-wire UART	•	•	
Auxiliary secondary 4-wire UART		•	
Auxiliary secondary 2-wire UART	•		

1. LARA-R6401 and LARA-R6401D only

	LARA-R2 series	LARA-R6 series
USB High-Speed Interface	•	•
I2C interface	•	•
Digital Audio Interface	•	• 5
Clock output	•	• <u>5</u>
GPIOs	•	•

Table 4: Summary of interfaces supported by LARA-R2/R6 migration guide modules

The LARA modules are also form-factor compatible with the u-blox SARA, LISA, and TOBY cellular module families: although each has a different form factor, the footprints for the TOBY, LISA, LARA, and SARA modules have been developed to ensure layout compatibility.

With the u-blox "nested design" solution, any TOBY, LISA, SARA, or LARA module can be alternatively mounted on the same space of a single "nested" application board as described in Figure 2, enabling straightforward development of products supporting different cellular radio access technologies.

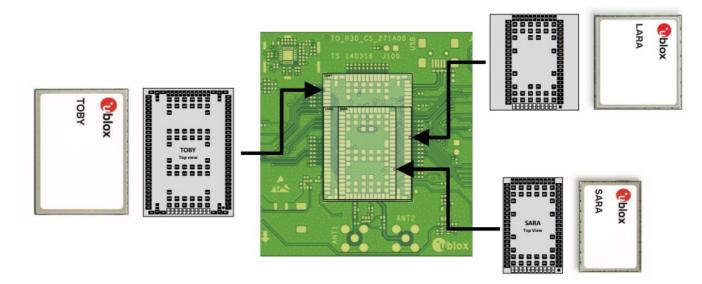


Figure 2: Cellular modules layout compatibility: all modules can be mounted on the same nested footprint

In detail, as described in Figure 3, a different top-side stencil (paste mask) is needed for each u-blox module form factor (TOBY, LISA, SARA, and LARA) to be alternatively mounted on the same space of a single "nested" application board.

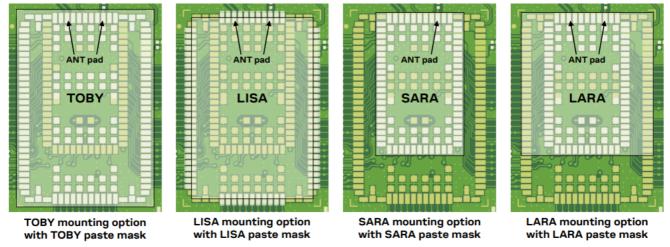


Figure 3: Top-side stencil (paste mask) designs to alternatively mount SARA, LARA, LISA, TOBY modules on the same PCB

Detailed guidelines to implement a nested application board, a comprehensive description of the u-blox reference nested design and detailed comparisons between the u-blox SARA, LARA, LISA, and TOBY modules are provided in the Nested design application note [3].

Pin-out comparison between LARA modules

Table 5 shows a pin-out comparison between LARA-R2 and LARA-R6 series modules.

No	LARA-R2 series	LARA-R6 series
1	GND	GND
	Ground	Ground
2	V_BCKP	RSVD
	RTC supply I/O	Reserved for future use. Internally not connected.
3	GND	GND
	Ground	Ground
4	V_INT	V_INT

	1.8 V (typical) supply output	1.0 M (tripical) crimply crimply
	Generated by internal DC/DC step-down regulator, when the module is turned on.	1.8 V (typical) supply output Generated by internal LDO linear regulator, when the module is turned on.
	Test point recommended	Test point recommended
5	GND	GND
	Ground	Ground
6	DSR	DSR
	Main primary UART Data Set Ready output (push-pull, idle high, active low)	Main primary UART Data Set Ready output (push-pull, idle high, active low)
		Alternative function:
		Second auxiliary UART HW flow control input
	V_INT voltage supply domain (1.8 V) Output driver	(idle high, active low, with internal active pull-up ena bled). V_INT voltage supply domain (1.8 V)
	strength: 6 mA	Output driver strength: 2 mA
	Internal active pull-up strength: ~7.5 k Ω	Internal active pull-up strength: ~100 kΩ
7	RI	RI
1		
	Main primary UART Ring Indicator output (push-pul I, idle high, active low)	Main primary UART Ring Indicator output (push-pull , idle high, active low) Alternative function:
		' ' '
		, idle high, active low) Alternative function:
		, idle high, active low) Alternative function: Second auxiliary UART HW flow control output
8	I, idle high, active low) V_INT voltage supply domain (1.8 V) Output driver	, idle high, active low) Alternative function: Second auxiliary UART HW flow control output (push-pull, idle high, active low). V_INT level (1.8 V)
8	I, idle high, active low) V_INT voltage supply domain (1.8 V) Output driver strength: 6 mA	, idle high, active low) Alternative function: Second auxiliary UART HW flow control output (push-pull, idle high, active low). V_INT level (1.8 V) Output driver strength: 2 mA DCD Main primary UART Data Carrier Detect output (push-pull, idle high, active low)
8	I, idle high, active low) V_INT voltage supply domain (1.8 V) Output driver strength: 6 mA DCD Main primary UART Data Carrier Detect output (pu	, idle high, active low) Alternative function: Second auxiliary UART HW flow control output (push-pull, idle high, active low). V_INT level (1.8 V) Output driver strength: 2 mA DCD Main primary UART Data Carrier Detect output (pus
8	I, idle high, active low) V_INT voltage supply domain (1.8 V) Output driver strength: 6 mA DCD Main primary UART Data Carrier Detect output (pu	, idle high, active low) Alternative function: Second auxiliary UART HW flow control output (push-pull, idle high, active low). V_INT level (1.8 V) Output driver strength: 2 mA DCD Main primary UART Data Carrier Detect output (push-pull, idle high, active low) Alternative function: Second auxiliary UART data output (push-pull, idle
8	I, idle high, active low) V_INT voltage supply domain (1.8 V) Output driver strength: 6 mA DCD Main primary UART Data Carrier Detect output (pu sh-pull, idle high, active low) V_INT voltage supply domain (1.8 V) Output driver	, idle high, active low) Alternative function: Second auxiliary UART HW flow control output (push-pull, idle high, active low). V_INT level (1.8 V) Output driver strength: 2 mA DCD Main primary UART Data Carrier Detect output (push-pull, idle high, active low) Alternative function: Second auxiliary UART data output (push-pull, idle high, active low). V_INT voltage supply domain (1.8 V)

Second auxiliary UART data input (idle high, active low, with internal active pull-up ena bled). V_INT voltage supply domain (1.8 V) Internal active pull-up strength: \sim 7.5 k Ω	Main primary UART Data Terminal Ready input (idle high, active low, with internal active pull-up en abled) to be set low to activate the greeting text.	Main primary UART Data Terminal Ready input (idle high, active low, with internal active pull-up ena bled) to be set low to activate the greeting text. Alternative function:
		(idle high, active low, with internal active pull-up ena

No	LARA-R2 series	LARA-R6 series
10	RTS	RTS
	Main primary UART HW flow control input	Main primary UART HW flow control input
	(idle high, active low, with internal active pull-up enabled) V_INT voltage supply domain (1.8 V)	(idle high, active low, with internal active pull-up enabled) V_INT voltage supply domain (1.8 V)
	Internal active pull-up strength: ~7.5 kΩ	Internal active pull-up strength: ~100 kΩ
11	стѕ	стѕ
	Main primary UART HW flow control output (push-pull, idle high, active low).	Main primary UART HW flow control output (push-pull, idle high, active low).
	V_INT voltage supply domain (1.8 V)	V_INT voltage supply domain (1.8 V)
	Output driver strength: 6 mA	Output driver strength: 2 mA
12	TXD	TXD
	Main primary UART data input	Main primary UART data input
	(idle high, active low, with internal active pull-up enabled). V_INT voltage supply domain (1.8 V)	(idle high, active low, with internal active pull-up enabled). V_INT voltage supply domain (1.8 V)
	Internal active pull-up strength: ~7.5 kΩ	Internal active pull-up strength: ~100 kΩ
13	RXD	RXD
	Main primary UART data output (push-pull, idle high, active low). V_INT voltage supply domain (1.8 V)	Main primary UART data output (push-pull, idle high, active low). V_INT voltage supply domain (1.8 V)
	Output driver strength: 6 mA	Output driver strength: 2 mA
14	GND	GND
	Ground	Ground
15	PWR_ON	PWR_ON

		Power-on/off input
	Power-on/off input (idle high, active low, with 10 kΩ internal pull-up). V _BCKP voltage supply domain (1.8 V) L-level: -0.30 ÷ 0.54 V L-level pulse time to trigger switch on: 50 μs min L-level pulse time to trigger graceful switch off: 1.0 s min No external pull-up to be connected Test point recommended	 (idle high, active low, with ~200 kΩ internal pull-up). Internal voltage supply domain (~0.8 V at the pin in i dle) L-level: -0.30 ÷ 0.35 V L-level pulse time to trigger switch on: 0.15 s min ÷ 3.2 s max L-level pulse time to trigger graceful switch off: 1.5 s min No external pull-up to be connected Test point recommended
16	GPIO1	GPIO1
	GPIO configurable as Input, Output, Network status indication, external GNSS supply enable. Default: tri-stated with internal pull-down enabled. V _INT voltage supply domain (1.8 V) Push-pull output type. Output driver strength: 6 mAInternal active pull-up strength: ~17 kΩ	GPIO configurable as Input, Output, Network status indication, external GNSS supply enable. Default: tri-stated with internal pull-down enabled. V _INT voltage supply domain (1.8 V) Push-pull output type. Output driver strength: 2 mA Internal active pull-up/down strength: ~100 kΩ
17	VUSB_DET	VUSB_DET
	5 V sense input to detect USB host and enable the USB. H-level: 1.5 ÷ 5.25 V Test point highly recommended	5 V sense input to detect USB host and enable the USB H-level: 1.5 ÷ 5.25 V Test point highly recommended
18	RESET_N	RESET_N
	Abrupt emergency reset shutdown input (idle high, active low, with 10 kΩ internal pull-up). V _BCKP voltage supply domain (1.8 V) L-level: -0.30 ÷ 0.54 V L-level time to trigger abrupt PMU and module rebo ot: 50 ms min Test point recommended	Abrupt emergency reset shutdown input (idle high, active low, with ~37 k Ω internal active pul l-up). Internal voltage supply domain (~1.8 V at the pin in idle) L-level: -0.30 \div 0.63 V L-level time to trigger graceful module reboot: 50 m s min \div 6 s max L-level time to trigger abrupt module switch off: 10 s min Test point recommended

No	LARA-R2 series	LARA-R6 series
19	GPIO6	GPIO6

25	GPIO4	GPIO4
	Internal active pull-up/down strength: ~7.5 kΩ	Internal active pull-up/down strength: ~100 kΩ
	Push-pull output type. Output driver strength: 6 mA	Push-pull output type. Output driver strength: 2 mA
	Default: input for external GNSS Tx data ready V_I NT voltage supply domain (1.8 V)	Default: input for external GNSS Tx data ready V_I NT voltage supply domain (1.8 V)
	GPIO configurable as Input, Output, Network status indication output, external GNSS supply enable out put, external GNSS data ready input.	GPIO configurable as Input, Output, Network status indication output, external GNSS supply enable out put, external GNSS data ready input, Last gasp trig ger input, Faster and safe power-off trigger input.
24	GPIO3	GPIO3
	Internal active pull-up/down strength: ~7.5 kΩ	Internal active pull-up/down strength: ~100 kΩ
	Push-pull output type. Output driver strength: 6 mA	Push-pull output type. Output driver strength: 2 mA
	GPIO configurable as Input, Output, Network status indication output, external GNSS supply enable out put. Default: output for external GNSS supply enable control V_INT voltage supply domain (1.8 V)	GPIO configurable as Input, Output, Network status indication output, external GNSS supply enable out put. Default: output for external GNSS supply enabl e control V_INT voltage supply domain (1.8 V)
23	GPIO2	GPIO2
	Ground	Ground
22	GND	GND
	Internal active pull-up/down strength: ~7.5 kΩ	
	Default: tri-stated with internal pull-down enabled. V _INT voltage supply domain (1.8 V)	Ground
	Selection of module / host processor configuration f unction not supported by current FW version.	
21	HOST_SELECT	GND
	Ground	Ground
20	GND	GND
	Internal active pull-up/down strength: ~7.5 kΩ	Internal active pull-up/down strength: ~100 kΩ
	Push-pull output type. Driver strength: 4 mA	Push-pull output type. Output driver strength: 2 mA
	. Default: tri-stated with internal pull-down enabled. V_INT voltage supply domain (1.8 V)	6. Default: tri-stated with internal pull-down enabled. V_INT voltage supply domain (1.8 V)
	13 or 26 MHz clock output enabled by AT command	12.288 MHz clock output enabled by AT command

	GPIO configurable as Input, Output, Network status indication output, external GNSS supply enable out put. Default: output / low	GPIO configurable as Input, Output, Network status indication output, external GNSS supply enable out put. Default: output / low
	V_INT voltage supply domain (1.8 V) Push-pull outp ut type.	V_INT voltage supply domain (1.8 V) Push-pull output type.
	Output driver strength: 6 mA	Output driver strength: 2 mA
	Internal active pull-up/down strength: ~7.5 kΩ	Internal active pull-up/down strength: ~100 kΩ
26	SDA	SDA
	I2C data	I2C data
	(open drain, idle high, active low, no internal pull-up). Alternative function:	(open drain, idle high, active low, 2.2 k Ω internal pul l-up).
	Second auxiliary UART data input	
	(idle high, active low, with internal active pull-up enabled).	
	V_INT voltage supply domain (1.8 V)	V_INT voltage supply domain (1.8 V)

No	LARA-R2 series	LARA-R6 series
27	SCL	SCL
	I2C clock (open drain, idle high, active low, no internal pullup). Alternative function: Second auxiliary UART data output (push-pull, idle high, active low). V_INT voltage supply domain (1.8 V)	I2C clock (open drain, idle high, active low, 2.2 k Ω internal pullup). V_INT voltage supply domain (1.8 V)
28	USB_D-	USB_D-
	USB data I/O (D-) High-speed USB 2.0	USB data I/O (D-) High-speed USB 2.0
	Test point highly recommended	Test point highly recommended
29	USB_D+	USB_D+
	USB data I/O (D+) High-speed USB 2.0	USB data I/O (D+) High-speed USB 2.0
	Test point highly recommended	Test point highly recommended
30	GND	GND
	Ground	Ground

31	RSVD	RSVD
	Reserved for future use	Reserved for future use
	Internally not connected	Internally not connected
32	GND	GND
	Ground	Ground
33	RSVD	RSVD
	Reserved use	Reserved use
	It must be connected to ground	Test point highly recommended
34	I2S_WA	I2S_WA 7
	I2S Word Alignment, alternatively configurable G PIO. Default: I2S Word Alignment	I2S Word Alignment, alternatively configurable GPIO. Default: I2S Word Alignment
	V_INT voltage supply domain (1.8 V) Push-pull output type.	V_INT voltage supply domain (1.8 V) Push-pull output type.
	Output driver strength: 6 mA	Output driver strength: 2 mA
	Internal active pull-up/down strength: ~7.5 kΩ	Internal active pull-up/down strength: ~7.5 kΩ
35	I2S_TXD	I2S_TXD <u>7</u>
	I2S data output, alternatively configurable GPIO. Default: I2S data output	I2S data output, alternatively configurable GPIO. Defa ult: I2S data output
	V_INT voltage supply domain (1.8 V) Push-pull output type.	V_INT voltage supply domain (1.8 V) Push-pull output type.
	Output driver strength: 6 mA	Output driver strength: 2 mA
	Internal active pull-up/down strength: ~7.5 kΩ	Internal active pull-up/down strength: ~100 kΩ
36	I2S_CLK	12S_CLK <u>7</u>
	I2S clock, alternatively configurable GPIO. Defaul t: I2S clock	I2S clock, alternatively configurable GPIO. Default: I2 S clock
	V_INT voltage supply domain (1.8 V) Push-pull output type.	V_INT voltage supply domain (1.8 V) Push-pull output type.
	Output driver strength: 6 mA	Output driver strength: 2 mA
	Internal active pull-up/down strength: ~7.5 kΩ	Internal active pull-up/down strength: ~100 kΩ
37	I2S_RXD	I2S_RXD <u>7</u>

I2S data input, alternatively configurable GPIO. D efault: I2S data input	I2S input, alternatively configurable GPIO. Default: I2 S data input
V_INT voltage supply domain (1.8 V) Push-pull output type.	V_INT voltage supply domain (1.8 V) Push-pull output type.
Output driver strength: 6 mA	Output driver strength: 2 mA
Internal active pull-up/down strength: ~7.5 k Ω	Internal active pull-up/down strength: ~100 k Ω

No	LARA-R2 series	LARA-R6 series
38	SIM_CLK	SIM_CLK
	Clock output for external 1.8 V / 3 V SIM card/chip	Clock output for external 1.8 V / 3 V SIM card/chip
39	SIM_IO	SIM_IO
	I/O data line for external 1.8 V / 3 V SIM card/chip	I/O data line for external 1.8 V / 3 V SIM card/chip
	Internal pull-up: 4.7 kΩ	Internal pull-up: 4.7 kΩ
40	SIM_RST	SIM_RST
	Reset output for external 1.8 V / 3 V SIM card/chip	Reset output for external 1.8 V / 3 V SIM card/chip
41	VSIM	VSIM
	Supply output for external 1.8 V / 3 V SIM card/chip	Supply output for external 1.8 V / 3 V SIM card/chip
42	GPIO5	GPIO5
	GPIO configurable as Input, Output, SIM detection i nput. Default: SIM detection input	GPIO configurable as Input, Output, SIM detection i nput. Default: SIM detection input
	V_INT voltage supply domain (1.8 V) Push-pull out put type.	V_INT voltage supply domain (1.8 V) Push-pull output type.
	Output driver strength: 6 mA	Output driver strength: 2 mA
	Internal active pull-up/down strength: ~7.5 kΩ	Internal active pull-up/down strength: ~100 kΩ
43	GND	GND
	Ground	Ground
44	SDIO_D2	RSVD
	SDIO serial data [2], not supported by current FW	
	Default: tri-stated with internal pull-down enabled.	Reserved for future use
45	SDIO_CLK	RSVD
	SDIO serial clock, not supported by current FW	
	Default: tri-stated with internal pull-down enabled.	Reserved for future use

46	SDIO_CMD	RSVD
	SDIO command, not supported by current FW Default: tri-stated with internal pull-down enabled.	Reserved for future use
47	SDIO_D0	RSVD
	SDIO serial data [0], not supported by current FW Default: tri-stated with internal pull-down enabled.	Reserved for future use
48	SDIO_D3	RSVD
	SDIO serial data [3], not supported by current FW Default: tri-stated with internal pull-down enabled.	Reserved for future use
49	SDIO_D1	RSVD
	SDIO serial data [1], not supported by current FW Default: tri-stated with internal pull-down enabled.	Reserved for future use
50	GND	GND
	Ground	Ground
51	vcc	vcc
	Supply input for the whole module Normal operatin g range: 3.3 ÷ 4.4 V Extended operating range: 3.0 ÷ 4.5 V LARA-R211: Supply input for baseband PMU part	Supply input for baseband PMU part Normal operating range: 3.3 ÷ 4.5 V Extended operating range: 3.1 ÷ 4.5 V
52	vcc	vcc
	Supply input for the whole module Normal operating range: 3.3 ÷ 4.4 V Extended operating range: 3.0 ÷ 4.5 V LARA-R211: Supply for RF Power Amplifiers part	Supply for RF Power Amplifiers part. Normal operating range: 3.3 ÷ 4.5 V Extended operating range: 2.8 ÷ 4.5 V

No	LARA-R2 series	LARA-R6 series
53	vcc	vcc
	Supply input for the whole module Normal operating range: 3.3 ÷ 4.4 V Extended operating range: 3.0 ÷ 4.5 V LARA-R211: Supply for RF Power Amplifiers part	Supply for RF Power Amplifiers part Normal operating range: 3.3 ÷ 4.5 V Extended operating range: 2.8 ÷ 4.5 V
54	GND	GND
	Ground	Ground

55	GND	GND
	Ground	Ground
56	ANT1	ANT1
	RF pin for main Tx / Rx cellular antenna	RF pin for main Tx / Rx cellular antenna
	50 Ω nominal characteristic impedance.	50 Ω nominal characteristic impedance.
57	GND	GND
	Ground	Ground
58	GND	GND
	Ground	Ground
59	ANT_DET	ANT_DET
	Input pin for antenna detection (optional function)	Input pin for antenna detection (optional function)
60	GND	GND
	Ground	Ground
61	GND	GND
	Ground	Ground
62	ANT2	ANT2
	RF pin for secondary Rx diversity cellular anten na	RF pin for secondary Rx diversity cellular antenna
	$50~\Omega$ nominal characteristic impedance.	50 Ω nominal characteristic impedance.
63	GND	GND
	Ground	Ground
	All pins from 63 to 96 are Ground pins	All pins from 63 to 96 are Ground pins
96	GND	GND
	Ground	Ground
97	RSVD	RSVD 8
		Reserved for future use
	Reserved for future use. Internally not connecte	RFCTL1 9
	d.	1.8 V push-pull output to control an antenna tuning IC.
98	RSVD	RSVD 8

		Reserved for future use
	Reserved for future use. Internally not connecte	RFCTL2 9
	d.	1.8 V push-pull output to control antenna tuning IC.
99	HSIC_DATA	RSVD
	HSIC USB not supported by current FW.	Reserved for future use
100	HSIC_STRB	RSVD
	HSIC USB not supported by current FW.	Reserved for future use

- Table 5: LARA-R2 and LARA-R6 series modules pin assignment and description, with remarks for migrationu
- For further details regarding characteristics, capabilities, usage or settings applicable for each interface of the LARA-R2 and LARA-R6 series cellular modules, see the related data sheet [1] [4], the related integration manual [2] [5], the related AT commands manual [6] [7], and the nested design application note [3].

Interfaces comparison between LARA modules

VCC module supply input

- As the LARA-R2 and LARA-R6 series modules have compatible power requirements, there are only minor differences in their VCC input voltage ranges and current consumption figures. The same compatible external VCC supply circuit can be implemented for all the LARA modules, as for example the one described in Figure 4.
- The nominal voltage provided at the VCC input pins must be within the related normal operating range limits, and the actual voltage during module operations has to be held above the minimum limit of the extended operating range to avoid the undervoltage switch-off of the module. For the detailed values of VCC input voltage ranges, see

Table 5, or the related module's data sheet [1] and [4].

- The time-division RF transmission of 2G radio access technology can be up to ~2 W, whereas in 3G or LTE radio access technology it is only up to ~0.25 W. Therefore, the pulse current profile in radio connected mode when a data/voice call is enabled may be significantly higher for cellular modules supporting the 2G radio access technology than for modules that do not have 2G fallback.
- While selecting and designing the supply source for LARA cellular modules, consider with adequate safe
 margin the maximum current consumption of the LARA cellular module specifically selected, considering the
 radio access technologies supported by the module.
- For the detailed module's current consumption figures, see the related module's data sheet [1] [4]. For additional specific design guidelines, see the related system integration manual [2] [5].

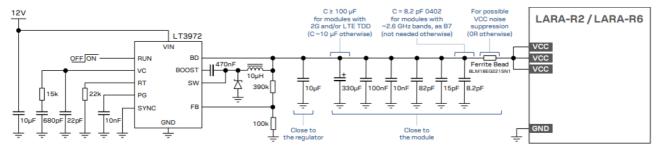


Figure 4: Example of compatible VCC supply application circuit using a high reliability step-down regulator

- The VCC supply circuit illustrated in Figure 4 includes capacitors with Self-Resonant Frequency in the supported RF cellular bands, intended to be placed close to the VCC pins of the module, narrowing the VCC line down to the pad of the capacitors, to adequately filter EMI in the supported RF cellular bands. Additionally, a ferrite bead specifically designed to suppress EMI in the GHz band is placed very close to the VCC pins of the module to suppress possible noise from the VCC line.
- Note that the switch-on sequence of LARA-R2 series can be triggered by applying a valid VCC supply, starting
 a voltage value of less than 2.1 V, and with a fast-rising slope (from 2.3 V to 2.8 V in less than 4 ms) up to the
 nominal VCC voltage within the normal operating range.
- Instead, LARA-R6 series modules continue to be switched off even after a valid VCC supply has been applied:
 the PWR_ON input line must be properly toggled low, with valid VCC supply present, to trigger the switch-on sequence of these modules.

V INT 1.8 V supply output

- LARA-R2 and LARA-R6 series modules provide a 1.8 V supply output at the V_INT pin, which is internally
 generated when the module is switched on.
- The same voltage domain is used internally to supply the generic digital interfaces of the modules (as the UARTs, I2C, I2S, GPIOs), and therefore it is recommended to use the V_INT supply output to supply the module side of external voltage translators connected to these interfaces of the modules.
- It is recommended to sense the status of the V_INT output to define when the module is switched on, and it is recommended to provide a test point for diagnostic.

V_BCKP RTC supply input/output

• LARA-R2 series modules provide the RTC supply input/output at the V_BCKP pin, which is not available on LARA-R6 series modules, having the same pin internally not connected.

Cellular RF interfaces

- LARA-R2 and LARA-R6 series modules provide the primary RF input/output line at the ANT1 pin, which must be connected to a suitable antenna to transmit and receive cellular RF signals, and they provide the secondary RF input line at the ANT2 pin, which is intended to be connected to an antenna to receive cellular RF signals in LTE and 3G radio access technologies implementing the Rx diversity function.
- The same optional antenna detection circuit can be implemented for LARA-R2 and LARA-R6 series modules using the available optional ANT_DET input pin.
- While selecting the antenna for LARA cellular modules, consider the frequency range supported by each LARA module, as illustrated in Figure 5.

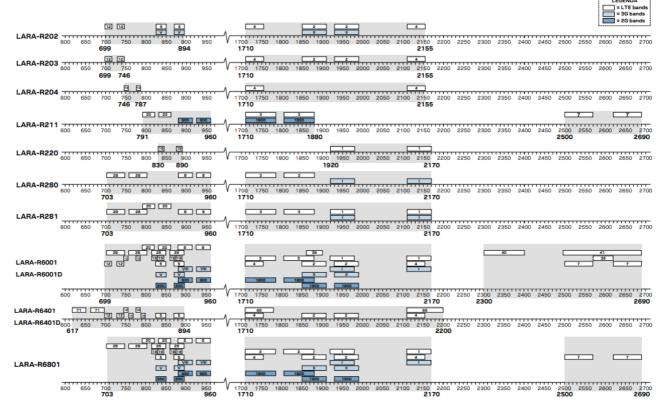


Figure 5: Summary of operating frequency bands supported by LARA modules

System control interfaces

- The PWR_ON and the RESET_N input lines have internal pull-up resistors on LARA-R2 and LARA-R6 series modules, and both lines are intended to be driven by external open drain drivers: same compatible external circuits can be implemented for all the LARA modules.
- The switch-on sequence of LARA-R2 series modules can be triggered by applying a valid VCC power supply
 (see section 2.3.1), while LARA-R6 series modules remain switched off after a valid VCC power supply is
 applied to the modules: the PWR_ON input line must be properly toggled low, with valid VCC supply present, to
 trigger the switch-on sequence of the modules.
- The PWR_ON input line can be used to trigger the graceful switch-off procedure of the LARA-R2 and LARA-R6 series modules, as an alternative to using the +CPWROFF AT command. Afterwards, the switch-on sequence of modules can be triggered again by properly toggling low PWR_ON input line.
- The assertion or toggling of the RESET N input line causes different actions:
- the RESET_N line of LARA-R2 series modules triggers an unconditional reboot of the module when toggled, with internal PMU shutdown when set low.
- the RESET_N line of LARA-R6 series modules triggers an unconditional graceful reboot of the module when set low for a short time period.
- the RESET_N line of LARA-R6 series modules triggers an unconditional shutdown of the module when set low for a long time period.
- The timings for proper control of the PWR_ON and RESET_N input lines of LARA-R2 and LARA-R6 series modules are reported in the related data sheet [1] and [4].
- It is recommended to provide test points on the PWR_ON and RESET_N input lines of LARA-R2 and LARA-R6 series modules, to trigger the FW update procedure, and for diagnostic purpose.

SIM interface

- The same compatible external SIM circuit can be implemented for all LARA modules: external 1.8 V and 3.0 V
 SIM card / IC are supported over the available standardized
- SIM interface (VSIM, SIM IO, SIM CLK, SIM RST pins).
- The same optional SIM detection circuit can be implemented for LARA series modules using the available GPIO5 pin.

UART interfaces

- · Main primary UART interface
- LARA-R2 and LARA-R6 modules provide a compatible main 8-wire 1.8 V UART interface including:
- data lines (RXD output, TXD input),
- hardware flow control lines (CTS output, RTS input),
- modem status and control lines (DTR input, DSR output, DCD output, RI output)
- The main primary UART interface supports AT commands and data communication, multiplexer functionality including virtual channel for GNSS tunneling, and FW update by means of FOAT on all the LARA modules.
- Additionally, LARA-R2 series modules support the FW update by means of the u-blox EasyFlash tool, and the diagnostic trace logging functions over the main primary UART interface.
- It is recommended to provide test points on RXD and TXD pins of LARA series modules, for FW update and diagnostic, in particular if the USB interface is connected to the external host processor.
- The primary UART interfaces of LARA series modules are electrically compatible, so that the same compatible
 external circuit can be used. It is recommended to use the V_INT output to supply the module side of external
 voltage translators connected to the UART interfaces.

The baud rates and configurations available and supported by LARA-R2 and LARA-R6 series modules for the main primary UART interface may slightly differ:

- LARA-R2 series modules have the automatic baud rate and frame format detection available by default, and they support high-speed UART data rates up to 6.5 Mbit/s.
- LARA-R6 series modules have the 115200 bit/s baud rate and the 8N1 frame format available by default, and they support high-speed UART data rates up to 3.0 Mbit/s.
- For more details about configurations of UART interfaces, see the u-blox AT commands manual [6], +IPR, +ICF, +IFC, &K, \Q, +UPSV, +CMUX, +USIO, +UUSBCONF AT commands, where supported).

Auxiliary UART interface

- LARA-R202, LARA-R203 and LARA-R211 modules provide an auxiliary secondary 2-wire 1.8 V UART serial interface, as alternative function of the I2C interface (SCL and SDA pins) including:
- data lines (SCL pin as AUX UART data output, SDA pin as AUX UART data input)
- LARA-R6 series modules provide an auxiliary secondary 4-wire 1.8 V UART serial interface, as alternative function of the main UART interface DTR, DSR, DCD and RI pins, including:
- data lines (DCD pin as AUX UART data output, DTR pin as AUX UART data input)
- HW flow control lines (RI as AUX UART flow control output, DSR as AUX UART flow control input)

- The data lines of the auxiliary UART interfaces of LARA series modules are electrically compatible, so that the same compatible external circuit can be used. However, the
- AUX UART data input and output functions are available on different pins comparing LARA-R2 and LARA-R6
 series modules. It is recommended to use the V_INT output to supply the module side of external voltage
 translators connected to the AUX UART.
- The baud rates and configurations available and supported by LARA-R2 and LARA-R6 series modules for the auxiliary UART interface may slightly differ: see the u-blox
- AT commands manual [6] (+IPR, +ICF, +IFC, &K, \Q, +USIO, +UUSBCONF AT commands, where supported).

USB interface

- LARA-R2 and LARA-R6 series modules provide a compatible USB 2.0 High-Speed interface including:
- VUSB_DET input pin to detect the presence of an external USB host, and enable the USB interface of the module by applying an external valid USB VBUS voltage (1.5 V minimum, 5.0 V typical),
- **USB_D+** and USB_D- data and signaling lines according to the USB 2.0 standard.
- The USB interface supports AT commands and data communication, GNSS tunneling, the FW update by means of FOAT, the FW update by means of the u-blox
- EasyFlash tool, and the diagnostic trace logging functions on all the LARA-R2 and LARA-R6 series modules.
- It is highly recommended to provide accessible test points on VUSB_DET, USB_D+ and USB_D- pins of LARA-R2 and LARA-R6 series modules, for FW update and diagnostic.
- The configurations available and supported by LARA-R2 and LARA-R6 series modules for the USB interface may slightly differ: see the related data sheet of the modules [1] [4], and the u-blox AT commands manual [6] (+USIO, +UUSBCONF AT commands, where supported).
- The USB interface of the LARA-R6 series modules is enabled only if an external voltage detectable as High logic level is applied at the VUSB_DET input during the switch-on boot sequence of the module.

I2C interface

- LARA-R2 and LARA-R6 series modules provide a compatible 1.8 V I2C interface (SDA, SCL pins) available to communicate with external u-blox GNSS chips / modules, and with external compatible
- I2C devices as for example an audio codec: the module acts as an I2C host which can communicate with I2C devices in accordance with the I2C bus specifications.
- LARA-R2 modules do not integrate pull-up resistors on SDA and SCL lines: external pull-up resistors have to
 be provided accordingly if the I2C interface is used in applications with LARA-R2 modules. Instead, LARA-R6
 series modules have internal pull-up resistors on SDA and SCL lines, so there is no necessity of external pullup resistors.
- It is recommended to use the V_INT output to supply the module side of external voltage translators connected to the I2C interface.

Digital audio interface

• LARA-R2 and LARA-R6 series modules provide a compatible 1.8 V digital audio interface over the I2S_TXD, I2S_RXD, I2S_CLK, I2S_WA pins, that can be configured by AT command to transfer digital audio data to/from an external device as an audio codec.

- The configurations available and supported by LARA-R2 and LARA-R6 series modules for the digital audio interface may slightly differ: see the Audio sections in the u-blox AT commands manual [6].
- LARA-R6001D / LARA-R6401D data-only product versions do not support voice / audio feature.

Clock output

- LARA-R2 and LARA-R6 series modules provide a compatible 1.8 V digital clock output on the GPIO6 pin. This is mainly designed to feed the clock input of an external audio codec, as it can be configured in "Audio dependent" mode (generated only when the audio is active), or in "Continuous" mode.
- LARA-R6001D / LARA-R6401D data-only product versions do not support GPIO6 clock output.

GPIOs

- LARA series modules provide nine compatible 1.8 V GPIO pins (GPIO1-GPIO5, I2S_TXD, I2S_RXD, I2S_CLK, I2S_WA) that can be configured as General Purpose
- Input/Output or to provide custom functions (for further details, see the related data sheet of the modules [1] [4], and the GPIO chapter in the u-blox AT commands manual [6]).

Antenna dynamic tuning

- LARA-R6401 and LARA-R6401D series modules support a wide range of frequencies, from 600 MHz to 2200 MHz. For such modules, to provide more efficient antenna designs over a wide bandwidth, RFCTL1 and RFCTL2 pins can be configured to change their output value in real time according to the operating LTE band in use by the module.
- These pins, paired with an external antenna tuner IC or RF switch, can be used to:
- tune antenna impedance to reduce power losses due to mismatch
- tune antenna aperture to improve total antenna radiation efficiency
- · select the optimal antenna for each operating band

Reserved pins

- LARA series modules include pins reserved for future use, marked as RSVD, which can all be left unconnected on the application board, except the RSVD #33 pin:
- It is recommended to connect to ground the RSVD #33 pin of LARA-R2 modules
- It is suggested to connect an accessible test point to the RSVD #33 pin of LARA-R6 modules

Other considerations and test points

• Table 6 lists the interfaces dedicated for special purposes, as the firmware update by means of u-blox EasyFlash tool and/or for diagnostic by means of u-blox m-center tool, on LARA modules.

Module	FW update by means of u-blox EasyFlash t ool	Diagnostic by means of u-blox m-center tool
LARA-R2	USB UART (2-wire data input/output)	USB UART (2-wire data input/output) AUX UART (2-w ire data input/output) HSIC
LARA-R6	USB	USB

- Table 6: Interfaces for FW update and/or diagnostic purposes on LARA modules
- It is highly recommended to provide test points directly connected to the pins with FW update and/or diagnostic functions available (as in particular the VUSB_DET, USB_D+ and USB_D- pins), depending also on which interface of the module is connected to external host application processor (as the RXD and TXD lines of the UART interface also have to be considered).
- Additionally, it is recommended to provide test points directly connected to the following pins of the modules for diagnostic purposes:
- V INT
- PWR ON
- RESET N
- RSVD #33 of LARA-R6 series modules
- All LARA-R2 and LARA-R6 series GND pins are intended to be externally connected to ground.
- For additional specific design-in guidelines, see the modules' system integration manual [2] [5].

Schematic for LARA modules integration

Figure 6 shows an example of a schematic diagram where a LARA-R2 or a LARA-R6 series module can be integrated into the same application board, using all the available interfaces and functions of the modules. The different mounting options for the external parts are noted herein according to the functions supported by each module.

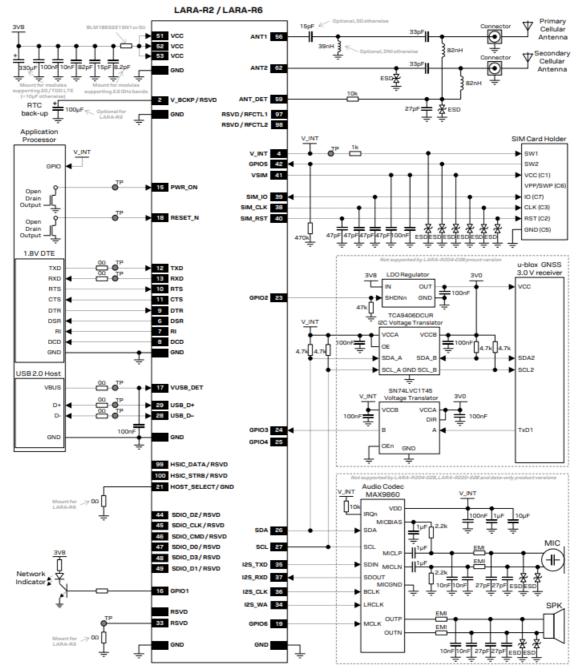


Figure 6: Example schematic diagram to integrate LARA-R2/LARA-R6 series modules on the same application board

Appendix A Glossary

Abbreviatio n	Definition	
2G	2G 2nd Generation Cellular Technology (GSM, GPRS, EGPRS)	
3G 3rd Generation Cellular Technology (UMTS, HSDPA, HSUPA)		
3GPP	3rd Generation Partnership Project	
8-PSK	8 Phase-Shift Keying modulation	
APAC	Asia-Pacific	
AT	AT Command Interpreter Software Subsystem, or attention	
AUX	Auxiliary	

Cat	Category			
CDMA	Code Division Multiple Access			
CS	Coding Scheme			
CSFB	Circuit-Switched-Fall-Back			
CTS	Clear To Send			
DCD	Data Carrier Detect			
DCS	Digital Cellular System			
DL	Down-Link (Reception)			
DSR	Data Set Ready			
DTLS	Datagram Transport Layer Security			
DTR	Data Terminal Ready			
EDGE	Enhanced Data rates for GSM Evolution (EGPRS)			
eDRX	Extended Discontinuous Reception			
EGPRS	Enhanced General Packet Radio Service (EDGE)			
E-GSM	Extended GSM			
EMEA	Europe, the Middle East and Africa			
EMI	Electro-Magnetic Interference			
ESD	Electro-Static Discharge			
E-UTRA	Evolved Universal Terrestrial Radio Access			
FDD	Frequency Division Duplex			
FOAT	Firmware update Over AT commands			
FOTA	Firmware update Over The Air			
FTPS	File Transfer Protocol Secure			
FW	Firmware			
GMSK	Gaussian Minimum-Shift Keying modulation			
GND	Ground			
GNSS	Global Navigation Satellite System			
GPIO	General Purpose Input Output			
GPRS	General Packet Radio Service			
GPS	Global Positioning System			
GSM	Global System for Mobile communication			
HSDPA	High Speed Downlink Packet Access			
HSIC	High-Speed Inter-Chip USB interface			

HSPA	High-Speed Packet Access
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Abbreviatio n	Definition			
HSUPA	High Speed Uplink Packet Access			
HTTPS	HyperText Transfer Protocol Secure			
I/O	Input/Output			
I2C	Inter-Integrated Circuit interface			
I2S	Inter IC Sound interface			
IP	Internet Protocol			
LED	Light Emitting Diode			
LGA	Land Grid Array			
LNA	Low Noise Amplifier			
LPWA	Low Power Wide Area			
LTE	Long Term Evolution			
LwM2M	Open Mobile Alliance Lightweight Machine-to-Machine protocol			
MCS	Modulation and Coding Scheme			
MQTT	Message Queuing Telemetry Transport			
PA	Power Amplifier			
PCS	Personal Communications Service			
PMU	Power Management Unit			
PSM	Power Saving Mode			
N.A.	Not Available / Not Applicable			
RAT	Radio Access Technology			
RF	Radio Frequency			
RI	Ring Indication			
Rx	Receiver			
RTC	Real Time Clock			
RTS	Request To Send			
SAW	Surface Acoustic Wave			
SDIO	Secure Digital Input Output			
SIM	Subscriber Identification Module			
SMS	Short Message Service			
SPI	Serial Peripheral Interface			

TCP	Transmission Control Protocol			
TDD	Time Division Duplex			
TLS	Transport Layer Security			
TP	Test Point			
Тх	Transmitter			
UART	Universal Asynchronous Receiver-Transmitter			
uCSP	u-blox Common Services Platform			
UDP	User Datagram Protocol			
uFOTA	u-blox Firmware update Over The Air			
UL	Up-Link (Transmission)			
UMTS	Universal Mobile Telecommunications System			
URC	Unsolicited Result Code			
USB	Universal Serial Bus			
VoLTE	Voice over LTE			

Related documents

- 1. u-blox LARA-R2 series data sheet, UBX-16005783
- 2. u-blox LARA-R2 series system integration manual, UBX-16010573
- 3. u-blox nested design application note, UBX-16007243
- 4. u-blox LARA-R6 series data sheet, UBX-21004391
- 5. u-blox LARA-R6 series system integration manual, UBX-21010011
- 6. u-blox AT commands manual, UBX-13002752
- 7. u-blox LARA-R6 series AT commands manual, UBX-21046719

For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (<u>www.u-blox.com</u>).

Revision history

Revisio n	Date	Name	Comments
R01	29-Apr-2021	sses	Initial release
R02	05-May-2022	psca / sses	Added LARA-R6001D and LARA-R6401D. Some corrections and clarifications.

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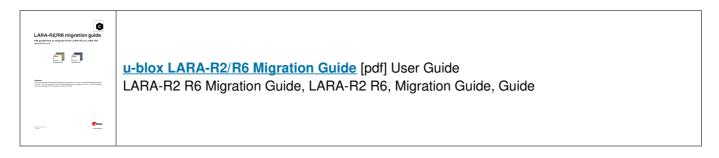
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Documents / Resources



References

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