U Blox JODY-W5 Series Host based Modules Instruction Manual

JODY-W5 series
Host-based modules with Wi-Fi 6 and Bluetooth 5.4
System integration manual

Contents

JODY-W5 Series Host based Modules

Abstract
Targeted towards hardware and software application engineers, this document describes how to integrate JODY-W5 modules in application products and explains the hardware design-in, software, component handling, regulatory compliance, and production testing. It also lists the external antennas approved for use with the module. JODY-W5 is designed for a wide range of industrial and automotive applications. Integrated with a MAC/Baseband processor and RF front end components, JODY-W5 modules connect to a host processor through SDIO for Wi-Fi, and High-Speed UART for Bluetooth.

Document information

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Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:
Product name

System description

1.1 Overview

The JODY-W5 series comprises ultra-compact multiradio modules that support 1×1 Wi-Fi 6 and Bluetooth 5.4 in product variants with single and dual antenna configuration. The modules are developed for reliable, highly demanding automotive and industrial applications.
JODY-W5 supports IEEE 802.11a/b/g/n/ac/ax Wi-Fi standards and delivers data throughput of up to 480 Mbps in dual band 2.4 / 5 GHz with a channel width of up to 80 MHz. Capable of working with different types of access point (AP) in both station and access point mode, the modules are used with an access-point or used in P2P communication, such as Wi-Fi direct.
JODY-W5 supports both Bluetooth BDR/EDR and Bluetooth Low Energy 5.4, including long-range PHY and isochronous channels for Bluetooth LE audio.
JODY-W5 series modules come with RF calibration data and MAC address available in OTP memory.
An optional LTE coexistence filter can also be ordered on request.
Radio type approvals for Europe (RED), the United States (FCC), and Canada (ISED).

1.2 Module architecture

JODY-W5 includes an NXP AW611 System-On-Chip (SoC) with fully integrated power management circuitry that provides power to the internal voltage domains of the SoC, a MAC address, transceivers for 2.4 GHz and 5 GHz Wi-Fi operation, and Bluetooth low energy 5.4.
JODY-W5 also includes discrete RF components for configuring the antenna interface enabling the antenna path connections as shown in [1].
For host CPU connectivity, the Secure Digital Input Output (SDIO) 3.0 interface is used for Wi-Fi communication and firmware downloads, and the Universal Asynchronous Receiver Transmitter (UART) interface for Bluetooth communication. The host interface configuration is selected by the configuration pins.
A PCM/I2S interface is available to connect an external audio codec and external audio system.
A 2-wire Wireless Coexistence Interface 2 (WCI-2) enables signaling between the modules, and an external co-located wireless device manages wireless medium sharing for optimal performance.
Several module variants, using one single RF architecture and antenna connection type are available.
The JODY-W562 architecture supports concurrent Wi-Fi SISO 2.4 and 5 GHz and simultaneous Bluetooth.
Table 1 defines the ordering codes and antenna configurations for module variant.

Ordering code	Antenna pin configuration	T emp.	LTE filter
JODY-W562-00A	RF_ANT0: Bluetooth; RF_ANT1: 2.4 GHz / 5 GHz Wi-Fi	85 °C	–
JODY-W562-01A	RF_ANT0: Bluetooth; RF_ANT1: 2.4 GHz and 5 GHz Wi-Fi	105 °C	–
JODY-W562-21A	RF_ANT0: Bluetooth; RF_ANT1: 2.4 GHz and 5 GHz Wi-Fi	105 °C	Wi-Fi and Bluetooth

Table 1: Available module configurations

Module integration

JODY-W5 must be integrated into the application product together with a host CPU system.
Figure 1 shows a typical integration.

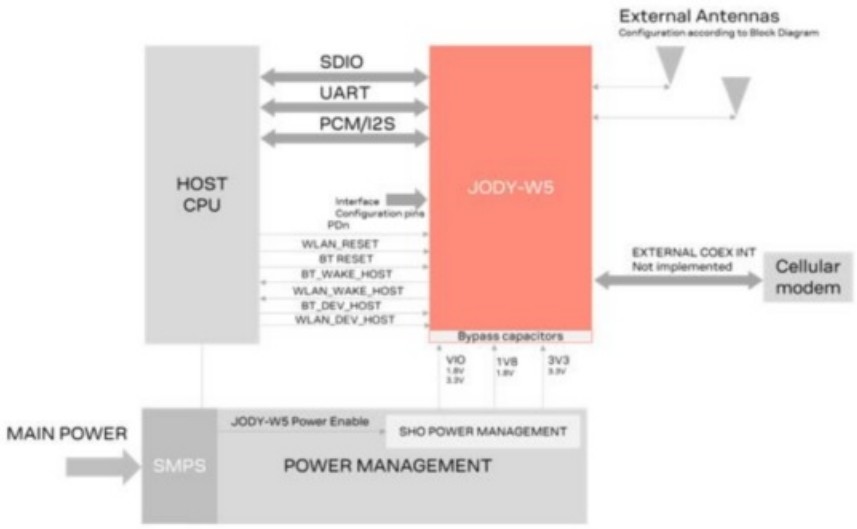


Figure 1. JODY-W5 integration in host system

- Wi-Fi 5 GHz and 2.4 GHz are combined in the diplexer and connected to the ANT1 Wi-Fi antenna pin for simultaneous operation. Bluetooth is connected separately to the ANT0 antenna pin.
- The SDIO interface is used for Wi-Fi data and downloading firmware.
- The UART interface is used for Bluetooth data.
- The preferred data and communication interface between Host CPU and JODY-W5 is set according to the instructions for Configuration pins.
- Control signals for power down, reset, and host and module wake up are available to control JODY-W5 from host CPU.
- The module is power supplied through the 3V3, 1V8, and VIO domain pins. To match the host CPU pad voltage, VIO can be set to either 1.8 V or 3.3 V.
- JODY-W562 modules have a dual antenna configuration for simultaneous Bluetooth and Wi-Fi 2.4 and 5 GHz operation through RF pins. See also Block diagram and Antenna interface in JODY-W5 data sheet [1].
- For correct operation, it is important to correctly configure JODY-W5 with the settings and startup sequences described in this document and in the JODY-W5 data sheet [1]. This configuration puts requirements for enabling the timing of power sources and the assertion of PDn.
- JODY-W5 includes a PCM /I2S interface that can be used to connect a codec for Bluetooth audio. If the interface isn't used, it can be omitted.
- The JODY-W5 product summary [17] lists the feature scope of the different JODY-W5 versions.
  This can be used to identify the JODY module that is best suited for the application product.

For a complete block diagram of JODY-W562 modules, see the data sheet [1].

2.1 Power supply interface

JODY-W5 series power supply pins 3V3, 1V8, and VIO pins must be sourced by a regulated DC power supply, such as an LDO or SMPS. The appropriate type for your design depends on the main power source of the application.

Pin	Name	I/O	Description	Remarks
2	3V3	PWR	3.3 V analog power supply	
3	VIO	PWR	VIO supply (1.8 V or 3.3 V)	
4	1V8	PWR	1.8 V analog power supply	

Table 2 Power supply pins

The DC power supply can be taken from any of the following sources:

- Switched Mode Power Supply (SMPS)
- Low Drop Out (LDO) regulator

Module power up must strictly follow the defined power-up sequence. It is important to design the power management to comply with the recommended power-up sequence.
The current consumed through the supply pins by JODY-W5 series modules can vary by several orders of magnitude depending on the operation mode and state. The current consumption can change from high consumption, experienced during Wi-Fi transmission at maximum RF power level in connected-mode, to low current consumption during the low power idle-mode when power saving is enabled. Regardless of the chosen DC power supply, it is crucial that it can satisfy the high peak current consumed by the module. When designing the supply circuitry for the module, a contingency of at least 20% over the stated peak current is recommended. See also Module supply design.

Domain	Allowable ripple (peak to peak)1 over DC supply		Current consumption, peak	
	10-100 kHz	100 kHz-1 MHz	>1 MHz	
3V3	65 mVpk-pk	25 mVpk-pk	10 mVpk-pk	TBD
1V8	65 mV	25 mVpk-pk	10 mVpk-pk	TBD
VIO	65 mVpk-pk	25 mVpk-pk	10 mVpk-pk	TBD

Table 3: Summary of voltage supply requirements

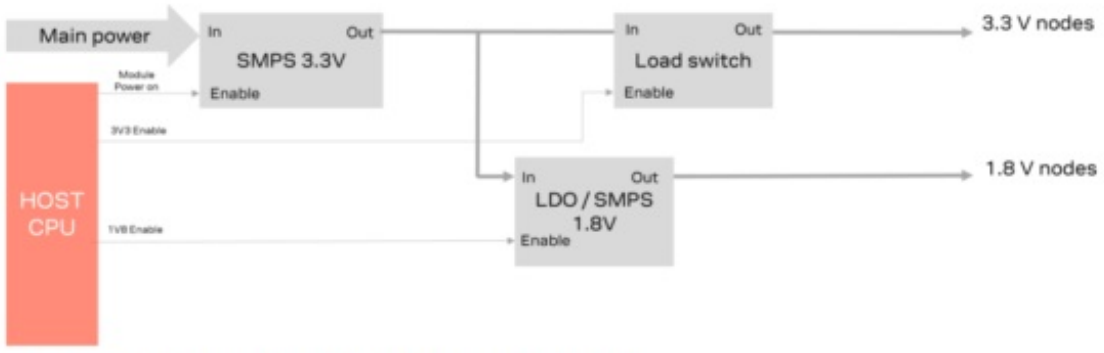


Figure 2: Proposed implementation of JODY-W5 power supply circuitry

1 Ripple measured on EVK-JODY-W5 power connectors

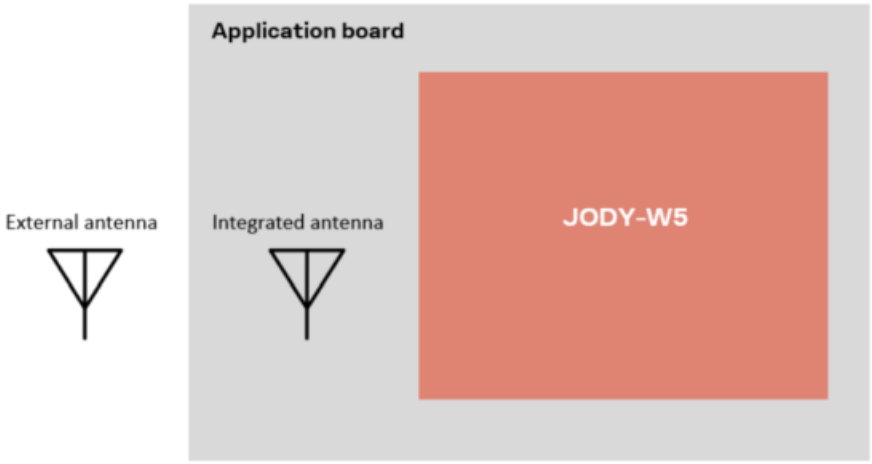
2.1.1 Digital I/O interfaces reference voltage (VIO)

The dedicated VIO pin enables integration of JODY-W5 in either 1.8 V or 3.3 V applications without the need for level converters according to the voltage level selected.
For information about the supply voltage requirements, see also the JODY-W5 series data sheet [1].

2.2 Antenna interfaces

JODY-W5 series modules include antenna pins to connect external antennas. Either integrated SMD or equivalent antennas mounted on the application board or an external antenna connected through an antenna connector and coaxial cable can be used.

Figure 3 shows the available antenna options.



External antenna

An external antenna of choice connects to the application board through the RF antenna pins, U.FL, or Reverse Polarity SMA connector on the module. Typically, a dipole antenna is connected to the module RF pins through a coaxial cable and U.FL connector on the main PCB.

Integrated antenna

A permanent antenna included into the PCB application design. Ideally, an SMD antenna mounted on the main application PCB that connects to the module RF pins (or U.FL connectors) through the RF transmission lines.

Figure 3: Antenna options

JODY-W562 module is a dual antenna configuration. Wi-Fi 5 GHz and 2.4 GHz are combined in the diplexer and connected to the ANT1 Wi-Fi antenna pin for simultaneous operation. Bluetooth is connected separately to the ANT0 antenna pin.

2.2.1 RF pins and connectors

RF pins are used to connect the Wi-Fi and Bluetooth antennas.

Pin	Name	I/O	Description	Remarks
24	ANT0	I/O, RF	JODY-W562-xxA: Bluetooth	50 Ω
29	ANT1	I/O, RF	I/O, RF JODY-W562-xxA: Wi -Fi 2 +5	50 Ω

Table 4. RF pins allocation

⚠ For proper implementation of antennas in the application product, follow the RF interface options.

⚠ To implement a design compliant with the u-blox FCC certification Grant follow the instructions in the Antenna Integration application note [11].

2.2.2 Approved antenna designs

JODY-W5 modules come with a pre-certified antenna designs that can save time and expense during the certification process. To leverage this benefit, customers are required to implement an antenna layout that is fully compliant with the u-blox reference design outlined in future versions of this document2 .

Reference design source files are available from u-blox on request.2

For Bluetooth and Wi-Fi operation, JODY-W5 modules have been tested and approved for use with the antennas featured in the list of Pre-approved antennas .
To implement a design compliant with the u-blox FCC certification Grant follow the instructions in the Antenna Integration application note [11].

2.2.3 Integrated antennas

JODY-W5 module allow SMD antennas to be mounted on the application board, connected with a transmission line to the RF_ANT pins.
For proper implementation for antennas in the application product, follow the RF interface options.

2.2.4 External antennas

External antennas can be used with JODY-W5 module. The antennas are preferably connected to the module through coaxial cable and U.FL or RPSMA connector.
External antennas are particularly suited for application products housed in metal casings that demand that the antennas are placed externally.
For proper implementation for antennas in the application product, follow the RF interface options.

⚠ To avoid invalidating the compliance and pre-certification of u-blox modules with the various regulatory bodies, use only external antennas included the list of Pre-approved antennas. u-blox modules may also be integrated with other antennas. In which case, OEM installers must certify their own designs with the respective regulatory agencies.

2.3 System function interfaces

2.3.1 Power-up sequence

Figure 4 shows the power-up sequences recommended for JODY-W5. During the power up of module, all power rails can be independently applied before PDn is set high.

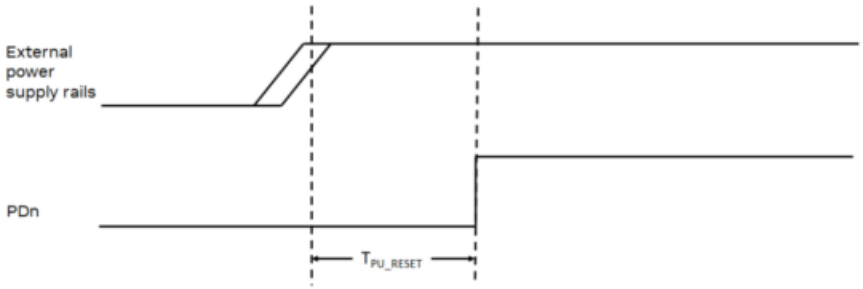


Figure 4: Power sequence of JODY-W5 module

PDn must be held low during start up and released when the power is stable, or later when the module must be turned on. PDn is powered by the 1V8 voltage domain and is connected through a 51 kΩ pull up resistor to 1V8. Optionally, the PDn pin can be left unconnected so that it follows 1V8 through the pull up resistor. In which case, the power down mode isn't accessible and a further full-power cycle must be made to reset the module.

Pin	Name	I/O	Description	Remarks
2	3V3	PWR	3.3 V analog power supply	
3	VIO	PWR	VIO supply (1.8 V or 3.3 V)	
4	1V8	PWR	1.8 V analog power supply	
58	PD#	I	Power down signal	Assert low for power down. Internal 51 kΩ pull-up to 1V8. Accepts 1.8 V to 4.5 V.

Table 5. Signals included in start-up sequence

☞ Power down mode can only be entered through PDn assertion by the host. For correct reset PDn must be

asserted for a minimum of 100 ms.

2.3.2 Reset

Although external reset isn't a prerequisite for correct operation, it can be asserted by the host controller through PDn in the event of any abnormal module behavior.
JODY-W5 series modules are reset to a default operating state by any of the following events:

- Power on (power good 90%)
- PDn assert: The device is reset when the PDn input pin is < 0.2 V and transitions from low to high

 A firmware download to the module is required after each reset. For information about downloading the firmware, see also Software.

2.3.3 Power-off sequence

JODY-W5 modules enter Power Down mode when PDn is asserted. After assertion, the power on the 3V3, 1V8, and VIO supplies can be removed. The module then enters the Power Off mode.

2.3.4 Wake-up signals

JODY-W5 series modules provide wake-up input and output signals that handle the low-power modes for both Wi-Fi and Bluetooth. See also Module supply design.
The wake-up signals are used to exit JODY-W5 or host CPU from sleep modes. Wake-up signals are powered by the VIO voltage domain. These signals are optional, out-of-band, wake-up pins that are used to wake up the transceiver from sleep mode.
Table 6 describes the various wake-up, input and output signals.

Pin	Pin name	I/O	Function	Description	Supply node
9	WL_WAKE_IN	I	WL_WAKE_IN / GPIO [16]	Multi-functional pin: Wi-Fi radio wake-up input signal GPIO [16]	VIO
10	WL_WAKE_OUT	O	WL_WAKE_OUT / GPIO[17]	Multi-functional pin: Wi-Fi radio wake-up output signal GPIO [17]	VIO
11	BT_WAKE_IN	I	BT_WAKE_IN / GPIO[18]	Multi-functional pin: Bluetooth radio wake-up input signal GPIO [18]	VIO
12	BT_WAKE_OUT	O	WL_WAKE_OUT /GPIO[19]	Multi-functional pin: Bluetooth radio wake-up output signal GPIO [19]	VIO

Table 6: Wake-up signals

2.3.5 Configuration pins

JODY-W5 series provides two configuration pins, CONFIG[0] and CONFIG[1], for selecting the host interface configuration, as shown in Table 7.
Additional configuration pins are used to set parameters following a reset. To set a configuration bit to 0, attach a 100 kΩ resistor to GND. No external pull-up resistor is required to set a configuration bit to 1. Additional configuration pins are described in Table 8.

Pin	Pin name	I/O	Function	Description	Supply node
7	CONFIG[0]	I	CONFIG_HOST_BOOT[0]	Host interface selection	1V8
8	CONFIG[1]	I	CONFIG_HOST_BOOT[1]	Host interface selection	1V8

Table 7: Host Interface selection configuration pins

Pin	Name	Description
81	RF_CNTL3_P	1 – Do not pull low during start-up
80	RF_CNTL4_N	1 – Do not pull low during start-up

Table 8: Additional configuration pins

Table 9 shows the configuration options for host interface selection.

CONFIG[1]	CONFIG[0]	Wi-Fi	Bluetooth/ Bluetooth LE	Firmware download	Number of SDIO functions
1	1	SDIO	UART	SDIO+UART (parallel/serial)	1 (Wi-Fi)
reserved	reserved				

Table 9: Host interface configuration options

2.3.6 Power states

JODY-W5 series modules have several operation states. The power states and general guidelines for Wi-Fi and Bluetooth operations are defined in Table 10.

General status	Power state	Description
Power-down	Not Powered	**3V3, 1V8**, and **VIO** supplies not present or below the operating range. The module is switched off.
	Power Down	Asserting **PDn** while **3V3, 1V8**, and **VIO** supplies are present powers down the module. This represents the lowest leakage mode of operation with active voltage rails. Register and memory states are not maintained in power-down mode. The module is automatically reset after exiting power-down mode, which means that the firmware must be downloaded again. If firmware isn't downloaded, the device must be kept in its power-down state to reduce the leakage.
Normal operation	Active	Enables TX/RX data connection with the system running at the specified power consumption.
	Deep sleep	Low-power state used in the sleep state of many power-save modes. Memory is placed in low-power retention mode.

Table 10: Description of module power states

2.4 Host interfaces

JODY-W5 series modules support SDIO 3.0 and high-speed UART host interfaces. This means that all Wi-Fi traffic is communicated through SDIO. By setting the appropriate boot option, the highspeed UART interface between the host and the JODY-W5 module is configured for the Bluetooth traffic. For information about the configuration options for the host interface, see also Configuration pins.

2.4.1 SDIO 3.0 interface

JODY-W5 series modules include a SDIO device interface that is compatible with the industrystandard SDIO 3.0 specification with a clock range of up to 208 MHz. The host controller uses the SDIO bus protocol to access the Wi-Fi function. The interface supports 4-bit SDIO transfer mode with data rates up to 50 MB/s in SDR50 or DDR50 modes. The modules also support the legacy modes, Default Speed (DS) and High-Speed (HS).

☞ The SDIO interface voltage is set to 1.8 V.

JODY-W5 modules act as devices on the SDIO bus.

Table 11summarizes the supported bus speed modes.

Bus speed mode	Max. bus speed [MB/s]	Max. clock frequency [MHz]	Interface voltage [V]
SDR104	104	208	1.8
SDR50	50	100	1.8
DDR50	50	50	1.8
SDR25	25	50	1.8
SDR12	12.5	25	1.8

Bus speed mode	Max. bus speed [MB/s]	Max. clock frequency [MHz]	Interface voltage [V]
HS: High-Speed	25	50	1.8
DS: Default Speed	12.5	25	1.8

Table 11: SDIO bus speeds

JODY-W5 includes internal 100 kΩ nominal pull-up resistors on the SDIO signals. Depending on the routing and trace impedance of the SDIO lines, it is recommended that pull-up resistors are connected to these lines. See also Data communication interfaces. Small value in-series termination resistors might also be applied to mitigate signal integrity and EMI issue.

Table 12 describes the function of each of the SDIO signals.

Pin	Name	I/O	Description	Remarks
53	SD_CLK	I	SDIO Clock input	
52	SD_CMD	I/O	SDIO Command line	External PU required
50	SD_D2	I/O	SDIO Data line bit 2	External PU required
51	SD_D3	I/O	SDIO Data line bit 3	External PU required
54	SD_D0	I/O	SDIO Data line bit 0	External PU required
55	SD_D1	I/O	SDIO Data line bit 1	External PU required
65	SD_INT	O	SDIO Interrupt output	Multiplexed with GPIO[21]

Table 12: SDIO signal definitions

SDIO interface pins are powered by the 1V8 voltage domain.

2.4.2 High-speed UART interface

JODY-W5 series modules support a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface in compliance with the industry standard 16550 specification.

The main features of the UART interface include:

- FIFO mode permanently selected for transmit and receive operations
- Two pins for transmit and receive operations
- Two flow control pins (RTS/CTS)
- Interrupt triggers for low-power, high-throughput operation
- The default baud rate is 115200 baud and can be modified using an HCI command

  The UART interface operation includes:
- Bluetooth firmware upload to the module
- Bluetooth data

  Table 13 describes the function of each of the UART signals.

Pin	Name	I/O	Description	Remarks
36	UART_SOUT	O	UART TX signal	Connect to Host RX
37	UART_SIN	I	UART RX signal	Connect to Host TX
38	UART_RTSn	O	UART RTS signal	Connect to Host CTS. Used as configuratio n pin. See also Configuration pins.
39	UART_CTSn	I	UART CTS signal	Connect to Host RTS. Used as configuration pin. See also Configuration p ins.

Table 13: UART pin description

High-Speed UART signals are powered by the VIO voltage domain.

2.4.3 PCM/I2S – Audio interface

JODY-W5 series modules include a bi-directional, 4-wire, PCM digital audio interface to connect an external digital audio devices like an audio codec.

The interface supports:

- PCM main node or sub node modes
- PCM bit width size of 8 bit or 16 bit
- Up to four PCM slots with configurable bit width and start positions
- PCM short frame and long frame synchronization
- I2S main node and sub node modes for I2S, MSB, and LSB audio interfaces

☞ PCM pins are shared with the I2S interface and configured to I2S mode using HCI commands.
Table 14 describes the function of each of the PCM digital audio signals.

Pin	Name	I/O	Description	Remarks
16	PCM_CLK	I/O	PCM clock. Alternate function: I2S clock	Main node output. Sub node input.
	PCM_MCLK	O	PCM main node clock	Optional clock used by some codecs
15	PCM_SYNC	I/O	PCM frame sync. Alternate function: I2S word select	Main node output. Sub node input.
18	PCM_DIN	I	PCM data in. Alternate function: I2S data in	
17	PCM_DOUT	O	PCM data out. Alternate function: I2S data out	

Table 14: PCM digital audio signal descriptions
PCM/I2S signals are powered by the VIO voltage domain.

2.5 Internal coexistence interface

JODY-W5 includes an internal coexistence arbitrarer handling Wi-Fi and Bluetooth 5.4 coexistence.

2.6 External coexistence interface

The included WCI-2 and PTA interface can operate coexistence with an external radio.
The external radio must be connected to the 2-wire wireless coexistence interface 2 (WCI-2). The WCI-2 message and message type comply with Bluetooth special interest group (SIG) core specification volume 7, part C.
Table 18 describes the function of each of the external coexistence signals.

Pin	Pin name	I/O type	Description	GPIO pin multiplexing
91	EXT_STATE	I	External radio state input signal External radio traffic direction (Tx/Rx): · 1: Tx · 0: Rx	GPIO[12]
88	EXT_GNT	O	External radio grant output signal	GPIO[14]
92	EXT_FREQ	I	External radio frequency input signal Frequency overlap between external radio and Wi-Fi: · 1: overlap · 0: non-overlap This signal is useful when the external radio is a frequency hopping device.	GPIO[20]
90	EXT_PRI	I	External radio input priority signal Priority of the request from the external radio. Can support 1 bit priority (sample once) and 2-bit priority (sample twice). Can also have Tx/Rx information following the priority information if EXT_STATE isn't used.	GPIO[15]
89	EXT_REQ	I	Request from the external radio	GPIO[13]
14	WCI-2_SIN	I	WCI-2 serial interface input	GPIO[25]
13	WCI-2_SOUT	O	WCI-2 serial interface output	GPIO[26]

Table 15: External coexistence interface description

2.7 JTAG

The module includes a JTAG test interface that is supported using the GPIO pins.

Pin	Pin name	I/O type	Description	GPIO pin multiplexing
32	JTAG_TCK	I	JTAG test clock input signal	GPIO[28]
33	JTAG_TMS	I	JTAG controller select input signal	GPIO[29]
86	JTAG_TDI	I	JTAG test data input signal	GPIO[30]
85	JTAG_TDO	O	JTAG test data output signal	GPIO[31]

Table 16: JTAG interface description

2.8 Other remarks

2.8.1 Unused pins

JODY-W5 series modules have unconnected (NC) pins that are reserved for future use. These pins must be left unconnected on the application board.

Design-in

Follow the design guidelines in this chapter to optimize the integration of JODY-W5 series modules in the final application board.

3.1 Overview

Although all application circuits must be properly designed, and the following aspects of the application design require special attention:

- Module antenna integration. RF_ANT.
  o Antennas and RF circuits affect the RF performance and certification compliance. It is important to follow the design instructions given here to reach specified performance.
  Furthermore, to maintain compliance and subsequent certification of the application design, it is important to observe the applicable parts of antenna schematic and layout described in [19].
- Module power supply. Power and GND.
  o Power supply circuits might affect the RF performance. It is important to select a suitable device capable to source the adequate voltage and current. It is also important to implement adequate power and ground planes in PCB stack-up and to implement bypass capacitors for these supplies. See also Supply interfaces.
- High-speed interfaces, such as PCIe, SDIO, high-speed UART, and PCM.
  o High-speed interfaces are a potential source of noise that can affect the regulatory compliance of standards for radiated emissions. It is important to follow the schematic and layout design recommendations described in SDIO 3.0 interface and the General high-speed layout guidelines.
- System functions: Power Down, Reset and Configuration pins.
  o Careful utilization of these pins in the application design is necessary to ensure that the module operates as it should. Specifically, observe the state and voltage level is correctly defined during module boot and operation.
  It is important to follow the pin design described in the General high-speed layout guidelines.
- Other pins: specific signals.
  o Careful utilization of these pins is necessary to ensure that the module operates as it should.
  It is important to follow the schematic and design layout recommendations.
- NC pins must not be connected.

3.2 RF interface options

Short range modules provide several RF-interface options for connecting external antennas. Module variants also provide internal or embedded antennas which special consideration when designing the host PCB:

- The RF_ANT ports have a nominal characteristic impedance of 50Ω. For correct impedance matching, these ports must be connected to the respective antenna through a 50Ω U.FL connector and coax or a transmission line – depending on the type of module connector. Poor termination of RF_ANT pins can result in degraded performance of the module.
- To optimize the isolation between the antennas and ensure good application performance in multiple antenna products, such as MIMO, follow the requirements given in Table 17 and Table 18.

 According to FCC regulations, the transmission line from the module antenna pin to the physical antenna (or antenna connector on the host PCB) is considered part of the approved antenna design. Therefore, module integrators must use exactly the antenna reference design used in the module FCC type approval or certify their own design.
For instructions on how to design circuits that comply with these requirements, see [19].

3.2.1 Antenna design

To optimize the radiated performance of the final product, the selection and placement of both the module and antenna must be chosen with due regard to the mechanical structure and electrical design of the product. To avoid later redesigns, it is important to decide the positioning of these components at an early phase of the product design.

The compliance and subsequent certification of the RF design depends heavily on the radiating performance of the antennas.
To ensure that the RF certification of JODY-W5 modules is extended through to the application design, carefully follow the guidelines outlined below.

- External antennas, including, linear monopole classes:
  o Place the module and antenna in any convenient area on the board. External antennas do not impose any restriction on where the module is placed on the PCB.
  o Select antennas with an optimal radiating performance in the operating bands. The radiation performance depends mainly on the antennas.
  o Choose RF cables that offer minimum insertion loss. Unnecessary insertion loss is introduced by low quality or long cables. Large insertion losses reduce radiation performance.
  o Use a high-quality 50 Ω coaxial connector for proper PCB-to-RF-cable transition.
- Integrated antennas, such as patch-like antennas:
  o Internal integrated antennas impose some physical restrictions on the PCB design:
  – Integrated antennas excite RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated. Consequently, the orientation of the ground plane relative to the antenna element must be considered.
  – Find a numerical example to estimate the physical restrictions on a PCB, where:
  Frequency = 2.4 GHz → Wavelength = 12.5 cm → Quarter wavelength = 3.5 cm in free space or 1.5 cm on a FR4 substrate PCB.
- Choose antennas with optimal radiating performance in the operating bands. Radiation performance depends on the complete product and antenna system design, including the mechanical design and usage of the product. See also Table 17.
- Make the RF isolation between the system antennas as high as possible and make the correlation between the 3D radiation patterns of the two antennas as low as possible. In general, RF separation of at least a quarter wavelength between the two antennas is required to achieve a minimum isolation and low pattern correlation. If possible, increase the separation to maximize the performance and fulfill the requirements described in Table 17.

Table 17 summarizes the requirements for the antenna RF interface.

Item	Requirements	Remarks
Impedance	50 W nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 W impedance of Antenna pins.
Frequency Range	2400 – 2500 MHz 5150 – 5895 MHz	For 802.11b/g/n/ax and Bluetooth. For 802.11a/n/ac/ax.
Return Loss	S11 < -10 dB (VSWR < 2:1) recommended S11 < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S11, as the VSWR, refers to the amount of reflected power, measuring how well the primary antenna RF connection matches the 50 W characteristic impedance of antenna pins. The impedance of the antenna termination must match as much as possible the 50 W nominal impedance of antenna pins over the operating frequency range, to maximize the amount of power transferred to the antenna.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	Radiation efficiency is the ratio of the radiated power to the power fed to the antenna input: the efficiency is a measure of how well an antenna receives or transmits.
Maximum Gain		To comply with regulatory agencies radiation exposure limits the maximum antenna gain must not exceed the value specified in type approval documentation.

Table 17: Summary of antenna interface requirements
Table 18 specifies additional requirements for implementing a dual antenna design.

Item	Requirements	Remarks
Isolation (in-band)	S21 > 30 dB recommended	The antenna-to-antenna isolation is the S21 parameter between the two antennas in the band of operation. Lower isolation might be acceptable depending on use- case scenario and performance requirements.
Isolation (out-of-band)	S21 > 35 dB recommended S21 > 30 dB acceptable	Out-of-band isolation is evaluated in the band of the aggressor. This ensures that the transmitting signal from the other radio is sufficiently attenuated by the receiving antenna. It also avoids any saturation and intermodulation effect on the receiver port.
Envelope Correlation Coefficient (ECC)	ECC < 0.1 recommended ECC < 0.5 acceptable	The ECC parameter correlates the far field parameters between antennas in the same system. A low ECC parameter is fundamental in improving the performance of MIMO-based systems.

Table 18: Summary of Wi-Fi/Bluetooth coexistence requirements

⚠ When operating dual antennas in the same 2.4 GHz band, sufficient isolation is critical for attaining an optimal throughput performance in Wi-Fi/Bluetooth coexistence mode.
Select antennas that provide:

- Optimal return loss (or VSWR) over all the operating frequencies.

- Optimal efficiency figure over all the operating frequencies.
- An appropriate gain that does not exceed the regulatory limits specified in some regulatory country authorities like the FCC in the United States.

A useful approach for the antenna microstrip design is to place a U.FL connector close to the embedded PCB or chip antenna. The U.FL connector only needs to be mounted on units used for verification.

3.2.1.1 Integrated antenna design

If integrated antennas are used, the transmission line is terminated by the antennas themselves or by the antenna together with the connected coaxial cable and U.FL plug.
Consider the following the guidelines when designing the antenna:

- The antenna design process should commence at the same time as the mechanical design of the product. PCB mock-ups are useful in estimating overall efficiency and radiation path of the intended design during early development stages.
- Use antennas designed by an antenna manufacturer that provide the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the related integrated antenna requirements. The ground plane of the application PCB may be reduced to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated. The overall antenna efficiency may benefit from larger ground planes.
- Proper placement of the antenna and its surroundings is also critical for antenna performance. Avoid placing the antenna close to conductive or RF-absorbing parts, such as metal objects or ferrite sheets. These parts may absorb part of the radiated power, shift the resonant antenna frequency of the antenna, or otherwise affect the antenna radiation pattern.
- Ensure that correct the installation and deployment of the antenna system, including PCB layout and matching circuitry, is done correctly. In this regard, it is recommended that you strictly follow the specific guidelines provided by the antenna manufacturer.
- Further to the custom PCB and product restrictions, antennas may also require tuning/matching to reach the target performance. It is recommended that you plan measurement and validation activities with the antenna manufacturer before releasing the end-product to manufacturing.
- The receiver section may be affected by noise sources like hi-speed digital busses. Avoid placing the antenna close to busses as DDR. Otherwise, consider taking specific countermeasures, like metal shields or ferrite sheets, to reduce the interference.
- Be aware of interaction between co-located RF systems, like LTE sidebands on 2.4 GHz band. Transmitted power can interact or disturb the performance of JODY-W5 modules if an LTE filter isn't included in the design.

3.2.1.2 RF transmission line design

RF transmission lines, such as those that connect from RF_ANT pins to their related antenna connectors or antenna, must be designed with a characteristic impedance of 50Ω.
Figure 5 shows the design options and the most important parameters for designing a transmission line on a PCB:

- Microstrip – track separated with dielectric material and coupled to a single ground plane.
- Coplanar microstrip – track separated with dielectric material and coupled to both the ground plane and side conductor.
- Stripline – track separated by dielectric material and sandwiched between two parallel ground planes.

The most common transmission line implementation is the coplanar microstrip, as shown in Figure 5.

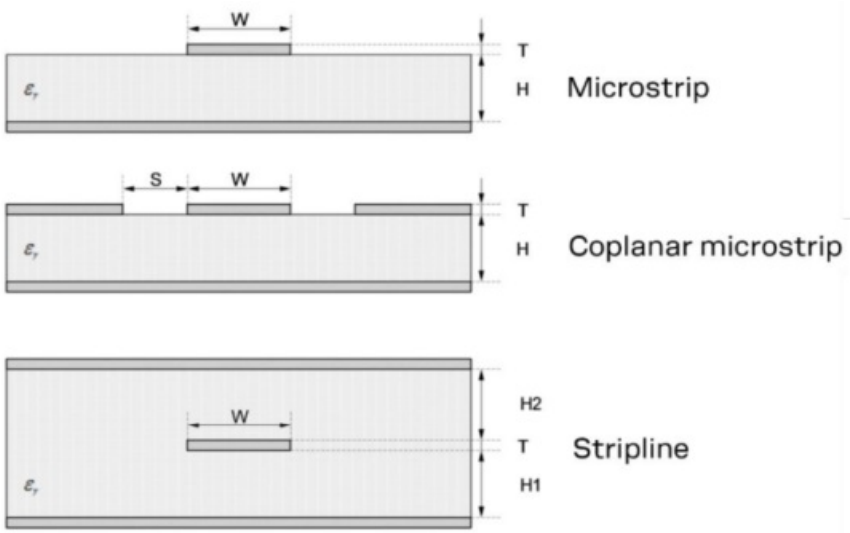


Figure 5: Transmission line trace design

Follow these recommendations to design a 50Ω transmission line correctly:

- Designers must provide enough clearance from surrounding traces and ground in the same layer.
  In general, the trace to ground clearance should be at least twice that of the trace width. The transmission line should also be “guarded” by the ground plane area on each side.
- In the first iteration, calculate the characteristic impedance using tools provided by the layout software. Ask the PCB manufacturer to provide the final values usually calculated using dedicated software and production stack-ups. It is sometimes possible to request an impedance test coupon on side of the panel to measure the real impedance of the traces.
- Although FR-4 dielectric material can result in high losses at high frequencies, it can still be an appropriate choice for RF designs. In which case, aim to:
  o Minimize RF trace lengths to reduce dielectric losses.
  o If traces longer than few centimeters are needed, use a coaxial connector and cable to reduce losses.
  o For good impedance control over the PCB manufacturing process, design the stack-up with wide 50 Ω traces with width of at least 200 µm.
  o Contact the PCB manufacturer for specific tolerance of controlled impedance traces. As FR-4 material exhibits poor thickness stability, it gives less control of impedance over the trace width.
- For PCBs with components larger than 0402 and dielectric thickness below 200 µm, add a keep-out, that is, some clearance (void area) on the ground reference layer below any pin on the RF transmission lines. This helps to reduce the parasitic capacitance to ground.
- Route RF lines in 45° angle and avoid acute angles. The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible.
- Add GND stitching vias around transmission lines.
- Provide a sufficient number of vias on the adjacent metal layer. Include a solid metal connection between the adjacent metal layer on the PCB stack-up to the main ground layer.
- To avoid crosstalk between RF traces and Hi-impedance or analog signals, route RF transmission lines as far from noise sources (like switching supplies and digital lines) and any other sensitive circuit.
- Avoid stubs on the transmission lines. Any component on the transmission line should be placed with the

connected pin located over the trace. Also avoid any unnecessary components on RF traces.

Figure 6 shows a trace and ground design example. From top left to bottom right: layer 1 mirrored, layer 1, layer 2, layer 3, layer 4, and so on.

Figure 6: RF trace and ground design example

Figure 7 shows typical artwork implementing a coplanar microstrip on an 8-layer PCB. The trace includes, from the module pad to the PCB edge, the (module-side) coplanar microstrip section, RF connector with switch (optional), impedance matching PI network, (SMA-side) coplanar microstrip section (2), and edge mounted SMA RF connector. The ground clearance on L2 and L3 allows for awider microstrip, which is less lossy than a narrow one. The ground clearance is especially critical in the 5 GHz band. A wider trace also has less impedance variation over PCB production batches due to the absolute tolerances in the PCB etching process.

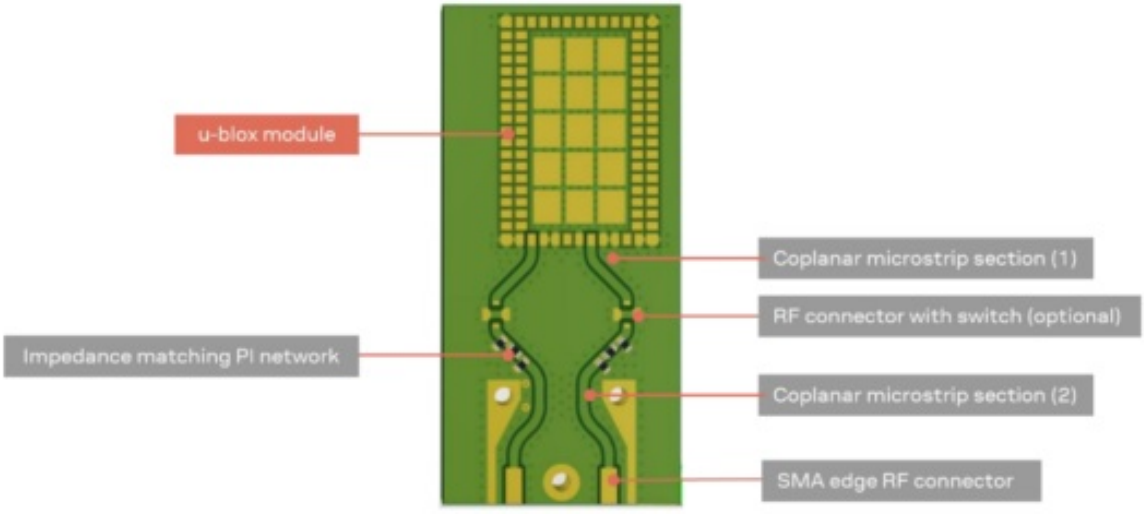


Figure 7: Layout example showing implementation

Figure 8 shows layout of pins for a U.FL connector. Pay particular attention to the GND clearance under the signal pad.

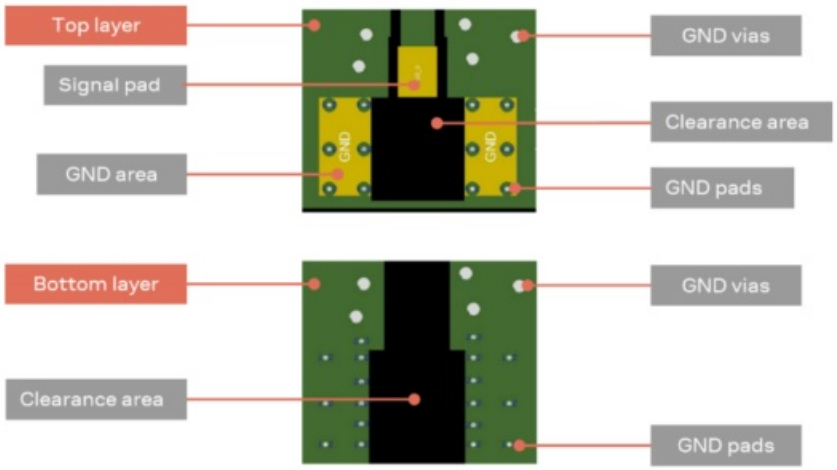


Figure 8: U.FL connector layout, top layer (left), and inner layer 1 (right)

3.3 Supply interfaces

3.3.1 Module supply design

Although the GND pins are internally connected, it is advisable to connect all available ground pins on the application board to solid ground with a good (low impedance) connection to external ground. This minimizes power loss, improves RF performance, and betters thermal performance.

Good connection of the module supply pins, supplied by a DC supply source, is required for accurate RF performance.

Consider the following guidelines when developing the schematic:

- All power supply pins must be connected to an appropriate DC source.
- Any series component with an Equivalent Series Resistance (ESR) greater than a few milliohms (mΩ) should be avoided. The only exception to this general rule is the use of ferrite beads for DC filtering. To avoid possible instability in the DC supply, only use ferrite beads if needed.
- For high-frequency filtering, additional bypass capacitors in the range of 100 nF to 1 µF are required on all supply pins. Offering low ESR/ESL resistance, a class II ceramic capacitor with an X7R or X5R dielectric is well suited for this purpose. Bypass capacitors of a smaller size can be chosen to minimize ESL (Equivalent Series Inductance) in the manufacturing process. The capacitor should be placed as close as possible to the module supply pin.
- To help filter current spikes from the RF section and avoid ground bounce, a minimum bulk capacitance of 10 µF should be applied to the 1V8 and 3V3 rails (optionally on VIO) and placed close to the module supply pins. Offering low ESR/ESL resistance, a class II ceramic capacitor with an X7R or X5R dielectric is well suited for this purpose. Special care should be taken in the selection of X5R/X7R dielectrics due to capacitance derating versus DC bias voltage.

3.3.1.1 Guidelines for supply circuit design using an SMPS

When choosing between a Switched Mode Power Supply (SMPS) or Low Drop-Out (LDO) regulator to supply the modules, it is advisable to consider the acceptable power and thermal dissipation of the application product.

An SMPS is generally recommended for converting the main supply to the module supply when the voltage difference is relatively high. In these circumstances, the use of an SMPS dissipate less power and subsequently generates less power dissipation and heat than an LDO.

By contrast, an LDO is generally simpler to use and does not generate the amount of noise an SMPS might. See also Guidelines for supply circuit design using a Low Drop-Out (LDO) linear regulator.

To avoid degrading the module stability, RF performance, or violate spurious emission standards, the characteristics of the SMPS should meet the following prerequisites:

- Power capability: The regulator, together with any additional filter in front of the module, must be capable of

providing a voltage within the specified operating range. It must also be capable of delivering the specified peak current.

- Low output ripple: The peak-to-peak ripple voltage of the switching regulator must not exceed the specified limits. This requirement is appliable to both the voltage ripple generated by the SMPS at operating frequency and the high-frequency noise generated by power switching.
- PWM/PFM mode operation: It is advisable to select regulators that support a fixed Pulse Width Modulation (PWM) mode. Pulse Frequency Modulation (PFM) mode typically exhibits higher ripple and can affect RF performance. If power consumption isn't a primary concern, PFM/PWM mode transitions should be avoided in favor of fixed PWM operation to reduce the peak-to-peak noise on voltage rails. Switching regulators with a mixed PWM/PFM mode can be used provided that the PFM/PWM modes and transition between modes complies with the requirements.

3.3.1.2 Guidelines for supply circuit design using a LDO linear regulator

The use of a linear regulator is appropriate when the difference between the available supply rail and the module supply is relatively low. Linear regulators can also be considered for powering 1.8 V domains – particularly those having low current requirements and those cascaded from an SMPSgenerated low voltage rail.
The characteristics of the Low Drop-Out (LDO) linear regulator used to power the voltage rails must meet the following prerequisites to comply with the requirements summarized in Table 3.

- Power capabilities: The LDO linear regulator must be able to provide a voltage within the specified operating range. It must also be capable of withstanding and delivering the maximum specified peak current while in "connected mode".
- Power dissipation: The power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range. The worst-case junction temperature can be estimated as shown below:

??,??? = (??? – ????) ∗ ???? ∗ ??? + ??

Where: ??? is the junction-to-ambient thermal resistance of the LDO package[3] , ???? is the current consumption of the given voltage rail in continuous TX/RX mode and ?? is the maximum operating temperature of the end product inside the housing.
3 Thermal dissipation capability reported on datasheets is usually tested on a reference board with adequate copper area (see also JESD51 [10]). Junction temperature on a typical PCB can be higher than the estimated value due to the limited space to dissipate the heat. Thermal reliefs on pads also affect the capability of a device to dissipate heat.

3.4 Data communication interfaces

3.4.1 SDIO 3.0

The high data rates of SDIO 3.0 bus in JODY-W5 series modules requires that special care must be taken to guarantee signal integrity and minimize electromagnetic interference (EMI) issues. The signals should be routed with a single-ended impedance of 50 Ω.
It is advisable to route all signals in the bus so that they have the same length and the appropriate grounding in the surrounding layers. The total bus length should be kept to a minimum. To minimize crosstalk with other parts of the circuit, the layout of the SDIO bus should be designed with adequate isolation between the signals, clock, and surrounding busses/traces.
Implement an undisrupted return-current path in close vicinity to the signal traces.
Figure 9 shows an optional application schematic for the SDIO bus in JODY-W5. Even though JODY-W5 includes on chip Pull-up resistors, it is advisable to add external ones for optimum pull-up to match routing and host CPU impedance.

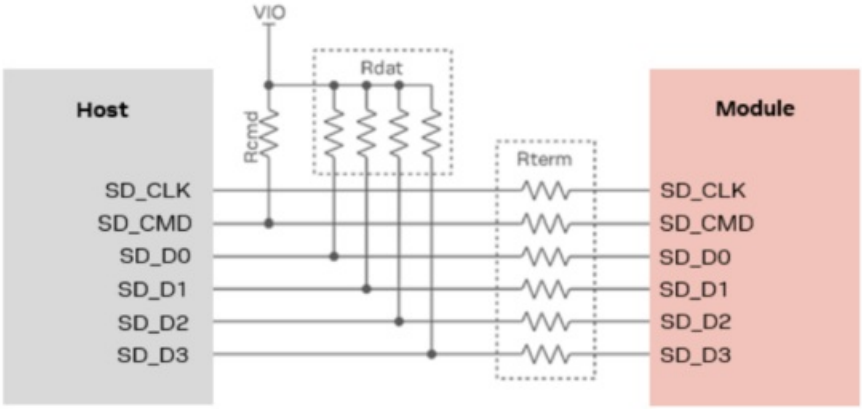


Figure 9: SDIO application schematic

☞ A small value capacitor in the range of a few pF to GND might be considered for SDIO_CLK as an EMI debug option and signal termination. This capacitor should be placed as close as possible to the JODY-W5 clock input pin and can be assembled only for EMI purpose. The capacitor value adds to total line capacitance and must not exceed total allowed capacitance to avoid violating clock rise and fall timing specifications.

☞ Small value “Rterm” series resistors, 10-22 Ω, are optionally included to mitigate interface signal integrity and EMI issues.

Table 19 summarizes the electrical requirements of the SDIO bus.

Signal group	Parameter	Min.	Typ.	Max.	Unit
CLK, CMD, DAT[0:3]	Single ended impedance, $?_0$		50		Ω
CLK, CMD, DAT[0:3]	Impedance control	?0 – 10%	?0	?0 + 10%	Ω
DAT[0:3]	Pull-Up range, Rdat	10	47	100	kΩ
CMD	Pull-Up range, Rcmd	10	10	50	kΩ
CLK, CMD, DAT[0:3]	Series termination (Host side), Rterm[4]	0	0		Ω
CLK, CMD, DAT[0:3]	Bus length[5]			100	mm
CMD, DAT[0:3]	Bus skew length mismatch to CLK	-3		+3	mm
CLK	Center-to-center CLK to other SDIO signals[6]	4*W			
CMD, DAT[0:3]	Center-to-center between signals[11]	3*W			

Table 19: SDIO bus requirements

3.4.2 High-speed UART interface

The high-speed UART interface for the JODY-W5 complies with the HCI UART Transport layer. The module uses the settings shown in Table 20.

UART Settings	
Baud rate default after reset	115 200 baud
Baud rate default after firmware load	115 200 baud
Data bits	8
Parity bit	No parity
Stop bit	1 stop bit
Flow Control	RTS/CTS

Table 20: HCI UART transport layer settings

RTS/CTS flow control is used to prevent temporary UART buffer overrun.

- If CTS is 1 the Host/Host Controller is allowed to send.
- If CTS is 0 the Host/Host Controller isn't allowed to send.

☞ The use of hardware flow control with RTS/CTS is mandatory.
Table 20 shows the possible baud rates for the UART interface.

Baud rate				
1 200	38 400	460 800	1 500 000	3 000 000
2 400	57 600	500 000	1 843 200	
4 800	76 800	921 600	2 000 000	
9 600	115 200	1 000 000	2 100 000	
19 200	230 400	1 382 400	2 764 800	

Table 21: Possible baud rates

4 Series termination values larger than typical recommended only for addressing EMI issues
5 Routing should minimize the total bus length.
6 To accommodate BGA escape, center-to-center spacing requirements can be ignored for up to 10 mm of routed length.
After a hardware reset, the UART interface is configured for 115 200 baud. A host application can configure the desired baud rate for the UART interface with the vendor specific HCI command HCI_CMD_MARVELL_UART_BAUD.
HCI command syntax using hcitool:
hcitool –i hci0 cmd 0x3F 0x0009 <4-byte value for baud rate>
In the following example, the baud rate is set to 3 000 000 baud.
$ hcitool –i hci0 cmd 0x3F 0x0009 0xC0 0xC6 0x2D 0x00
< HCI Command: ogf 0x3f, ocf 0x0009, plen 4 C0 C6 2D 00
> HCI Event: 0x0e plen 4 01 7A 0C 00
The HCI event notification is transmitted to the host at the old baud rate. Once the host receives the command, it can switch to the new baud rate and then wait for 5 ms or more before sending the next command.
3.5 Other interfaces
All pins have internal keeper resistors. Leave un-used pins open.
3.6 General high-speed layout guidelines

These guidelines describe best practices for the layout of all high-speed busses on JODY-W5.
Designers should prioritize the layout of higher speed busses. Low frequency signals, other than those with high-impedance traces, are generally not critical to the layout.
⚠ Low frequency signals with high-impedance traces (such as signals driven by weak pull resistors) can be affected by crosstalk. For these high impedance traces, a supplementary isolation of 4*W from other busses is recommended.

3.6.1 General considerations for schematic design and PCB floor planning

- Verify which signal bus requires termination and add appropriate series resistor terminations to the schematics.
- Carefully consider the placement of the module with respect to the antenna position and host processor; minimize RF trace length first and then the SDIO bus length.
- SDIO bus routing must aim to keep layer-to-layer transition to a minimum.
- Verify the allowable stack-ups and the controlled impedance dimensioning for antenna traces and busses with the PCB manufacturer.
- Verify that the power supply design and power sequence are compliant with the JODY-W5 specifications described in Power-up sequence and [19].

3.6.2 Component placement

- Accessory parts, like bypass capacitors, must be placed as close as possible to the module to improve filtering capability. Prioritize placing the smallest capacitors close to module pins.
- Do not place components close to the antenna area. Follow the recommendations of the antenna manufacturer to determine distance of the antenna in relation to other parts of the system.
  Designers should also maximize the distance of the antenna to High-frequency busses, like DDRs and related components. Alternatively, consider an optional metal shield to reduce interferences that might otherwise be picked up by the antenna and subsequently reduce module sensitivity.

3.6.3 Layout and manufacturing

- Avoid stubs on high-speed signals. Test points or component pads should be placed over the PCB trace.
- Verify the recommended maximum signal skew for differential pairs and length matching of buses.
- Minimize the routing length; longer traces degrade signal performance. Ensure that maximum allowable length for high-speed busses isn't exceeded.
- Ensure to track your impedance matched traces. Consult early with your PCB manufacturer for proper stack-up definition.
- RF, analog, and digital sections should have dedicated and clearly separated areas on the board.
- No digital routing is allowed in the GND reference plane area of RF traces (ANT pins and Antenna).
- Designers are strongly recommended to avoid digital routing beneath all layers of RF traces.
- Ground cuts or separation are not allowed below the module.
- As a first priority, minimize the length of the RF traces. Then, minimize bus length to reduce potential EMI issues related to the radiation of digital busses.
- All traces (Including low speed or DC traces) must couple with a reference plane (GND or power).
  High-speed busses should be referenced to the ground plane. If designers need to change the ground reference, an adequate number of GND vias must be added in the area of transition. This facilitates a low-impedance path between the two GND layers for the return current.
- Hi-speed busses are not allowed to change reference plane. If a change to the reference plane is unavoidable,

some capacitors should be added in the area to provide a low impedance return path through the various reference planes.
- Trace routing should maintain a distance that is greater than 3*W from the edge of the ground plane routing.
- Power planes should maintain a safe distance from the edge of the PCB. The distance must be sufficient to route a ground ring around the PCB, and the ground ring must then be stitched to other layers through vias.
- Route the power supply in low impedance power planes. If you choose to route the power supply with traces, do not route loop structures.

⚠ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of application baseboards under JODY-W5 series modules. Avoid placing temperature-sensitive devices close to the module and provide these devices with sufficient grounding to transfer generated heat to the PCB.

3.7 Module footprint and paste mask

Figure 10 shows the pin layout of JODY-W5 series modules. Detailed mechanical drawing and measures are shown in [1]. The proposed land pattern layout complements the pin layout of the module. Both Solder Mask Defined (SMD) and Non Solder Mask Defined (NSMD) pins can be used with adherence to the following considerations:

- All pins should be Non-Solder Mask Defined (NSMD)
- To help with the dissipation of the heat generated by the module, GND pads must have good thermal bonding to PCB ground planes.

The suggested stencil for the copper pad layout of the outer pads on the module is described in Figure 10.

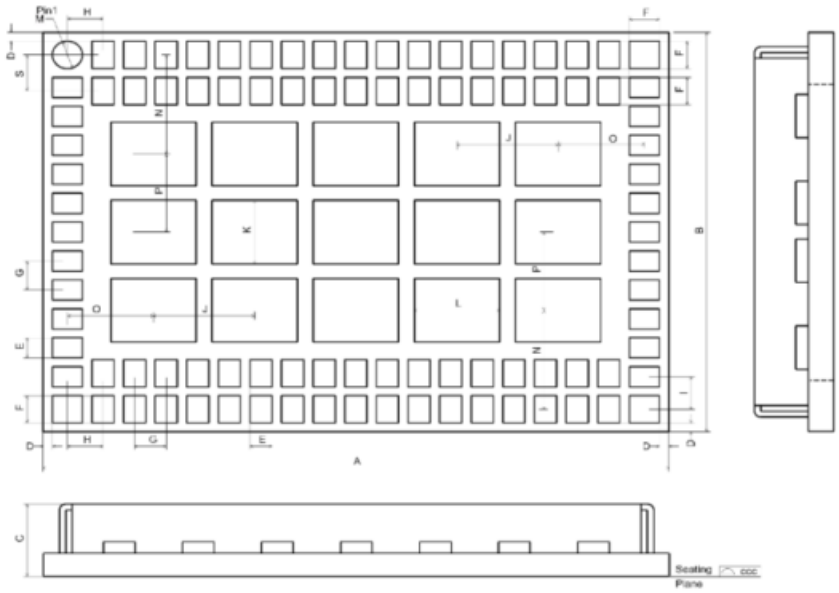


Figure 10: Recommended footprint for JODY-W5, bottom view

When deciding the layout for the central pads, you should use a special solder paste pattern with the following characteristics:

- Solder paste area should be split in several smaller parts. Typically, four to nine parts – depending on copper pad area.
- Total solder paste area should cover about 50% to 60% of copper thermal pad area.
- Total solder paste area must not exceed 65% of copper thermal pad area.

Neglecting paste optimization can lead to poor soldering quality in production.
A suggested implementation of the stencil opening for inner thermal pads is shown in Figure 11, where the outer rectangle represents the pad and the four gray rectangles represent the aperture in the solder stencil. Solder paste is only applied to the four gray rectangles.

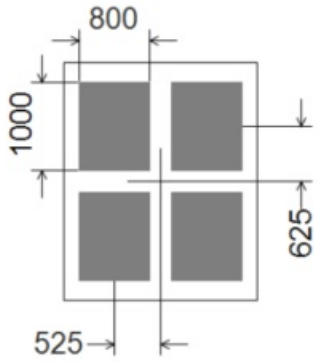


Figure 11: Stencil opening example for inner thermal pads (dimensions in µm)

⚠ The exact mask geometries, distances, and stencil thicknesses must be adapted to the specific production process chosen by the customer.

3.8 Thermal guidelines

JODY-W5 series modules are designed to operate from -40 °C to +85 °C, or -40 °C to +105 °C at an ambient temperature inside the enclosure box. The board generates heat during high loads that must be dissipated to sustain the lifetime of the components.
The improvement of thermal dissipation in the module decreases its internal temperature and consequently increases the long-term reliability of device applications operating at high ambient temperatures.
For best performance, layouts should adhere to the following guidelines:

- Vias specification for ground filling: 300/600??, with no thermal reliefs allowed on vias.
- Ground via densities under the module: 50 ????/??2 ; thermal vias can be placed in gaps between the thermal pads of the module.
- Minimum layer count and copper thickness: 4 ??????, 35 ??.
- Minimum board size: 55?70 ??.
- To optimize the heat flow from the module, power planes and signal traces should not cross the layers beneath the module.

These recommendations facilitate a design that is capable of achieving a thermal characterization parameter of ψ?? = ??? °?/? for -40 °C to +85 °C where, ?? refers to the junction between the module and the bottom side of the main PCB characterization parameter.
Use the following hardware techniques to further improve thermal dissipation in the module and optimize its performance in customer applications:

- Maximize the return loss of the antenna to reduce reflected RF power to the module.
- Improve the efficiency of any component that generates heat, including power supplies and processor, by dissipating it evenly throughout the application device.
- Provide sufficient ventilation in the mechanical enclosure of the application.
- For continuous operation at high temperatures, particularly in high-power density applications or smaller PCB sizes, include a heat sink on the bottom side of the main PCB. The heat sink is best connected using electrically insulated / high thermal conductivity adhesive7.

3.9 ESD guidelines

JODY-W5 modules are manufactured using a highly automated process, which complies with IEC61340-5-1 [6] (STM5.2-1999 Class M1 devices) standard. Customer on-site manufacturing processes that satisfy the basic ESD control program are sufficient to comply with the necessary precautions8 for handling the modules.
Table 22 describes the target ESD ratings of the JODY-W5 pins – subject to module qualification.

Application	Category	Immunity level
All exposed surfaces of the radio equipment and an y ancillary equipment in the end product.	Contact discharge	4 kV
	Air discharge	8 kV

Table 22: ESD immunity rating for pins of the JODY-W5 module
7 Typically not required.
8 Minimum ESD protection level for safe handling is specified in JEDEC JEP155 (HBM) and JEP157 (CDM) for ±500 V and ±250 V respectively.
In compliance with the following European regulations, designers must implement proper protection measures against ESD events on any pin exposed to end users:

- ESD testing standard CENELEC EN 61000-4-2 [4]
- Radio equipment standard ETSI EN 301 489-1 [5]

The minimum requirements as per these European regulations are summarized in Table 23.

Application	Category	Immunity level
All exposed surfaces of the radio equipment and an y ancillary equipment in the end product.	Contact discharge	4 kV
	Air discharge	8 kV

Table 23: Minimum ESD immunity requirements based on EN 61000-4-2
Compliance with the protection levels specified in EN 61000-4-2 [4] are fulfilled by including proper ESD protection in parallel to any susceptible trace that is close to areas accessible to end users.
⚠ Special care should be taken with the RF_ANT pins that must be protected by choosing an ESD absorber with adequate parasitic capacitance. For 5 GHz operation, a protection with maximum internal capacitance of 0.1 pF is advised.

3.10 Design-in checklists

3.10.1 Schematic checklist

- Check that the module pins have been properly numbered and designated in the schematic (including thermal pins). See Pin list.
- Power supply design complies with the voltage supply requirements in Table 3 and the power supply requirements described in the module data sheet [1].
- The Power-up sequence has been properly implemented
- Adequate bypassing has been included in front of each power pin.
- Each signal group is consistent with its own power rail supply or proper signal translation has been provided. See pin list in [19].
- Configuration pins are properly set at bootstrap. See Configuration pins.
- SDIO bus includes series resistors and pull-ups, if needed. See also Figure 9 and SDIO 3.0.

- Unused pins are properly terminated, normally unconnected. See pin list in [19].
- A pi-filter is provided in front of each antenna for final matching.

3.10.2 Layout checklist

- PCB stack-up and controlled impedance traces follow the recommendations given by the PCB manufacturer. See RF transmission line design.
- All pins are properly connected, and the footprint follows u-blox pin design recommendations. See Module footprint and paste mask.
- Proper clearance has been provided between the RF and digital sections of the design. See Layout and manufacturing.
- Proper isolation has been provided between antennas (RF co-location, diversity, or multi-antenna design).
- Bypass capacitors have been placed close to the module. See Component placement.
- Low impedance power path has been provided to the module. See Component placement.
- Controlled impedance traces have been properly implemented in the layout (both RF and digital) and the recommendations provided by the PCB manufacturer have been followed. See RF transmission line design and Component placement.
- 50 Ω RF traces and connectors follow the rules described in Antenna interfaces.
- Antenna integration has been reviewed by the antenna manufacturer.
- Proper grounding has been provided to the module for the low impedance return path and heat sink. See Layout and manufacturing.
- Reference plane skipping has been minimized for high frequency busses. See Layout and manufacturing.
- All traces and planes are routed inside the area defined by the main ground plane. See Layout and manufacturing
- u-blox has reviewed and approved the PCB 9 .

9 This is applicable only for end-products based on u-blox reference designs

Software

The instructions in this chapter describe the basic available software options for JODY-W5 series modules, which are based on the NXP AW611 chipset. Including several examples, it also describes how the reference driver packages are compiled and deployed in the target system.
☞ The proprietary driver developed by NXP and distributed by u-blox is only made available to customers that have signed a limited use license agreement (LULA-M) [3] with u-blox. The driver package and additional documentation can also be obtained directly from NXP.

4.1 Available Software packages

4.1.1 Open-source Linux/Android drivers

The drivers and firmware required to operate JODY-W5 series modules are developed by NXP. The software releases from NXP contain Wi-Fi and Bluetooth release notes and a list of supported software features. The driver source code is provided free of charge as open-source software under NXP licensing terms and conditions. As open-source resource, the drivers can be integrated or ported to other non-NXP based host platforms. Yocto recipes for the driver and firmware, that can be used to develop custom Linux-based systems, are part of the NXP i.MX Linux BSP.
The latest version of the driver source code and Wi-Fi/Bluetooth firmware is available from the following open-source repositories:

- Wi-Fi driver: https://github.com/nxp-imx/mwifiex
- Firmware: https://github.com/NXP/imx-firmware
  - o SDIO firmware
  - o SDIO-UART fimware
- i.MX meta-layer: https://github.com/nxp-imx/meta-imx
  - o ./meta-bsp/recipes-connectivity/nxp-wlan-sdk
  - o ./meta-bsp/recipes-kernel/kernel-modules/kernel-module-nxp89xx.bb
  - o ./meta-bsp/recipes-kernel/linux-firmware/linux-firmware_%.bbappend

The Wi-Fi driver uses the TCP/IP stack from the Linux kernel for data transmission and the cfg80211 subsystem in the kernel for configuration and control. Bluetooth uses the hci_uart driver from the Linux kernel and BlueZ host stack. For further information about initialization and configuration of the Wi-Fi and Bluetooth features, see also the NXP User Manual UM11490 [14].

4.2 u-blox software deliverables

The following additional software deliverables are provided by u-blox for JODY-W5 series modules:

- A Yocto/OpenEmbedded meta layer, which includes recipes for related development tools. For more information about the Yocto layer, see also Yocto meta layer.
  - ☞ For the latest JODY-W5 series software deliverables, contact your local support team.

4.2.1 Yocto meta layer

Yocto is an open-source project aimed at helping the development of custom Linux-based systems for embedded products. It provides a complete development environment with tools, documentation, and metadata like recipes, classes, and configuration. Yocto is based on the OpenEmbedded build system.
A Yocto/OpenEmbedded meta layer “meta-ublox-modules” is provided by u-blox for all host-based modules. This layer is used in Yocto projects to build the image for most host platforms that run Linux kernels. It contains the recipes used to build the Linux drivers, support tools, and any configuration files that are needed to operate the modules.

Item	Description
Build recipe	Includes all the instructions to extract, compile and install the drivers, firmware and tools in the root file system of the host system image.
Patches	Used to fix bugs in u-blox-distributed drivers seen either locally or reported by the vendor.
Calibration files	Calibration files, provided by u-blox, used while loading the driver. These files store the tuning parameters needed for RF parts present in the module, like the crystal.
Output power configuration	RF power specific files for the different bands, rates and countries are stored in configuration files provided by u-blox.
Modprobe rules	Configuration files for the modprobe utility used to store the driver load parameters.
Manufacturing package recipes	Includes different recipes for building the manufacturing tools. These recipes are used in production and RF-related tests.

Table 24: Content of the Yocto layer

☞ Calibration files are needed for the modules during the prototype stage of development. After prototyping, all

required calibrations are programmed into the OTP on the module.
☞ Further information about the Yocto layer and how to integrate it into the development environment is provided in the README files of the meta layer.

4.3 Software architecture

From a software perspective, the host-based JODY-W5 series modules contain only on-board OTP memory with calibration parameters and MAC addresses. Consequently, the modules require a hostside driver and device firmware to run. At startup and at every reset or power cycle, the host driver needs to download the firmware binary file to the module. The host driver interfaces the bus drivers with the upper-layer protocol stacks of the operating system.
Figure 13 shows the architecture of the Linux open source Wi-Fi driver (mxm_mwifiex), which is a unified driver for all supported NXP Wi-Fi chipsets. The driver allows simple migration and forward compatibility with future devices. Driver sources can be used or ported for other non-NXP host platforms. Bluetooth uses the Linux BlueZ host stack through the hci_uart interface of the module but other stacks can also be supported.

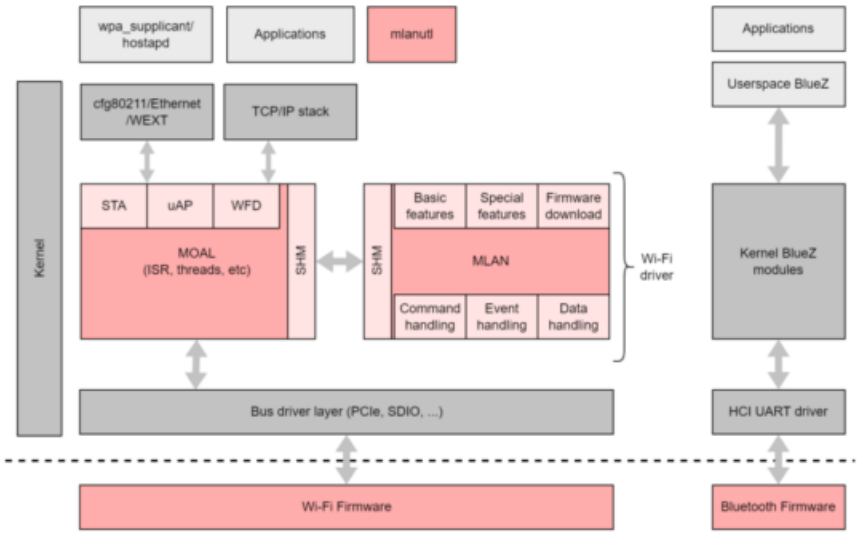


Figure 14: Basic Software view

The software includes SDIO 3.0 for Wi-Fi and UART for Bluetooth.
The host driver interfaces the lower-layer bus drivers with the upper-layer protocol stacks of the operating system. The Wi-Fi driver uses the TCP/IP stack from the Linux kernel for data transmission, and the cfg80211 subsystem in the kernel is used for configuration and control.The Bluetooth interface can be brought-up using the NXP Bluetooth UART driver (btnxpuart), or the standard Linux HCI UART driver (hci_uart). The btnxpuart driver is available in the i.MX Linux BSP L6.1.22 and later. It supports a power-save feature that automatically puts the chip into a sleep state when idle.

⚠ JODY-W5 series prototypes do not contain calibration data and MAC addresses yet. Calibration settings must be loaded from a separate configuration file while loading the driver to ensure correct operation.

4.4 Driver package structure

The NXP driver packages include different components, depending on the supported host interfaces.
The content of the packages is described in Table 25.

Component	Folder	Description
Release Notes and features	_	Release notes describing all of the supported features, changes and all known issues associated with the release.
AR-* _automotive-*	Android_hal	Hardware Abastractio Layer (HAL) for Wi-Fi and Bluetoth for Android
FwImage	FwImage	Binary firmware images. For details about the firmware images
SDIO-WIFI-*-app-src	wlan_src/mapp	Source code for the user space applications necessary to set up the different modes for Wi-Fi operation.
SDIO-WIFI-*-src	wlan_src/mlinux	Source code for the driver module moal.ko, which implements the Linux-specific part of the Wi-Fi driver. This container also includes the driver, Makefile and README files.
SDIO-WIFI-*-mlan-src	wlan_src/mlan	Source code for the driver module mlan.ko, which implements the chipset specific functionality of the Wi-Fi driver.
UART-*-src	muart_src	Source code for the HCI UART Bluetooth driver module hci_uart.ko.
UART-FW-LOADER-*-src	uartfwloader_src	Source code for the fw_loader firmware download tool used to download the Bluetooth firmware over UART in parallel mode.

Table 25: Components of the NXP driver package

4.5 Usage examples

The Wi-Fi features demonstrated in the NXP User Manual [14] are configured with the open-source wpa_supplicant/hostapd and Linux utilities. Wi-Fi features include scanning for nearby access points, connecting to an access point, configuring the device as an access point, Wi-Fi security, Wi-Fi Direct, and throughput testing using the iperf utility. The document covers the initialization and configuration of the Wi-Fi and Bluetooth interfaces. It is applicable for JODY-W5 series on i.MX 8 family NXP host processors and other NXP-based wireless modules. The Bluetooth features use the Linux BlueZ host stack and comprise scan, pair, Bluetooth or Bluetooth Low Energy (LE) device connection, A2DP profile, hands-free profile, and Bluetooth LE device GATT server operation. Guidelines for enabling driver debug logging are also provided. The manual also explains how to perform radio testing for Wi-Fi and Bluetooth using the open-source drivers.
For Android Bluetooth integration, see the Android integration Note [14].

4.6 Driver debugging

Driver debugging is provided through the kernel print function printk and the proc file system. Driver states are recorded and are retrieved through the proc file system during runtime.
The printk command output includes the following debug information files:
• /proc/mwlan/config or /proc/net/mwlan/config
• /proc/mwlan/mlanX/info or /proc/net/mwlan/mlanX/info
• /proc/mwlan/mlanX/debug or /proc/net/mwlan/mlanX/debug
☞ Note that the physical file location is dependent on the Linux kernel version.
☞ mlanX is the name of the device node created at runtime. Other file name possibilities include uapX and wfdX for the access point and Wi-Fi Direct interfaces respectively.
Debug messages are also printed to the kernel ring buffer through printk calls. These messages are accessed using the /proc/kmsg interface or by the dmesg command. Alternatively, this can also be handled by more advanced logging facilities.

4.6.1 Compile-time debug options

The extent to which the debug messages can be printed at runtime is controlled by the CONFIG_DEBUG variable

in the driver Makefile. The CONFIG_DEBUG variable can have any of the following values:

- n: debug messages are disabled and not compiled into the driver module
- 1: all kinds of debug messages can be configured except for MENTRY, MWARN and MINFO.
  By default, MMSG, MFATAL and MERROR are enabled.
- 2: all kinds of debug messages can be configured

4.6.2 Runtime debug options

Once debugging is enabled in the Makefile, debug messages can be selectively enabled or disabled atruntime. Set or clear the corresponding bits of the drvdbg parameter accordingly:

```
bit 0:  MMSG          PRINTM(MMSG,...)
bit 1:  MFATAL        PRINTM(MFATAL,...)
bit 2:  MERROR        PRINTM(MERROR,...)
bit 3:  MDATA         PRINTM(MDATA,...)
bit 4:  MCMND         PRINTM(MCMND,...)
bit 5:  MEVENT        PRINTM(MEVENT,...)
bit 6:  MINTR         PRINTM(MINTR,...)
bit 7:  MIOCTL        PRINTM(MIOCTL,...)
...
bit 16: MDAT_D        PRINTM(MDAT_D,...), DBG_HEXDUMP(MDAT_D,...)
bit 17: MCMD_D        PRINTM(MCMD_D,...), DBG_HEXDUMP(MCMD_D,...)
bit 18: MEVT_D        PRINTM(MEVT_D,...), DBG_HEXDUMP(MEVT_D,...)
bit 19: MFW_D         PRINTM(MFW_D,...),  DBG_HEXDUMP(MFW_D,...)
bit 20: MIF_D         PRINTM(MIF_D,...),  DBG_HEXDUMP(MIF_D,...)
...
bit 28: MENTRY        PRINTM(MENTRY,...), ENTER(), LEAVE()
bit 29: MWARN         PRINTM(MWARN,...)
bit 30: MINFO         PRINTM(MINFO,...)
```

To change the value of the drvdbg parameter, enter it as a module parameter when the driver is loaded, or write to the debug file in the proc file system, or set it using either the iwpriv or mlanutl tools.

```
iwpriv mlan0 drvdbg                          # Get the current driver debug mask
iwpriv mlan0 drvdbg 0                        # Disable all debug messages
echo "drvdbg=0x7" > /proc/mwlan/mlan0/debug  # enable MMSG, MFATAL and MERROR
mlanutl mlan0 drvdbg -1                      # Enable all debug messages
```

Handling and soldering

⚠ JODY-W5 series modules are Electrostatic Sensitive Devices that demand the observance of special handling precautions against static damage. Failure to observe these precautions can result in severe damage to the product.

5.1 ESD handling precautions

As the risk of electrostatic discharge in the RF transceivers and patch antennas of the module is of particular concern, standard ESD safety practices are prerequisite. See also Figure 12.
Consider also:

- When connecting test equipment or any other electronics to the module (as a standalone or PCBmounted device), the first point of contact must always be to local GND.
- Before mounting an antenna patch, connect the device to ground.
- When handling the RF pin, do not touch any charged capacitors. Be especially careful when handling materials like patch antennas (~10 pF), coaxial cables (~50-80 pF/m), soldering irons, or any other materials that can develop charges.

- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk of the exposed antenna being touched in an unprotected ESD work area, be sure to implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the RF pin on the receiver, be sure to use an ESD-safe soldering iron (tip).

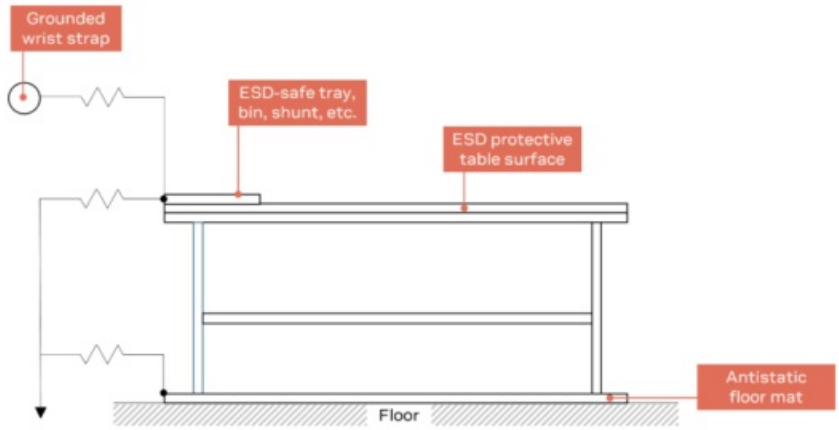


Figure 12: Standard workstation setup for safe handling of ESD-sensitive devices

5.2 Packaging, shipping, storage, and moisture preconditioning

For information pertaining to reels, tapes, or trays, moisture sensitivity levels (MSL), storage, shipment, and drying preconditioning, see the JODY-W5 series data sheet [1] and Packaging information reference guide [2].

5.3 Reflow soldering process

☞ JODY-W5 is approved for two-time reflow processes.

JODY-W5 modules are surface mounted devices supplied on a multi-layer FR4-type PCB with goldplated connection pads. The modules are produced in a lead-free process using lead-free soldering paste. The thickness of solder resist between the host PCB top side and the bottom side of the JODYW5 module must be considered for the soldering process. JODY-W5 modules are compatible with industrial reflow profile for RoHS solders, and “no-clean” soldering paste is strongly recommended. The reflow profile used is dependent on the thermal mass of the entire populated PCB, the heat transfer efficiency of the oven, and the type of solder paste that is used. The optimal soldering profile must be trimmed for the specific process and PCB layout.

⚠ The target values shown in Table 26 and Figure 13 are given as general guidelines for a Pb-free process only. For further information, see also the JEDEC J-STD-020E [7] standard.

Process parameter		Unit	Target
Pre-heat	Ramp up rate to T_{SMIN}	K/s	3
	TSMIN	°C	150
	TSMAX	°C	200
	t_S (from 25°C)	s	150
	t_S (Pre-heat)	s	110
Peak	T_L	°C	217
	t_L (time above T_L)	s	90
	T_P	°C	245-250
	t_P (time above T_P -5°C)	s	30
Cooling	Ramp-down from T_L (max)	K/s	6
General	Tto peak	s	300
	Allowed reflow soldering cycles	–	2

Table 26: Recommended reflow profile

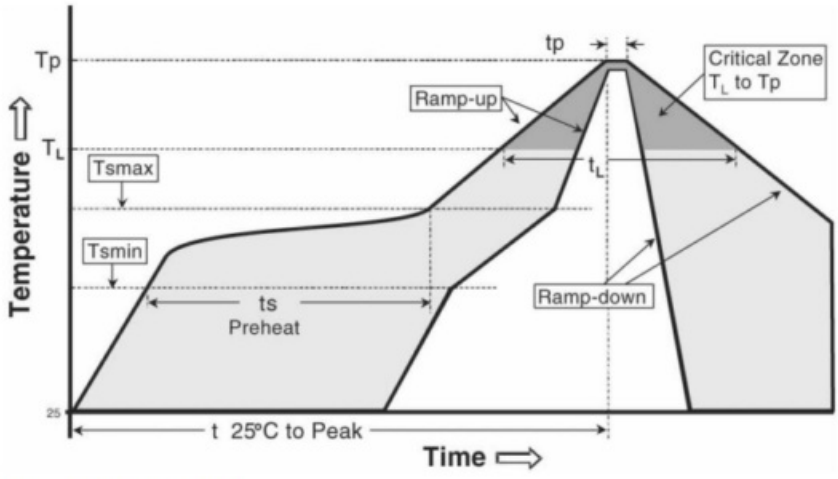


Figure 13: Reflow profile

☞ The lower value of TP and slower ramp down rate is preferred.

5.3.1 Cleaning

Cleaning the modules isn't recommended. Residues underneath the modules can't be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pins. Water will also damage the sticker and the ink-jet

printed text.

- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the housing, areas that are not accessible for post-wash inspections. The solvent will also damage the label and the ink-jet printed text.
- Ultrasonic cleaning can permanently damage the module and the crystal oscillators in particular. For best results use a “no clean” soldering paste and circumvent the need for a cleaning stage after the soldering process.

5.3.2 Other notes

- Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices might require wave soldering of the THT components. Only a single wave-soldering process is allowed for boards populated with the modules. Miniature Wave Selective Solder processes are preferred over traditional wave soldering processes.
- Hand-soldering isn’t recommended.
- Rework isn’t recommended.
- Conformal coating can affect the performance of the module, which means that it is important to prevent the liquid from flowing into the module. The RF shields do not provide protection for the module from coating liquids with low viscosity; therefore, care is required while applying the coating. Conformal coating of the module will void the warranty.
- Grounding metal covers: Attempts to improve grounding by soldering ground cables, wick, or other forms of metal strips directly onto the EMI covers is done so at the customer’s own risk and will void the module warranty. The numerous ground pins on the module are adequate to provide optimal immunity to interferences.
- The modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding, etc.) can damage the module. The use of ultrasonic processes together with the module will void the warranty.

Regulatory compliance

6.1 General requirements

JODY-W5 series modules are designed to comply with the regulatory demands of Federal Communications Commission (FCC), Innovation, Science and Economic Development Canada (ISED)10 and the CE mark. This chapter contains instructions on the rocess needed for an integrator when including the JODY-W5 module into an end-product.

- Any deviation from the process described may cause the JODY-W5 series module not to comply with the regulatory authorizations of the module and thus void the user’s authority to operate the equipment.
- Any changes to hardware, hosts or co-location configuration might require new radiated emission and SAR evaluation and/or testing.
- The regulatory compliance of JODY-W5 does not exempt the end-product from being evaluated against applicable regulatory demands; for example, FCC Part 15B criteria for unintentional radiators [9].
- The end-product manufacturer must follow all the engineering and operating guidelines, as specified by the grantee (u-blox).
- JODY-W5 is for OEM integrators only.
- Only authorized antenna(s) may be used. Refer to JODY-W5 data sheet [1] for the list of authorized antennas.

In the end-product, the JODY-W5 module must be installed in such a way that only authorized antennas can be used.

- The end-product must use the specified antenna trace reference design, as described in the JODY-W5 antenna reference design application note [11].
- Any notification to the end user about how to install or remove the integrated radio module is NOT allowed.

⚠ If these conditions can't be met or any of the operating instructions are violated, the u-blox regulatory authorization is considered invalid. In these circumstances, the integrator must reevaluate the end-product including the JODY-W5 series module and then obtain their own regulatory authorization. In certain circumstances, u-blox may be able to add a customer design to the u-blox grant. See also Antenna requirements.

6.1 European Union regulatory compliance (pending)

JODY-W5 series modules comply with the essential requirements and other relevant provisions of Radio Equipment Directive (RED) 2014/53/EU.

For information about the regulatory compliance of JODY-W5 series modules against requirements and provisions in the European Union, see the JODY-W5 Declaration of Conformity (pending).

6.1.1 CE End-product regulatory compliance

6.1.1.1 Safety standard

In order to fulfill the safety standard EN 60950-1 [8], the JODY-W5 module must be supplied with a Class-2 Limited Power Source.

6.1.2 CE Equipment classes

In accordance with Article 1 of Commission Decision 2000/299/EC11 , JODY-W5 is defined as either Class-1 or Class-2 radio equipment, the end-product integrating JODY-W5 inherits the equipment class of the module.

☞ For guidance on end product marking in according with RED, see **http://ec.europa.eu/**

⚠ The EIRP of the JODY-W5 module must not exceed the limits of the regulatory domain that the module operates in. Depending on the host platform implementation and antenna gain, integrators have to limit the maximum output power of the module through the host software. For information about the corresponding maximum transmit power levels of Pre-approved antennas.

6.2 Great Britain regulatory compliance

For information about the regulatory compliance of JODY-W5 series modules against requirements and provisions in Great Britain, see also the JODY-W5 UKCA Declaration of Conformity (pending).

6.2.1 UK Conformity Assessed (UKCA)

☞ The United Kingdom is made up of the Great Britain (including England, Scotland, and Wales) and the Northern Ireland. Northern Ireland continues to accept the CE marking. The following notice is applicable to Great Britain only.

JODY-W5 series modules have been evaluated against the essential requirements of the Radio Equipment Regulations 2017 (SI 2017 No. 1206, as amended by SI 2019 No. 696).

For guidance on end product marking in accordance with UKCA, see **https://www.gov.uk/guidance/using-the-ukca-marking**.

6.3 United states/Canada End-product regulatory compliance

u-blox represents that the modular transmitter fulfills the FCC/ISED regulations when operating in authorized modes on any host product given that the integrator follows the instructions as described in this document. Accordingly, the host product manufacturer acknowledges that all host products referring to the FCC ID or ISED certification number of the modular transmitter and placed on the market by the host product manufacturer need to fulfil all of the requirements mentioned below. Noncompliance with these requirements may result in revocation of the FCC approval and removal of the host products from the market. These requirements correspond to questions featured in the FCC guidance for software security requirements for U-NII devices, FCC OET KDB 594280 D02 (pending).

⚠ The modular transmitter approval of JODY-W5, or any other radio module, does not exempt the end product from being evaluated against applicable regulatory demands.

The evaluation of the end product shall be performed with the JODY-W5 module installed and operating in a way that reflects the intended end product use case. The upper frequency measurement range of the end product evaluation is the 10th harmonic of 5.8 GHz as described in KDB 996369 D04.

11 2000/299/EC: Commission Decision of 6 April 2000 establishing the initial classification of radio equipment and telecommunications terminal equipment and associated identifiers.

The following requirements apply to all products that integrate a radio module:

- Subpart B – UNINTENTIONAL RADIATORS
  To verify that the composite device of host and module comply with the requirements of FCC part 15B, the integrator shall perform sufficient measurements using ANSI 63.4-2014.
- Subpart C – INTENTIONAL RADIATORS
  It is required that the integrator carries out sufficient verification measurements using ANSI 63.10-2013 to validate that the fundamental and out of band emissions of the transmitter part of the composite device complies with the requirements of FCC part 15C.

When the items listed above are fulfilled, the end product manufacturer can use the authorization procedures as mentioned in Table 1 of 47 CFR Part 15.101, before marketing the end product. This means the customer has to either market the end product under a Suppliers Declaration of Conformity (SdoC) or to certify the product using an accredited test lab.
The description is a subset of the information found in applicable publications of FCC Office of Engineering and Technology (OET) Knowledge Database (KDB). We recommend the integrator to read the complete document of the referenced OET KDB's.

- KDB 178919 D01 Permissive Change Policy
- KDB 447498 D01 General RF Exposure Guidance
- KDB 594280 D01 Configuration Control
- KDB 594280 D02 U-NII Device Security
- KDB 784748 D01 Labelling Part 15 18 Guidelines
- KDB 996369 D01 Module certification Guide
- KDB 996369 D02 Module Q&A
- KDB 996369 D04 Module Integration Guide

6.3.1 United States compliance statement (FCC)

Table 27 shows the FCC IDs allocated to JODY-W5 series modules.

Model	FCC ID
JODY-W562-00A	XPYJODYW562

Table 27: FCC IDs for different variants of JODY-W5 series modules

JODY-W5 series modules have modular approval and comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

⚠ Any changes or modifications NOT explicitly APPROVED by u-blox could cause the JODY-W5 series module to cease to comply with FCC rules part 15 thus void the user's authority to operate the equipment.
The internal / external antenna(s) used for this module must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.
For FCC end poduct labeling requirements, see End product labeling requirements.

6.3.2 Canada compliance statement (ISED)

JODY-W5 series modules are certified for use in accordance with the Canada Innovation, Science and Economic Development Canada (ISED) Radio Standards Specification (RSS) RSS-247 Issue 2 and RSS-Gen. Table 28 shows the ISED certification IDs allocated to JODY-W5 series modules.

Model	ISED certification ID
JODY-W562-00A	8595A-JODYW562

Table 28: ISED IDs for different variants of JODY-W5 series modules

JODY-W5 series complies with ISED (Innovation, Science and Economic Development Canada)12 license-exempt RSSs. Operation is subject to the following two conditions:

1. This device may not cause interference, and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

☞ Any notification to the end user of installation or removal instructions about the integrated radio module is NOT allowed. Unauthorized modification could void authority to use this equipment.

This equipment complies with ISED RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body.

This radio transmitter IC: 8595A-JODYW562 / IC: 8595A-JODYW562 has been approved by ISED to operate with the antenna types listed in Approved antennas with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

☞ Operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

☞ Operation in the 5600-5650 MHz band is not allowed in Canada. High-power radars are allocated as primary users (i.e., priority users) of the bands 5250-5350 MHz and 5650-5850 MHz and that these radars could cause interference and/or damage to LE-LAN devices.

The internal / external antenna(s) used for this module must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

For ISED end poduct labeling requirements, see End product labeling requirements.

☞ The approval type for all JODY-W5 series variants is a single modular approval. Due to ISED Modular Approval Requirements (Source: RSP-100 Issue 10), any application which includes the module must be approved by the module manufacturer (u-blox). The application manufacturer must provide design data for the review procedure.

6.3.3 Referring to the u-blox FCC/ISED certification ID

If the General requirements, United states/Canada End-product regulatory compliance and all Antenna requirements are met, the u-blox modular FCC/ISED regulatory authorization is valid and the end-product may refer to the u-blox FCC ID and ISED certification number. U-blox may be able to support updates to the u-blox regulatory authorization by adding new antennas to the u-blox authorization for example. See also Antenna requirements.

⚠ To use the u-blox FCC / ISED grant and refer to the u-blox FCC ID / ISED certification ID, the integrator must confirm with u-blox that all requirements associated with the Configuration control and software security of end-products are fulfilled.

6.3.4 Obtaining own FCC/ISED certification ID

Integrators who do not want to refer to the u-blox FCC/ISED certification ID, or who do not fulfil all requirements to do so may instead obtain their own certification. With their own certification, the integrator has full control of the grant to make changes.

Integrators who want to base their own certification on the u-blox certification can do so via a process called “Change in ID” (FCC) / “Multiple listing” (ISED). With this, the integrator becomes the grantee of a copy of the u-blox FCC/ISED certification. U-blox will support with an approval letter that shall be filed as a Cover Letter exhibit with the application.

☞ For modules where the FCC ID / ISED certification ID is printed on the label, the integrator must replace the module label with a new label containing the new FCC/ISED ID. For a description of the labeling requirements, see also the JODY-W5 series data sheet [1].

⚠ It is the responsibility of the integrator to comply with any upcoming regulatory requirements.

6.3.5 Antenna requirements

In addition to the general requirement to use only authorized antennas, the u-blox grant also requires a separation distance of at least 20 cm from the antenna(s) to all persons. The antenna(s) must not be co-located with any other antenna or transmitter (simultaneous transmission) as well. If this can't be met, a Permissive Change as described below must be made to the grant.

☞ To support verification activities that may be required by certification laboratories, customers applying for Class-II Permissive changes must implement the setup described in Software.

6.3.5.1 Separation distance

If the required separation distance of 20 cm can't be fulfilled, a SAR evaluation must be performed.

This consists of additional calculations and/or measurements. The result must be added to the grant file as a Class II Permissive Change.

6.3.5.2 Co-location (simultaneous transmission)

If the module is to be co-located with another transmitter, additional measurements for simultaneous transmission are required. The results must be added to the grant file as a Class II Permissive Change.

6.3.5.3 Adding a new antenna for authorization

If the authorized antennas and/or antenna trace design can't be used, the new antenna and/or antenna trace designs must be added to the grant file. This is done by a Class I Permissive Change or a Class II Permissive Change, depending on the specific antenna and antenna trace design.

- Antennas of the same type and with less or same gain as those included in the list of Pre-approved antennas can be added under a Class I Permissive Change.
- Antenna trace designs deviating from the u-blox reference design and new antenna types are added under a Class II Permissive Change.
- For 5 GHz modules, the combined minimum gain of antenna trace and antenna must be greater than 0 dBi to comply with DFS testing requirements.

⚠ Integrators intending to refer to the u-blox FCC ID / ISED certification ID must contact their local support team to discuss the Permissive Change Process. Class II Permissive Changes are subject to NRE costs.

6.3.6 Configuration control and software security of end-products

☞ "Modular transmitter" hereafter refers to the JODY-W5xx FCC ID (TBD).

As the end-product must comply with the requirements addressed by the OET KDB 594280 [15], the host product integrating the JODY-W5 must comply with the following requirements:

- Upon request from u-blox, the host product manufacturer can provide all of the necessary information and documentation to demonstrate how the requirements listed below are met.
- The host product manufacturer must not modify the modular transmitter hardware.
- The configuration of the modular transmitter when installed into the host product must be within the authorization of the modular transmitter at all times and can't be changed to include unauthorized modes of operation through accessible interfaces of the host product. The Wi-Fi Tx output power limits must be followed. In particular, the modular transmitter installed in the host product will not have the capacity to operate in the operating channels/frequencies referred to in the section(s) below, namely one or several of the following channels: 12 (2467 MHz), 13 (2472 MHz), 120 (5600 MHz), 124 (5620 MHz), and 128 (5640 MHz). The channels 12 (2467 MHz), 13 (2472 MHz), 120 (5600 MHz), 124 (5620 MHz), and 128 (5640 MHz) are allowed to be used only for modules that are certified for the usage ("modular transmitter"). Customers must verify that the module in use is certified as supporting DFS client/master functionality.
- The host product uses only authorized firmware images provided by u-blox and/or by the manufacturer of the RF chipset used inside the modular transmitter.
- The configuration of the modular transmitter must always follow the requirements specified in Operating frequencies and can't be changed to include unauthorized modes of operation through accessible interfaces of

the host product.

- When installed into the host product, the modular transmitter must have a regional setting that is compliant with authorized US modes. The host product must also be protected to prevent unauthorized modes of operation of the modular transmitter, including the country code and other modifications, by third parties.
- The host product into which the modular transmitter is installed does not provide any interface for the installer to enter configuration parameters into the end product that exceeds those authorized.
- The host product into which the modular transmitter is installed does not provide any interface that allows third parties to upload any unauthorized firmware images into the modular transmitter. The host product also prevents third parties from making nauthorized changes to all or parts of the modular transmitter device driver software and configuration.

☞ OET KDB 594280 D01 [15] lists the topics that must be addressed to ensure that the endproduct specific host meets the Configuration Control requirements.
☞ OET KDB 594280 D02 [16] lists the topics that must be addressed to ensure that the endproduct specific host meets the Software Security Requirements for U-NII Devices.

6.3.7 Operating frequencies

JODY-W5 802.11b/g/n/ax operation outside the 2412–2462 MHz band is prohibited in the US and Canada and 802.11a/n/ac/ax operation in the 5600–5650 MHz band is prohibited in Canada.
Configuration of the module to operate on channels 12–13 and 120–128 must be prevented accordingly.
The channels allowed while operating under the definition of a master or client device 13 are described in Table 29.

Channel number	Channel center frequency [MHz]	Main node device	Client device	Remarks
1 – 11	2412 – 2462	Yes	Yes	
12 – 13	2467 – 2472	No	No	
36 – 48	5180 – 5240	Yes	Yes	Canada (ISED): Devices are restricted to indoor operation only and the end product must be labelled accordingly.
52 – 64	5260 – 5320	No14	Yes	
100 – 116	5500 – 5580	No14	Yes	
120 – 128	5600 – 5640	No	No	USA (FCC): Client device operation allowed under KDB 905462
132 – 144	5660 – 5720	No14	Yes	
149 – 165	5745 – 5825	Yes	Yes	
169 – 177	5835 – 5885	No15	No16	Only USA (FCC) indoor operation

Table 29: Allowed channel usage under FCC/ISED regulation

☞ 15.407 (j) Operator Filing Requirement:
Before deploying an aggregate total of more than one thousand outdoor access points within the 5.15–5.25 GHz band, parties must submit a letter to the Commission acknowledging that, should harmful interference to licensed services in this band occur, they will be required to take corrective action. Corrective actions may include reducing

power, turning off devices, changing frequency bands, and/or further reducing power radiated in the vertical direction. This material shall be submitted to Laboratory Division, Office of Engineering and Technology, Federal Communications Commission, 7435 Oakland Mills Road, Columbia, MD 21046. Attn: U-NII

13 47 CFR §15.202
14 DFS certification is pending.
15 Certification of U-NII-4 band is pending
16 Certification of U-NII-4 band is pending
Coordination, or via Web site at **https://www.fcc.gov/labhelp** with the subject line: “U-NII-1 Filing”.

6.3.8 End product labeling requirements

For an end-product using the JODY-W5, there must be a label containing, at least, the following information:
This device contains
FCC ID: (XYZ)(UPN)
IC: (CN)-(UPN)
(XYZ) represents the FCC “Grantee Code”, this code may consist of Arabic numerals, capital letters, or other characters, the format for this code will be specified by the Commission’s Office of Engineering and Technology17 . (CN) is the Company Number registered at ISED. (UPN) is the Unique Product Number decided by the grant owner.
The label must be affixed on an exterior surface of the end product such that it will be visible upon inspection in compliance with the modular labeling requirements of OET KDB 784748. The host user manual must also contain clear instructions on how end users can find and/or access the FCC ID of the end product.
The label on the JODY-W5 module containing the original FCC ID acquired by u-blox can be replaced with a new label stating the end-product’s FCC/ISED ID in compliance with the modular labeling requirements of OET KDB 784748.

FCC end product labeling

The outside of final products containing the JODY-W5 module must display in a user accessible area a label referring to the enclosed module. This exterior label can use wording such as the following:
“Contains Transmitter Module FCC ID: XPYJODYW5xy” or “Contains FCC ID: XPYJODYW5xy”.
In accordance with 47 CFR § 15.19, the end product shall bear the following statement in a conspicuous location on the device:
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
This device may not cause harmful interference, and
This device must accept any interference received, including interference that may cause undesired operation.

ISED end product labeling

The ISED certification label of a module shall be clearly visible at all times when installed in the host device; otherwise, the host device must be labeled to display the ISED certification number for the module, preceded by the words “Contains transmitter module”, or the word “Contains”, or similar wording expressing the same meaning, as follows: “Contains transmitter module IC: 8595A- JODYW5xy”.
The end product shall bear the following statement in both English and French in a conspicuous location on the device:
Operation is subject to the following two conditions:
This device may not cause interference, and
This device must accept any interference, including interference that may cause undesired operation of the device.
Labels of end products capable to operate within the band 5150–5250 MHz shall also include:
For indoor use only
Pour usage intérieur seulement
When the device is so small or for such use that it is not practicable to place the statements above on it, the information shall be placed in a prominent location in the instruction manual or pamphlet supplied to the user or, alternatively, shall be placed on the container in which the device is marketed.
However, the FCC/ISED ID label must be displayed on the device as described above.
In case, where the final product will be installed in locations where the end-consumer is unable to see the FCC/ISED ID and/or this statement, the FCC/ISED ID and the statement shall also be included in the end-product manual.

6.4 Pre-approved antennas

Refer to the JODY-W5 antenna reference design application note [19] for the specifications that must be fulfilled in the end product that uses radio type approval of the JODY-W5 module. The JODY-W5 antenna reference design application note provides PCB layout details and electrical specifications. For Bluetooth and Wi-Fi operation in the 2.4 GHz band and Wi-Fi operation in the 5 GHz band, JODY-W5 has been tested and approved for use with the antennas listed in Table 30.

Manufacturer	Part number	Antenna type	Peak gain [dBi] / band		Validated regulatory domain
			2.4 GHz	5 GHz	
Linx Technologies	ANT-DB1-RAF-RPS	Dual-band dipole antenna	4.1	5.1	US/Canada (FCC/ISED)
Molex	1461530050	PCB patch	3.2	4.25	US/Canada (FCC/ISED)
–	–	–	0	0	EU/Great Britain (RED/UKCA)

Table 30: List of approved antennas

☞ No antennas have been used for RED/UKCA certifications. All radiated measurements were performed with 50 Ω terminations. The power limits in Wi-Fi transmit output power limits are valid for the antenna gains stated in .
⚠ For compliance with FCC §15.407(a), the EIRP is not allowed to exceed 125 mW (21 dBm) at any elevation angle above 30° (measured from the horizon) when operated as an outdoor access point in U-NII-1 band, 5.150-5.250 GHz.

Product testing

7.1 u-blox in-line production testing

As part of our focus on high quality products, u-blox maintain stringent quality controls throughout the production process. This means that all units in our manufacturing facilities are fully tested and that any identified defects are carefully analyzed to improve future production quality.
The Automatic test equipment (ATE) deployed in u-blox production lines logs all production and measurement data – from which a detailed test report for each unit can be generated. Figure 14 shows the ATE typically used during u-blox production.
u-blox in-line production testing includes:

- Digital self-tests (firmware download, MAC address programming)
- Measurement of voltages and currents
- Functional tests (host interface communication)
- Digital I/O tests
- Measurement and calibration of RF characteristics in all supported bands, including RSSI calibration, frequency tuning of reference clock, calibration of transmitter power levels, etc.
- Verification of Wi-Fi and Bluetooth RF characteristics after calibration, like modulation accuracy, power levels, and spectrum, are checked to ensure that all characteristics are within tolerance when the calibration parameters are applied.

Figure 14: Automatic test equipment for module test

7.2 OEM manufacturer production test

As all u-blox products undergo thorough in-series production testing prior to delivery, OEM manufacturers do not need to repeat any firmware tests or measurements that might otherwise be necessary to confirm RF performance. Testing over analog and digital interfaces is also unnecessary during an OEM production test. OEM manufacturer testing should ideally focus on:

- Module assembly on the device; it should be verified that:
  - o Soldering and handling process did not damage the module components
  - o All module pins are well soldered on the application board
  - o There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - o Communication with host controller can be established
  - o The interfaces between module and device are working
  - o Overall RF performance test of the device including antenna

In addition to this testing, OEMs can also perform other dedicated tests to check the device. For example, the measurement of module current consumption in a specified operating state can identify a short circuit if the test result deviates that from that taken against a “Golden Device”.
The standard operational module firmware and test software on the host can be used to perform functional tests (communication with the host controller, check interfaces) and perform basic RF performance testing. Special manufacturing firmware can also be used to perform more advanced RF performance tests.

Appendix

A Wi-Fi transmit output power limits

A.1 FCC/ISED regulatory domain

Table 31 and Table 32 list the maximum allowable conducted output power limits for operation in the FCC/ISED regulatory domains. The output power limits are applicable with the pre-approved antennas listed in section 6.4.

A.1.1 Wi-Fi output power for 2.4 GHz band

	802.11b	802.11g	802.11n 20 MHz	802.11n 40 MHz	802.11ax 20 MHz	802.11ax 40 MHz
1	19	15	15	n/a	14	n/a
2	19	16	16	n/a	14	n/a
3	19	17	16	13	15	14
4	19	17	16	13	15	13
5	19	18	17	13	16	13
6	19	18	17	13	17	13
7	19	18	17	13	17	13
8	19	17	17	12	15	13
9	19	16	16	11	15	12
10	19	15	15	n/a	13	n/a
11	19	14	14	n/a	12	n/a

Table 31: FCC / ISED Wi-Fi power table for operation in the 2.4 GHz band

A.1.2 Wi-Fi output power for 5 GHz band

	802.11a	802.11n 20 MHz	802.11n 40 MHz	802.11ac 20 MHz	802.11ac 40 MHz	802.11ac 80 MHz	802.11ax 20 MHz	802.11ax 40 MHz	802.11ax 80 MHz
36	15	15	14	15	14	10	14	13	10
40	15	15	14	15	14	10	14	13	10
44	15	15	15	15	15	10	14	14	10
48	15	15	15	15	15	10	14	14	10
52	17	17	17	17	17	10	17	17	10
56	17	17	17	17	17	10	17	17	10
60	17	17	14	17	14	10	17	13	10
64	17	15	14	15	14	10	15	13	10
100	14	14	12	14	12	10	14	12	10
104	17	16	12	16	12	10	15	12	10
108	18	18	17	18	17	10	18	16	10
112	18	18	17	18	17	10	18	16	10
116	18	18	n/a	18	n/a	n/a	18	n/a	n/a
132	18	18	13	18	13	17	18	12	17
136	18	18	13	17	13	17	16	12	17
140	15	15	18	15	18	17	14	18	17
144	18	18	18	18	18	17	18	18	17
149	18	18	18	18	18	14	18	18	14
153	18	18	18	18	18	14	18	18	14
157	18	18	18	18	18	14	18	18	14
161	18	18	18	18	18	14	18	18	14
165	18	18	n/a	18	n/a	n/a	18	n/a	n/a

Table 32: FCC / ISED Wi-Fi power table for operation in the 5 GHz band

A.2 RED regulatory domain

Table 33 and Table 34 list the maximum allowable conducted output power limits for operation in the RED/UKCA regulatory domains. The output power limits are applicable with the pre-approved antennas listed in section 6.4.

A.2.1 Wi-Fi output power for 2.4 GHz band

	802.11b	802.11g	802.11n 20 MHz	802.11n 40 MHz	802.11ax 20 MHz	802.11ax 40 MHz
1 – 13	17	18	18	17	18	17

Table 33: RED Wi-Fi power table for operation in the 2.4 GHz band

A.2.2 Wi-Fi output power for 5 GHz band

Channels	802.11a	802.11n 20 MHz	802.11n 40 MHz	802.11ac 20 MHz	802.11ac 40 MHz	802.11ac 80 MHz	802.11ax 20 MHz	802.11ax 40 MHz	802.11ax 80 MHz
36 – 48	16	16	16	16	16	16	16	16	16
52 – 64	16	16	16	16	16	16	16	16	16
100 – 140	16	16	16	16	16	16	16	16	16
149 – 165	16	16	16	16	16	16	16	16	16

Table 34: RED Wi-Fi power table for operation in the 5 GHz band

B Glossary

Abbreviation	Definition
AEC	Automotive Electronics Council
AP	Access Point
API	Application Programming Interface
ATE	Automatic Test Equipment
BT	Bluetooth
CDM	Charged Device Model
CE	European Conformity
CTS	Clear to Send
DC	Direct Current
DDR	Double Data Rate

DFS	Dynamic Frequency Selection
DHCP	Dynamic Host Configuration Interface
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIRP	Equivalent Isotropic Radiated Power
EMI	Electromagnetic Interference
ESD	Electro Static Discharge
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FCC	Federal Communications Commission
GND	Ground
GPIO	General Purpose Input/Output
HBM	Human Body Model
HS	High-Speed
HCI	Host Controller Interface
ISED	Innovation, Science and Economic Development Canada
I2C	Inter-Integrated Circuit
KDB	Knowledge Database
LAN	Local Area Network
LDO	Low Drop Out
LED	Light-Emitting Diode
LPO	Low Power Oscillator

LTE	Long Term Evolution
MAC	Medium Access Control
MMC	Multi Media Card
MWS	Mobile Wireless Standards
NRE	Non-recurring engineering
NSMD	Non Solder Mask Defined
OEM	Original equipment manufacturer
OET	Office of Engineering and Technology
OS	Operating System
PCB	Printed Circuit Board

Abbreviation	**Definition**
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCM	Pulse-code modulation
PHY	Physical layer (of the OSI model)
PMU	Power Management Unit
RF	Radio Frequency
RSDB	Real Simultaneous Dual Band
RST	Request to Send
SDIO	Secure Digital Input Output
SMD	Solder Mask Defined

SMPS	Switching Mode Power Supply
SMT	Surface-Mount Technology
SSID	Service Set Identifier
STA	Station
TBD	To be Decided
THT	Through-Hole Technology
UART	Universal Asynchronous Receiver-Transmitter
VCC	IC power-supply pin
VIO	Input offset voltage
VSDB	Virtual Simultaneous Dual Band
VSWR	Voltage Standing Wave Ratio
WFD	Wi-Fi Direct
WLAN	Wireless local area network
WPA	Wi-Fi Protected Access

Table 35: Explanation of the abbreviations and terms used

Related documentation

[1] JODY-W5 series data sheet, UBX-23002865
[2] Packaging information reference, UBX-14001652
[3] u-blox Limited Use License Agreement, LULA-M
[4] IEC EN 61000-4-2 – Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test
[5] ETSI EN 301 489-1 – Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements
[6] IEC61340-5-1 – Protection of electronic devices from electrostatic phenomena – General requirements
[7] JEDEC J-STD-020E – Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices
[8] ETSI EN 60950-1:2006 – Information technology equipment – Safety – Part 1: General requirements
[9] FCC Regulatory Information, Title 47 – Telecommunication
[10] JESD51 – Overview of methodology for thermal testing of single semiconductor devices
[11] Antenna Integration application note, UBX-18070466
[12] Embedded Linux for i.MX Applications Processors

[13] MCUXpresso Software Development Kit (SDK)
[14] NXP UM11490, Feature Configuration Guide for NXP-based Wireless Modules on i.MX 8M Quad EVK
[15] FCC guidance 594280 D01 Configuration Control v02 r01,
[16] FCC guidance 594280 D02 U-NII Device Security v01r03
[17] JODY-W5 product summary, UBX-23007124
[18] Android integration for NXP-based modules, UBX-19035432
[19] JODY-W5 Antenna Reference Design_AppNote, UBXDOC-465451970-3645.
☞ For product change notifications and regular updates of u-blox documentation, register on our website, **www.u-blox.com**.

Revision history

Revision	Date	Name	Comments
R01	22-Jan-2024	lber, tpat	Initial release
R02	19-Feb-2024	frca	Changed disclosure restriction class only
R03	11-Jun-2024	Lber, fkru, fcam	Revised country certification plan for radio type approvals in Overview. Updated mechanical drawing. Added approved antenna list.
R04		Lber, fkru, fcam	Corrected table for Wake-up signals descriptions Wake-up signals Added Wi-Fi transmit power limits in Wi-Fi transmit output power limits Revised status for type approvals Regulatory compliance. SDIO information modified in SDIO 3.0 interface

JODY-W5 series – System integration manual

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Documents / Resources

	**U Blox JODY-W5 Series Host based Modules** [pdf] Instruction Manual JODYW562, XPYJODYW562, JODY-W5 Series Host based Modules, JODY-W5 Series, Host based Modules, based Modules, Modules

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- u-blox.com/docs/UBX-23002865
- u-blox.com/docs/UBX-23007124
- User Manual