

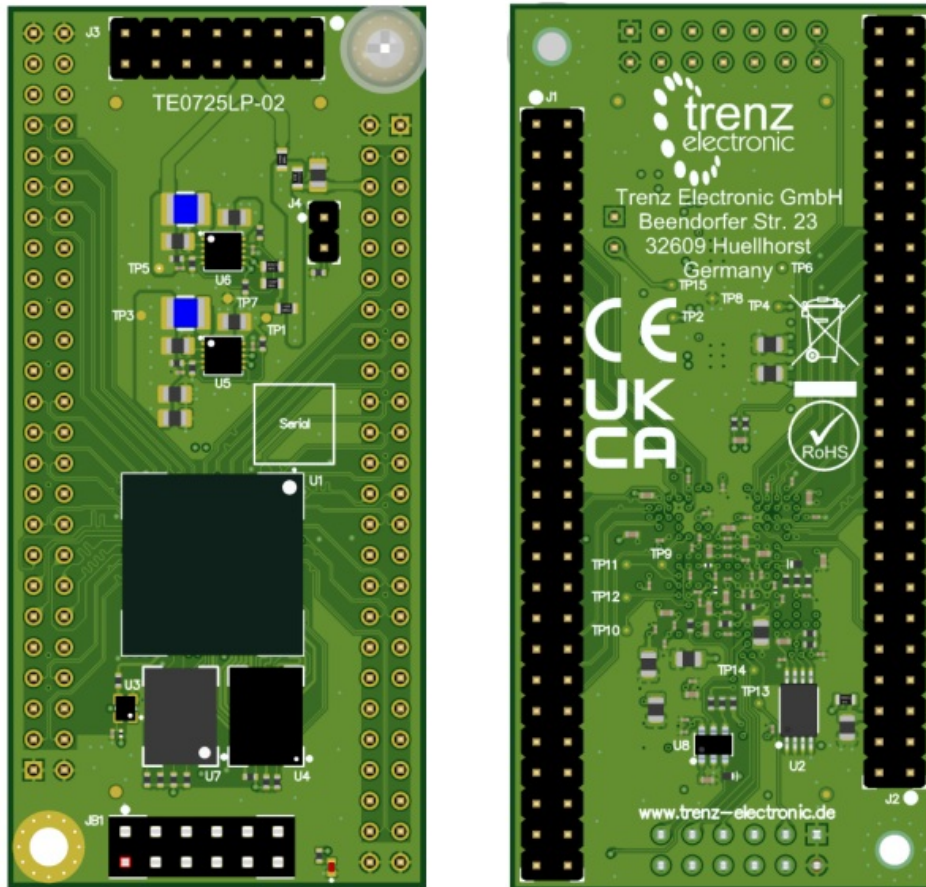


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Trenz Electronic TE0725LP System On Modules



Specifications

- Title: Legal Notices Modules
- Number: TE0725LP 72C-AU
- Date: 2023-07-14
- Copyright: Trenz Electronic GmbH
- Filename: Legal Notices Modules.SchDoc

Product Information

- The TE0725LP module is designed and manufactured by Trenz Electronic GmbH. It features an Xilinx Artix-7 FPGA, XADC, SPI_SCK, JTAG, Serial Flash, UART, HyperRAM, and various IOs/LVDS pairs. The module includes several enhancements and modifications for improved performance and functionality.

Legal Disclaimer

- It is important to note that the schematics and documentation provided with the TE0725LP module are protected under copyright. Reverse engineering or recreating the design, even with modifications, is strictly prohibited. The materials are intended

for informational purposes only.

Changes List

- The TE0725LP module has undergone several revisions with enhancements such as component replacements, additions, and modifications. Refer to the latest revision changes document for the information on the updates.

System Overview

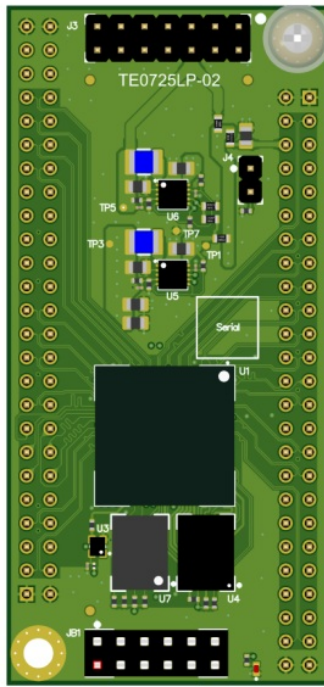
- The TE0725LP module has a comprehensive system overview detailing the components, interfaces, and connections of the FPGA module. Familiarize yourself with the system architecture to understand the functionalities of different elements.

Power-On Sequencing

- For proper operation, ensure that the voltage input (VIN) is set to 3.3V. The module includes various power rails such as VCCIO35, VCCIO34, VCCINT, and VCCBRAM. Follow the specified power-on sequencing to ensure correct power distribution within the module.

Regarding the usage of our schematics and similar documentation for the Trenz module TE0725LP.

- The project is protected under copyright, and we strongly and strictly prohibit reverse engineering or recreation, even if the design is just adapted or modified. TE0725LP is protected under such right, and in case of plagiarism, we will have to do anything necessary in order to protect our assets.
- Schematics and other handouts serve for informational purposes only!



	Title: Legal Notices Modules		
	A4	Number: TE0725LP 72C-AU	Rev. 04
	Date: 2023-07-14	Copyright: Trenz Electronic GmbH	Page 1 of 12
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REV	Description	
-01	Initial revision	
-02	<ol style="list-style-type: none">1. [L1], [L2], [L6] ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000.2. Added [J4] and [R30] (JTAG only Enable).3. Added Diode [D1] for INIT reset.4. Added Diode [D3] for [U8] input protection.5. Added a pull-up resistor [R29] on [U7B] RESET, pin A4.6. Added a pull-up resistor [R31] on SPI_DQ2, pin C4.7. Added capacitor [C22] to avoid false resetting.8. Resistors [R13], [R72], [R29], [R18], [R20], [R31], [R21], [R3], [R9] value 5.6kOhms changed to 2.2kOhms.9. Resistor [R7] 10 kOhms replaced with 2.2 kOhms to optimise the voltage divider values.10. Resistors [R4], [R15] value 2kOhms changed to 330Ohms according to AMD specification (UG470).11. Added a 2.4 kOhm resistor [R32].12. Capacitor [C21] value 47 uF changed to 100 uF, added additional decoupling capacitors [C33], [C34], [C35] according to AMD specification (UG 483).13. Added [C24] to improve noise immunity.14. AVCC power rail filter is improved. [C1] connected to 1.8V.15. Added pages Legal notices, power diagram.16. Added System Overview.17. Added testpoints [TP1] - [TP15].	VG (05.08.2024)

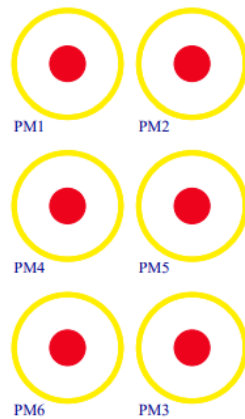
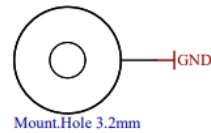
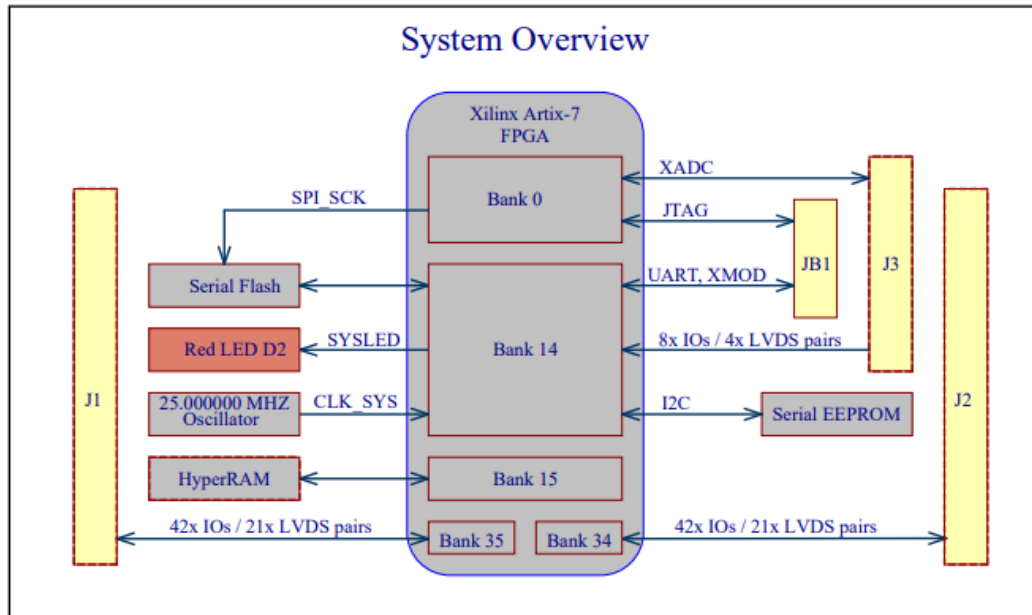
	Title: TE0725LP - Changes list		
	A4	Number: TE0725LP 72C-AU	Rev. 02
	Date: 2023-07-14	Copyright: Trenz Electronic GmbH	Page2 of 12
	Filename: Revision_Changes.SchDoc		

U FPGA PWR MISC
FPGA PWR MISC.SchDoc

Power_Diagram
Power_Diagram.SchDoc

U_PowerSupply
POWER.SchDoc

System Overview



Serial
Serial
SerialNumber 6,3 x 6.3mm

RoHS1

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY

UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

MECH1

TE Address Overlay

LOGO ADDRESS

LOGO1


TE Logo PRINT Layer

LOGO PRINT

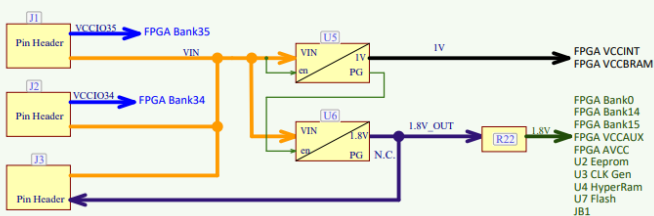
CE

CE Logo on Top Overlay

CE-TOPOVERLAY

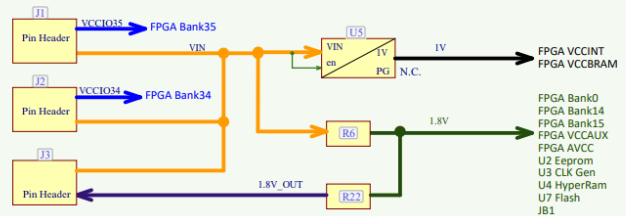
Drawn by	VG			Title: TE0725LP - Overview	
Checked by	MT			A4	Number: TE0725LP 72C-AU
Assembly variant	72C-AU			Rev.	02
Created by				Date:	2023-07-14
Modified by				Copyright:	Trenz Electronic GmbH
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Power-on sequencing: VIN = 3.3V



Depends on assembly option

Power-on sequencing: VIN = 1.8V

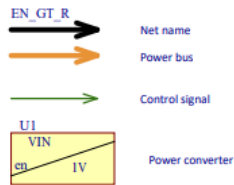


Depends on assembly option

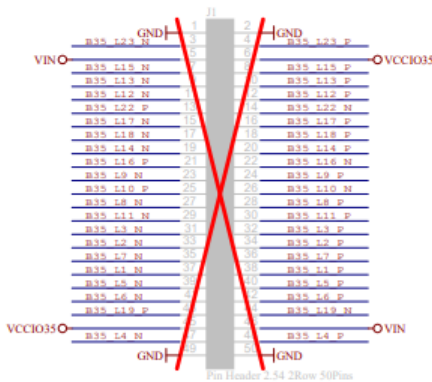
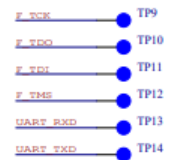
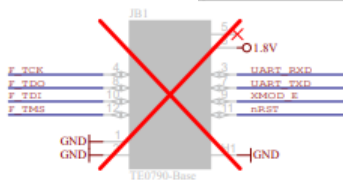
Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3V / 1.8V	+/-3%	Micromodule Power	J1, J2, J3
1.8V_OUT	OUT	1.8V	+/-3%	Power supply for external use	J3
VCCIO35	IN	1.8V ... 3.3V	+/-3%	Power of Bank 35	J1
VCCIO34	IN	1.8V ... 3.3V	+/-3%	Power of Bank 34	J2

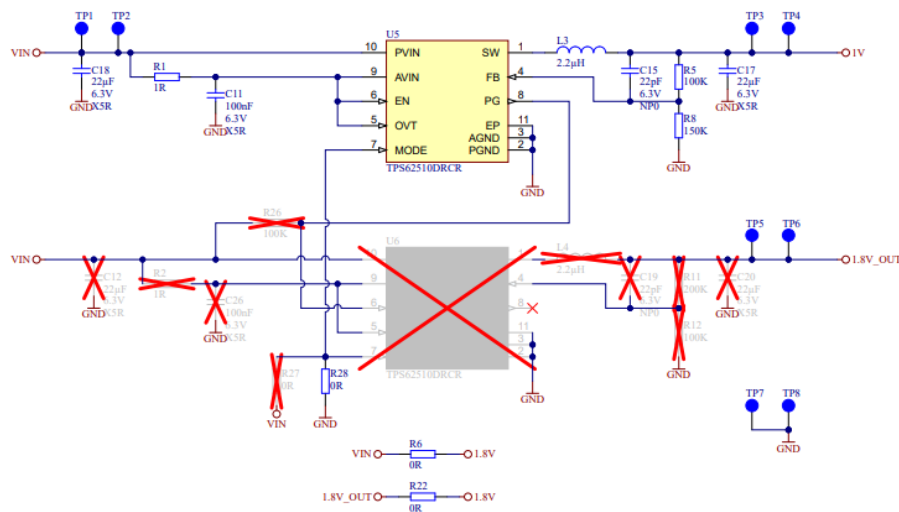
Programmable Logic, supplied by power rail
Low-Power Domain, supplied by power rail




				Title: Power Diagram	
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Title: TE0725LP - B14 & B16		
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	Title: TE0725LP - POWER		
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FAQS

Can I modify the design of the TE0725LP module?

: No, the design of the TE0725LP module is protected under copyright, and any form of reverse engineering or recreation is strictly prohibited.

How can I stay updated on revisions and changes to the module?

: Refer to the revision changes document provided by Trenz Electronic GmbH to stay informed about any modifications or enhancements made to the TE0725LP module.

Documents / Resources



[Trenz Electronic TE0725LP System On Modules \[pdf\]](#) User Manual
TE0725LP, 72C-AU, TE0725LP System On Modules, TE0725LP, System
On Modules, Modules

References

- [User Manual](#)

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electronic

◆ 72C-AU, Modules, System On Modules, TE0725LP, TE0725LP System On Modules, trenz
electronic

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