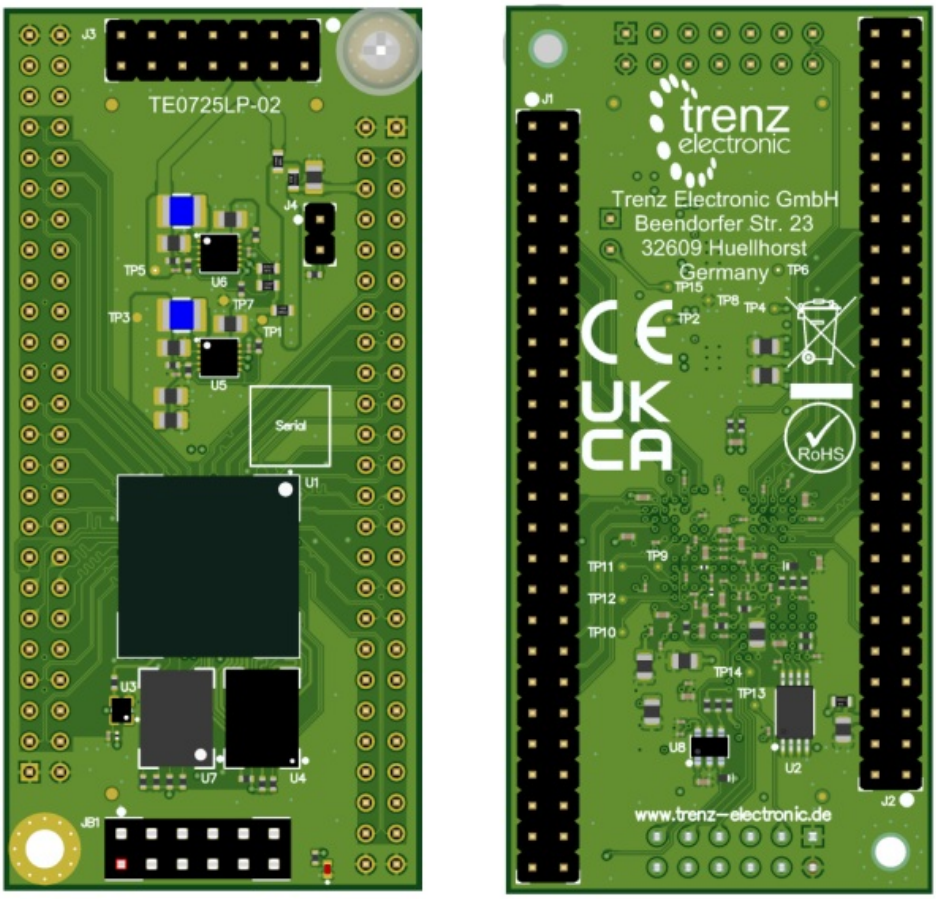
Contents [hide]

Trenz Electronic TE0725LP Integrated Circuits Module



Specifications

- Product Name: TE0725LP
- Manufacturer: Trenz Electronic GmbH
- Date: 2023-07-14
- Copyright: Trenz Electronic GmbH
- Revision: 04
- Pages: 12

Product Information

The TE0725LP module is designed and manufactured by Trenz Electronic GmbH. It features an Xilinx Artix-7 FPGA, various interfaces including XADC, SPI, JTAG, Serial Flash, UART, and more. The module includes power rails, decoupling capacitors, resistors, and other components for optimal performance.

Power-on Sequencing

Ensure that the input voltage (VIN) is set to 3.3V. Connect the power supplies to the respective pins as indicated:

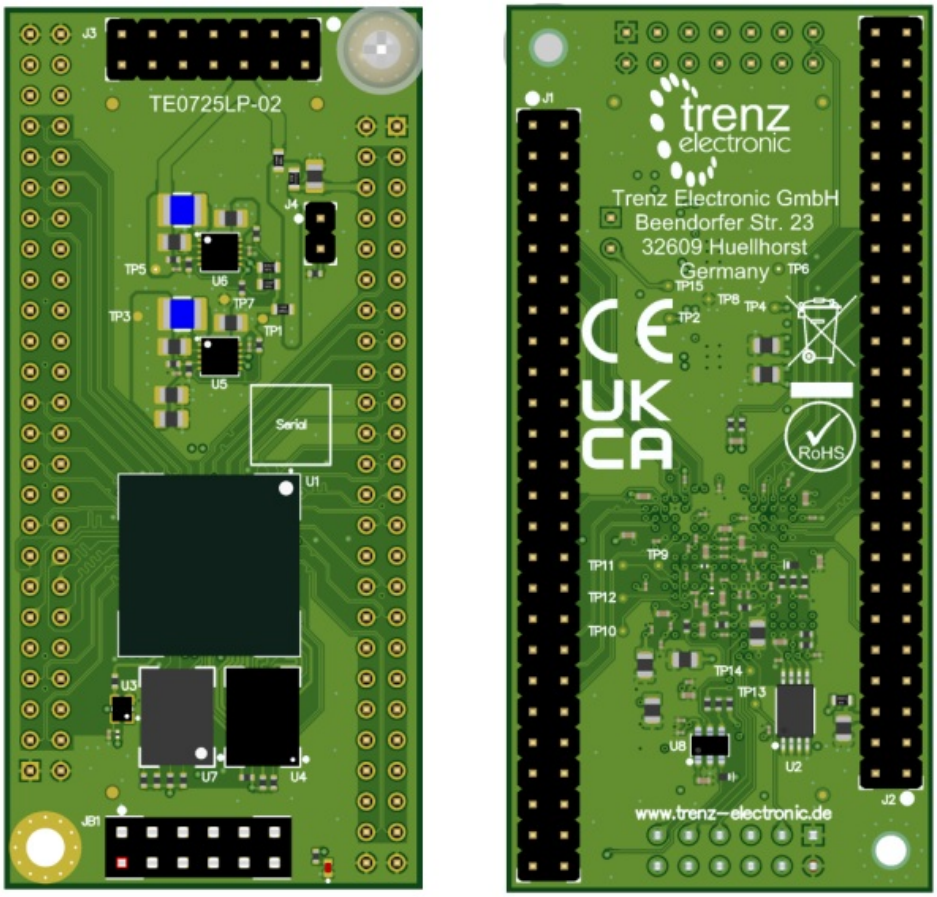
- J1 VCCIO35 – FPGA Bank35
- J2 VCCIO34 – FPGA Bank34
- J3 Pin Header

Component Changes

- The TE0725LP module has undergone revisions and component changes for improved performance. Refer to the revision log for details on component replacements and additions.

System Overview

The module includes an overview of the system components, such as the Xilinx Artix-7 FPGA, various interfaces, LEDs, oscillators, and mounting holes. Familiarize yourself with the system layfor proper operation integration.



- Regarding the usage of our schematics and similar documentation for the Trenz module TE0725LP.
- The project is protected under copyright, and we strongly and strictly prohibit reverse

engineering or recreation, even if the design is just adapted or modified. TE0725LP is protected under such right, and in case of plagiarism, we will have to do anything necessary in order to protect our assets.

- Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: Legal Notices Modules	
	A4 / Number: TE0725LP 72C-A	Rev. 04
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	Filename: Legal Notices Modules.SchDoc	

REV	Description	
-01	Initial revision	
-02	1. L1 , L2 , L6 ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000. 2. Added J4 and R30 (JTAG only Enable). 3. Added Diode D1 for INIT reset. 4. Added Diode D3 for U8 input protection. 5. Added a pull-up resistor R29 on U7B RESET, pin A4. 6. Added a pull-up resistor R31 on SPI_DQ2, pin C4. 7. Added capacitor C22 to avoid false resetting. 8. Resistors R13 , R72 , R29 , R18 , R20 , R31 , R21 , R3 , R9 value 5.6kOhms changed to 2.2kOhms. 9. Resistor R7 10 kOhms replaced with 2.2 kOhms to optimise the voltage divider values. 10. Resistors R4 , R15 value 2kOhms changed to 330Ohms according to AMD specification (UG470). 11. Added a 2.4 kOhm resistor R32 . 12. Capacitor C21 value 47 uF changed to 100 uF, added additional decoupling capacitors C33 , C34 , C35 according to AMD specification (UG 483). 13. Added C24 to improve noise immunity. 14. AVCC power rail filter is improved. C1 connected to 1.8V. 15. Added pages Legal notices, power diagram. 16. Added System Overview. 17. Added testpoints TP1 - TP15 .	VG (05.08.2024)

trenz electronic	Title: TE0725LP - Changes list	
	A4 / Number: TE0725LP 72C-A	Rev. 02
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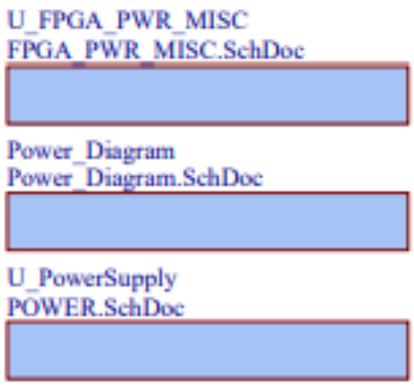
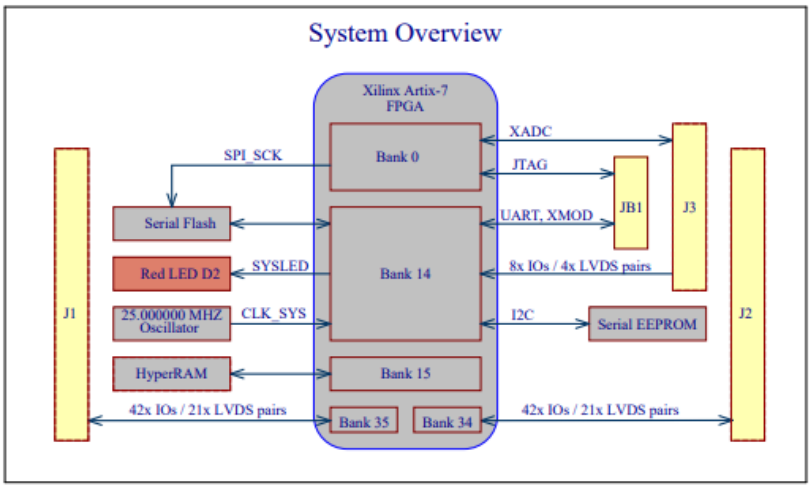
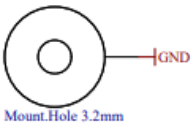
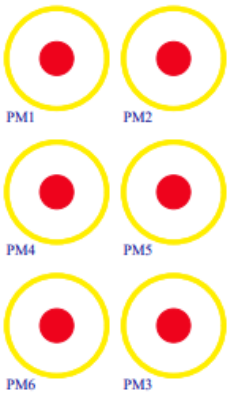






Mount.Hole 3.2mm



Serial
Serial
Serialnumber 6,3 x 6.3mm

RoHS1
RoHS Logo on Top Overlay
RoHS-TOPOVERLAY

UKCA
UKCA Logo on Top Overlay
UKCA-TOPOVERLAY

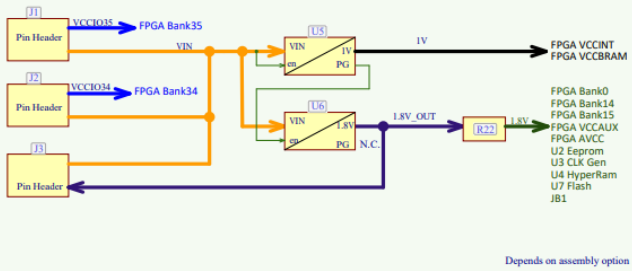
MECH1
TE Address Overlay
LOGO ADDRESS

LOGO1
TE Logo PRINT Layer
LOGO PRINT

CE
CE Logo on Top Overlay
CE-TOPOVERLAY

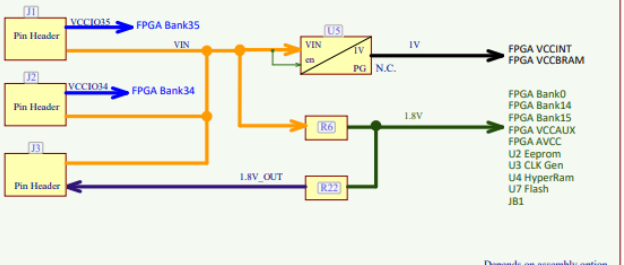
Drawn by	VG	Title: TE0725LP - Overview		
Checked by	MT			
Assembly variant	72C-A	A4	Number: TE0725LP 72C-A	Rev. 02
Created by				
Modified by		Date: 2023-07-14	Copyright: Trenz Electronic GmbH	Page3 of 12
Modified at		Filename: TE0725LP.SchDoc		

Power-on sequencing: VIN = 3.3V



Depends on assembly option

Power-on sequencing: VIN = 1.8V

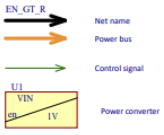


Depends on assembly option

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3V / 1.8V	+/-3%	Micromodule Power	J1, J2, J3
1.8V_OUT	OUT	1.8V	+/-3%	Power supply for external use	J3
VCCIO35	IN	1.8V ... 3.3V	+/-3%	Power of Bank 35	J1
VCCIO34	IN	1.8V ... 3.3V	+/-3%	Power of Bank 34	J2

Programmable Logic, supplied by power rail
Low-Power Domain, supplied by power rail



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Title:	Power Diagram		
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Title:	TE0725LP - B2B Connectors		
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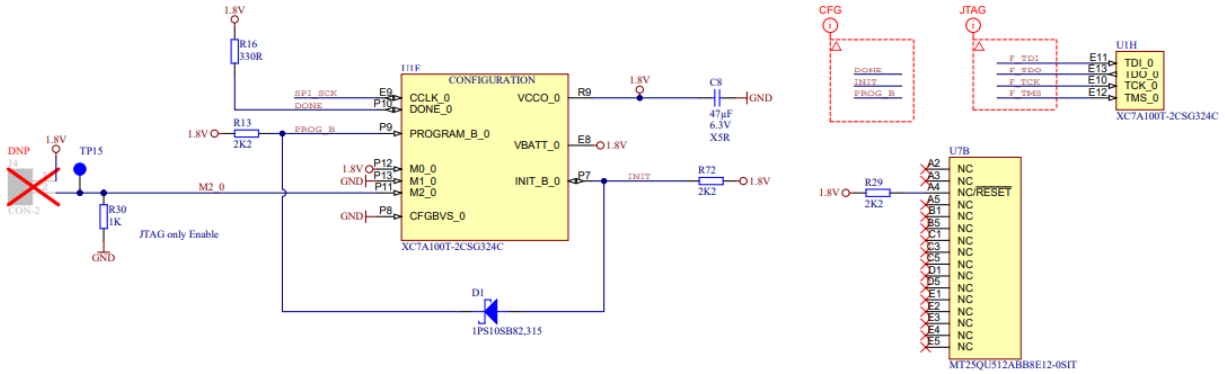
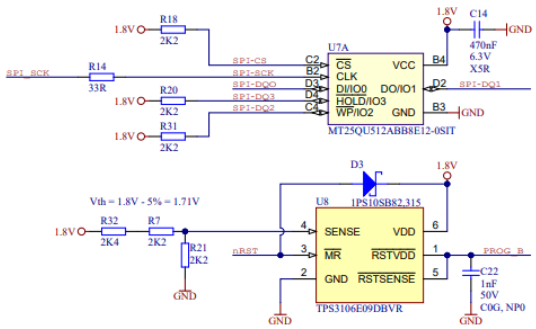


Table 2-1: **7 Series FPGA Configuration Modes (UG470)**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32(1)	Input
Slave Serial(2)	111	x1	Input



trenz electronic	Title: TE0725LP - FPGA CFG		
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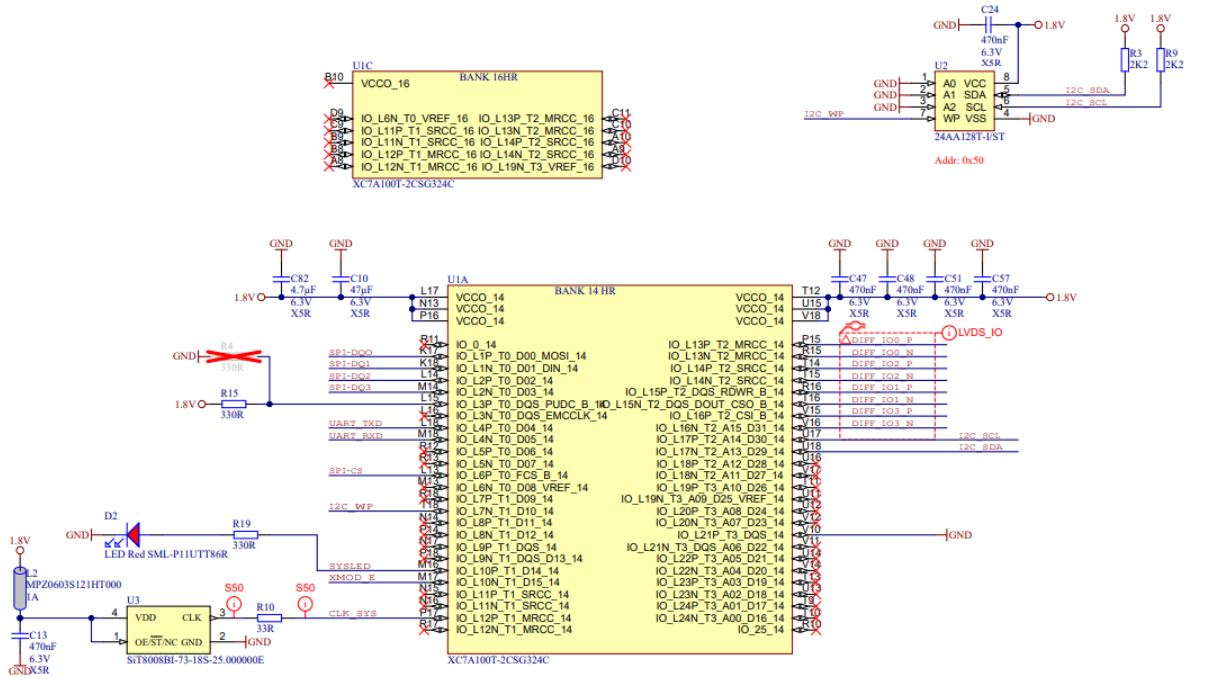

trenz electronic	Title: TE0725LP - B14 & B16		
	A4	Number: TE0725LP 72C-A	Rev. 02
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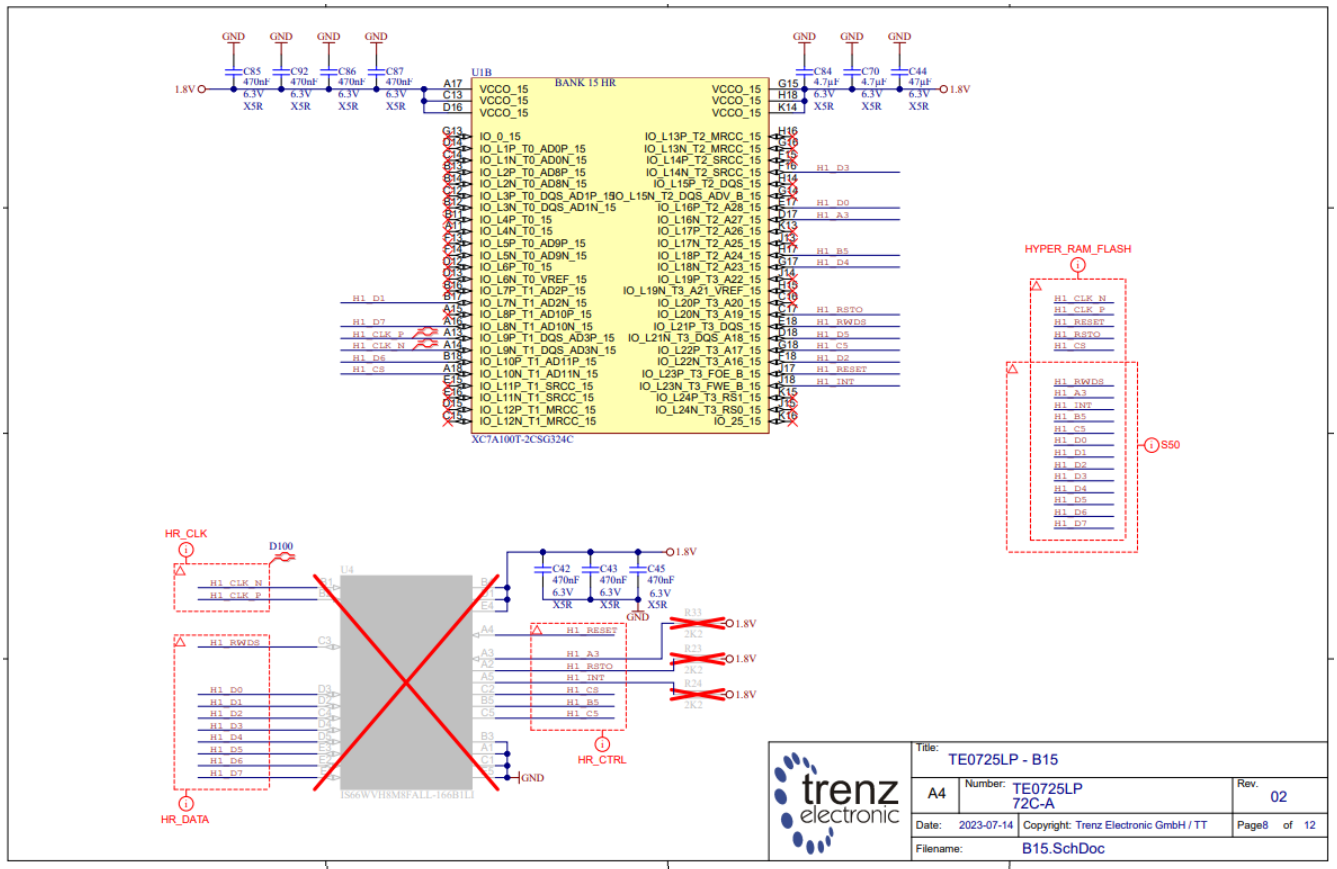

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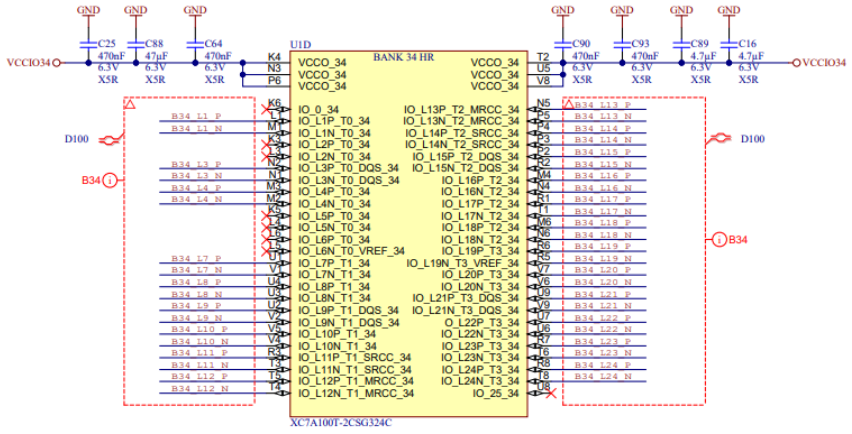

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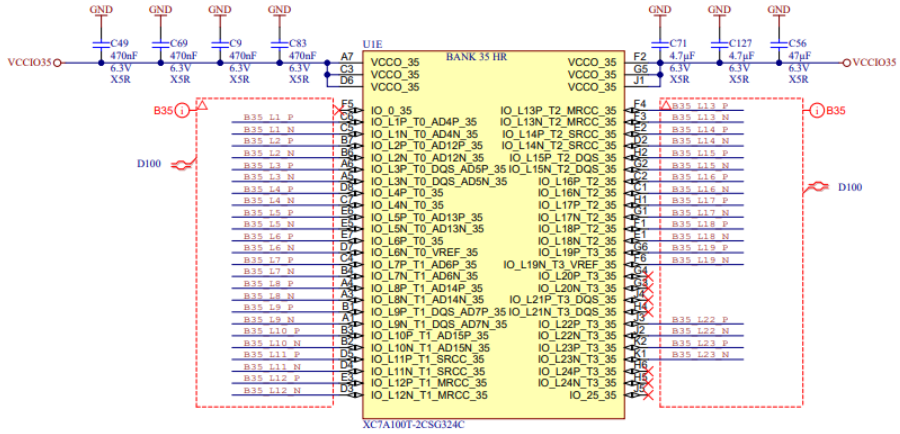

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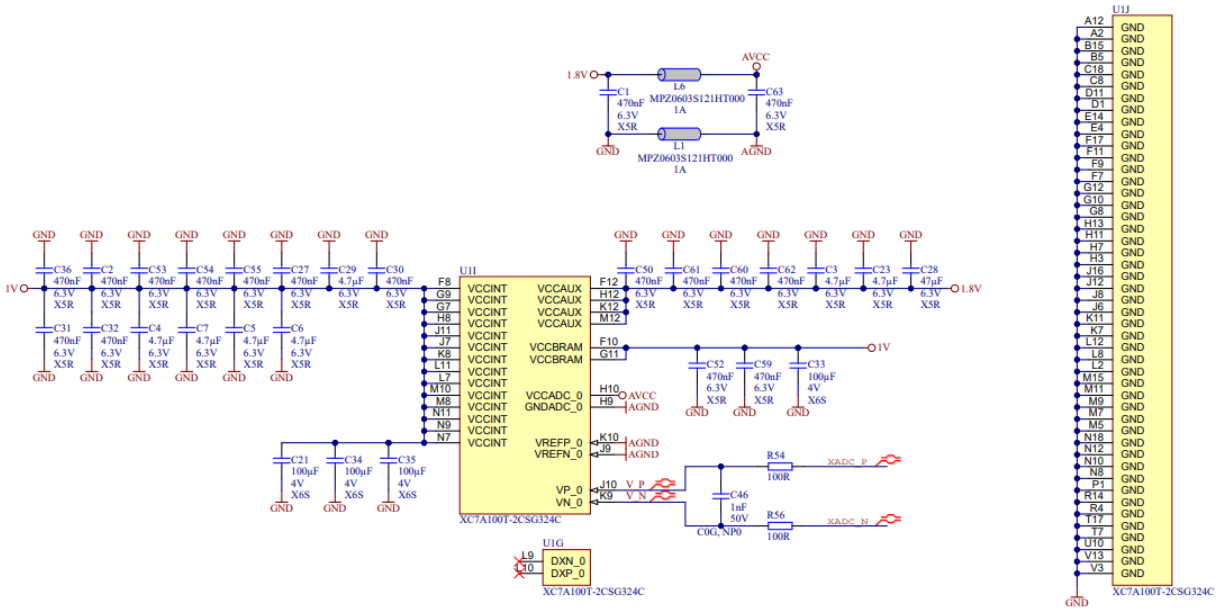

Title:	TE0725LP - FPGA PWR MISC		
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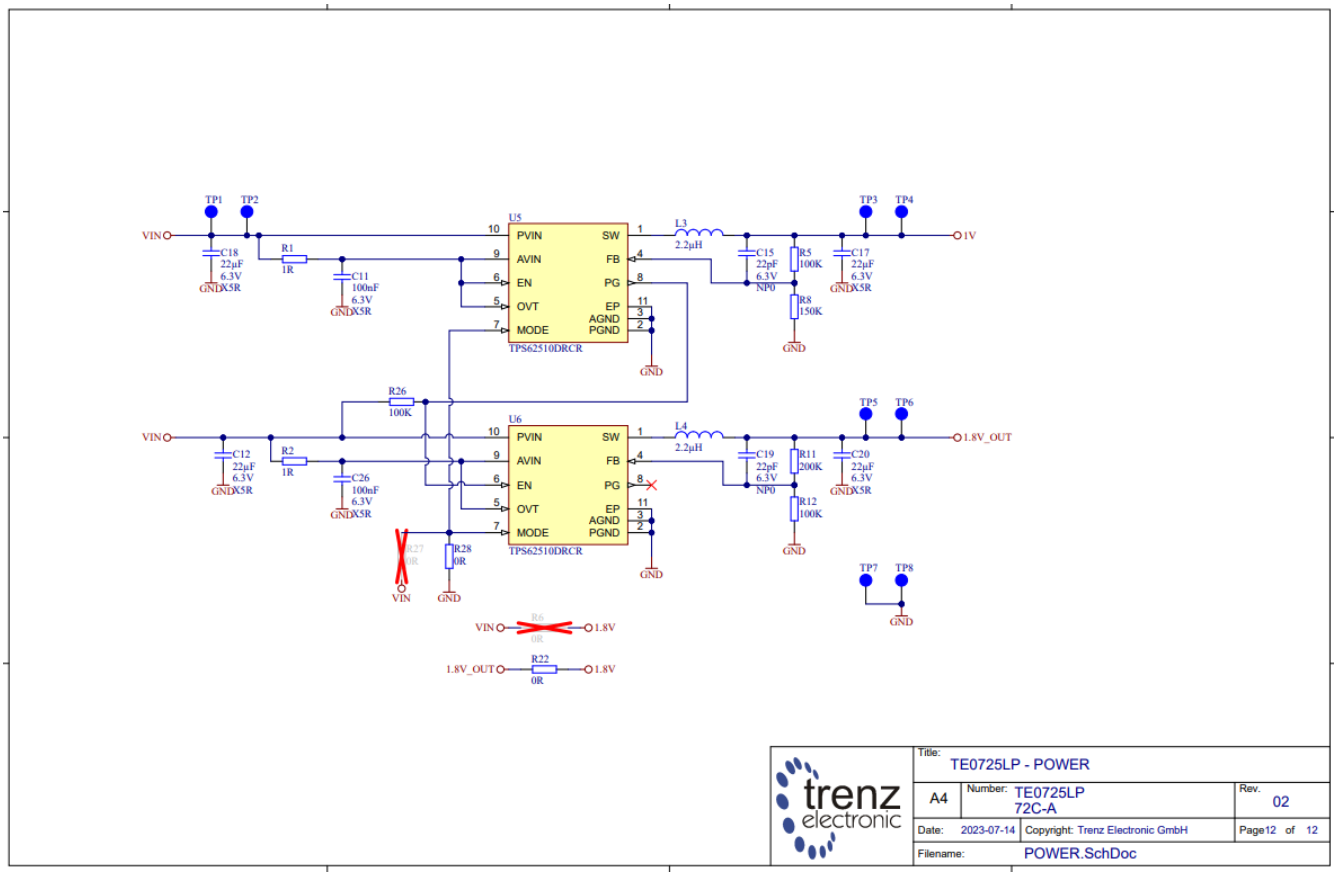

Frequently Asked Questions

: Can I modify the design of the TE0725LP module?

No, the TE0725LP module is protected under copyright laws, and any reverse engineering or recreation of the design is strictly prohibited by Trenz Electronic GmbH.

What is the power-on sequencing for the TE0725LP module?

: The module requires a 3.3V input voltage for proper power-on sequencing. Ensure correct connections to the designated pins for VCCIO35, VCCIO34, and other power supplies.

Are there any specific component changes in the latest revision of the TE0725LP module?

: Yes, the latest revision includes various component changes such as resistor value

adjustments, capacitor replacements, and additional decoupling capacitors to meet AMD specifications.

Documents / Resources

	Trenz Electronic TE0725LP Integrated Circuits Module [pdf] User Guide TE0725LP, 72C-A, TE0725LP Integrated Circuits Module, TE0725LP, Integrated Circuits Module, Circuits Module, Module

References

- User Manual

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72C-A, Circuits Module, Integrated Circuits Module, Module, TE0725LP, TE0725LP Integrated Circuits Module, trenz electronic

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