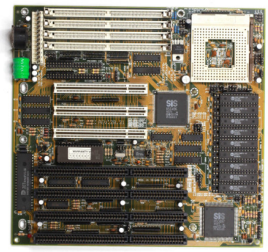

the retro web S4967 486 Cache System Board User Manual

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2 FEATURES
3 CHAPTER 2 SYSTEM BOARD LAYOUT
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CHAPTER 1 INTRODUCTION

SYSTEM OVERVIEW

The S4967 Rev:2B.31 486 Cache system board Is 2/3 Baby AT-sized, fully PC/AT compatible and offers outstanding performance and features.
With 128K/256K/512K/1M cache memory on board, this system board Is really a high speed machine that is well suited for building advanced personal computers or workstat- lons.
The $4967 Rev:2B.31 486 Cache system board is designed with the SIS 85C496/85C497 chipset which are highly integrated. With this chipset, there are only a few discrete
devices required, which allows 4 memory banks to be placed on the board. The size of the memory can be scaled from 1 MB up to 255 MB.

FEATURES

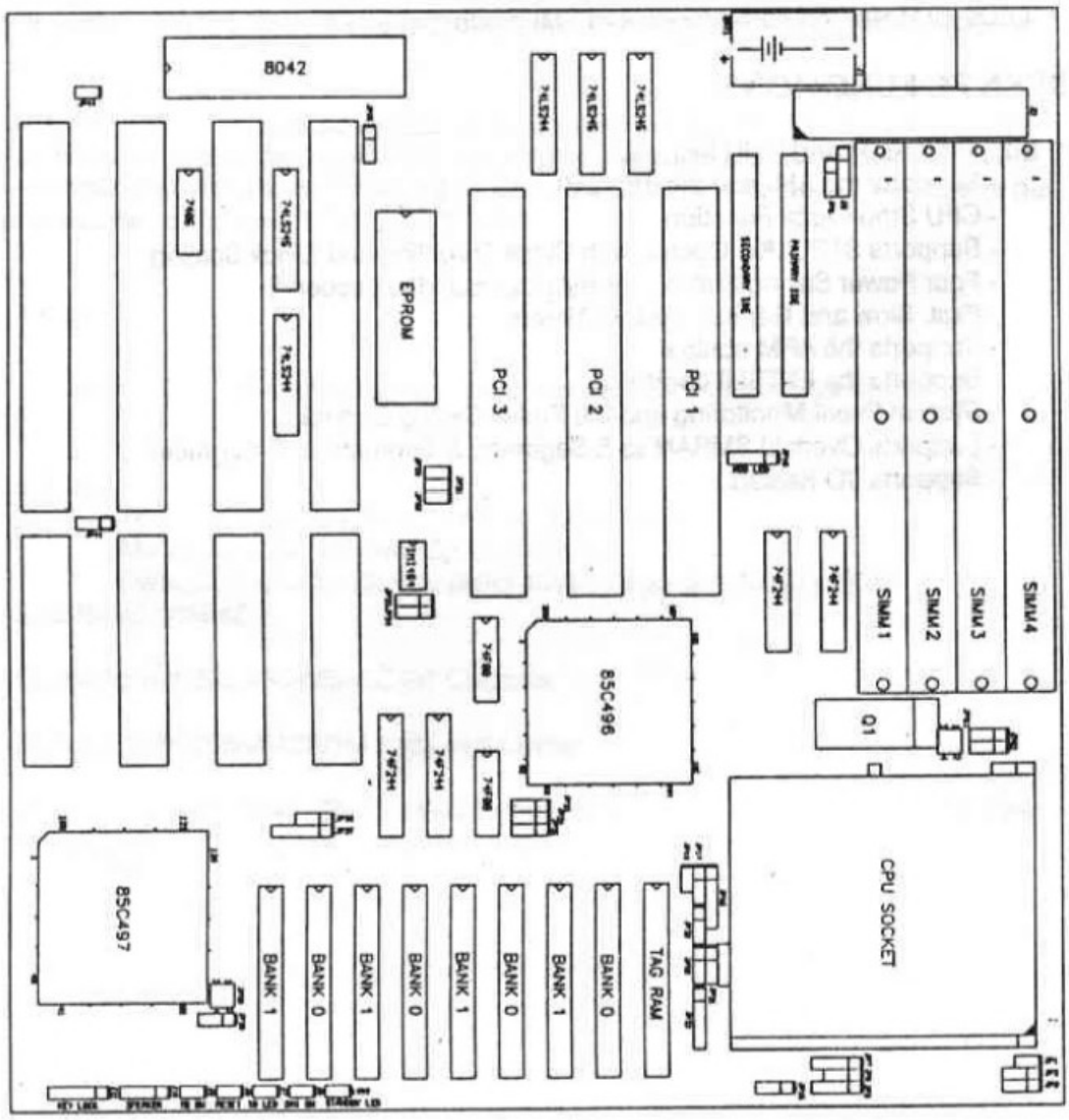
The $4967 Rev:2B.31 486 Cache system board supports (or includes) the following features:
* **Support**

Intel 486SX/SX2/DX/DX2,DX4(3.45V),P24D,P24T AMD DX,DX2/DX4(NV8T),OX2/DX4(SVEB) Cyrix SX/DX/DX2,DX2-V66/VB0(3.45V),DX4(3.45V), 15×86 (3.45V) in 25/33/40/SOMHZ

- Designed with SIS 85C496/85C497 Chipsets
- Support 128K/256K/512K/1M 2nd Level Cache
- Support 4 DRAM Banks. The DRAM can be bul with elther Single-Sided or Double- Sided SIMMs. The maximum memory Is up to 255MB
- Software-controlied shadow RAM for system and/or video BIOS
- Three 32-bit PCI local bus slots, four 16-bk expansion slots

CHAPTER 2 SYSTEM BOARD LAYOUT

Placement of the S486 Rev:2B.31



SILKSCREEN FOR COMPONENT SIDE

CHAPTER 3 HARDWARE CONFIGURATION

Before the system Is ready to operate, the hardware must be configured to allow for various functions within the system. To configure the $4967 Rev:2B.31 Cache system
board is a simple task, only a few Jumpers, connectors, and sockets needs to be selected.

CACIIE MEMORY SOCKETS

The $4967 Rev:2B.31 Cache system board supports 2 banks of SRAM which provides either 126/256K/512K/1MB of cache memory. The following table lists the detailed information.

Cache Size	Bank 0	Bank 1	Tag
128 K	four 32K x 8		one 8K x 8
256 K	four 32K x 8	four 32K x 8	one 16K x 8 or 32K x 8
256 K	four 64K x 8		one 16K x 8 or 32K x 8
512 K	four 64K x 8	four 64K x 8	one 32K x 8
512 K	four 128K x 8		one 32K x 8
1MB	four 128K x 8	four 128K x 8	one 64K x 8

The corresponding bank to part identification are as follows:
Bank 0 – U9, U11, U19, U24
Bank 1 – U10, U14, U20, U2
Tag =~ U8 –

CACHE Size Select

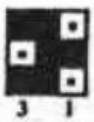
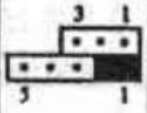
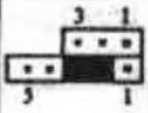
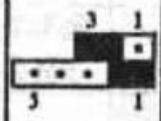
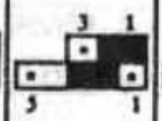
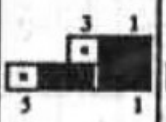
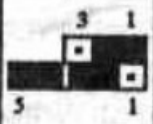
	128K	256K	256K	512K	512K	1MB
JP23 JP24 JP25						
JP36 JP37						
TAG	8KX8	32KX8	32KX8	32KX8	32KX8	64KX8
BANK 0 U9,U11, U19,U24	32KX8	32KX8	64KX8	64KX8	128KX8	128KX8
BANK 1 U10,U14, U20,U25	X	32KX8	X	64KX8	X	128KX8

Table 3-1 Cache Size Select

Cache size	Cacheable DRAM size (8 bit tag)	Cacheable DRAM size (7 bit tag)
– 64K byte	16fvW fe 32M-byte 64M byte	8M byte
—128K byte		t6M byte 32M byte
256K byte		
512Kb_yte	128M byte	64M byte
1M byte	255M byte	128M byte

Table 3-2 Cache Size Options

Processor Type	Ll Cache Mode	L2 Cache Mode
4 86SX/DX/DX2/ DX4/S L-Enhanced	WT	WT/WB WTNV B
P24D/P24T	WT/WB	
Cyrix M7/DX4/M1sc	WT/WB	WT/WB
Am486DXL/DX2 DX4-10 0 NV8T	WE	WT/WB
Arn486Dr47100/120 SV 8B	WI/WS	WT/WB

Table 3-3 Lt/L2 Cache Configurations

Cycle Definition Hiiinii–emory	Total Clocks at Host Interface			S0MHz
	251V1Hz	33MHz	40MHz	
Single-Read (L2 Cache Hit)	2	2	2	2
—-S ri-i-gle-Reacf(12 Cache Miss)	3	4	5	6
—Teurst-Read (L 2 Cache Hit)	2-1-1-1	2-1-1-1	3-2-2-2	3-2-2-2
urst-Read (L2 Cache Miss)	3-2-2-2	4-3-3-3	5-4-4-4	6-5-5-5
–Single-Write (L2 Cache Hit)	2	2/VVB,3/WT	3/W6,4/WT	3/VVB,5NVI
Single-Write (L2 Cache Miss)	2 2-1-1-1/WB 3-2-2-2/WT 3-2-2-2	3 2-1-1-1/WB 3-2-2-2/WT 3-2-2-2	4 3-2-2-2/WB 4-3-3-3/WT	5 3-2-2-2/WB 5-4-4-4/WT
*Burst-Write (U C ache Hit)				
Burst-Write (U Cache Miss)			4-3-3-3	5-4-4-4

Table 3-4 U Cache/DRAM Performance Options

SHADOW CACHEABLE

UMB (Upper Memory Block) which Is not main memory area Is by default non-cacheable. However, once shadowed, the RAM segments 0C0000-OFFFFFh can be further cached in Level 2 and Level 1 cache. Each 32K memory segments can be Individually enabled to be cacheable by both 85C495's secondary level cache and CPU's internal cache.SIMM SOCKETS

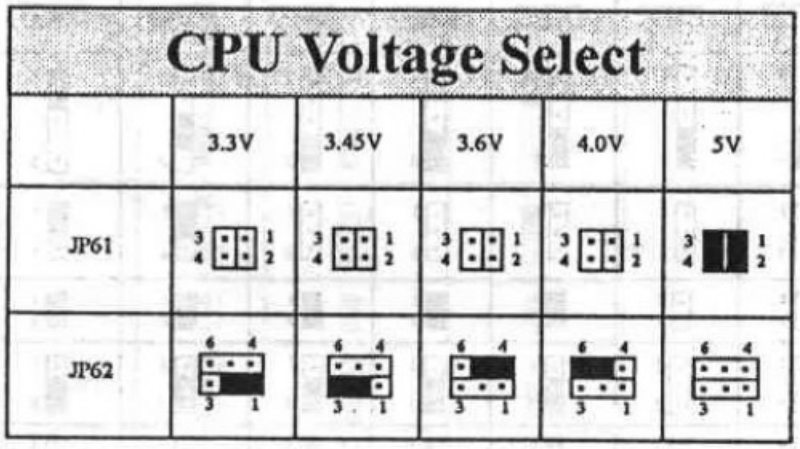
je $4967 Rev:2B.31 Cache system board will support 4 DRAM banks, Bank 0 and Bank 1 k 2 and Bank 3 in SIMM sockets use 72-pin SIMM : DRAM type can be 256K, 512K, , 2M, 4M, or 16M by 32/36 bits Single side or Double side Fast Page Mode and faster in BONs.

the use of 256K, 512K, 1M, 2M, 4M or 16M DRAM modules, 1M and upto 255 M of memory can be attained. The installation of DRAM SIMMs Is "Table-free", which

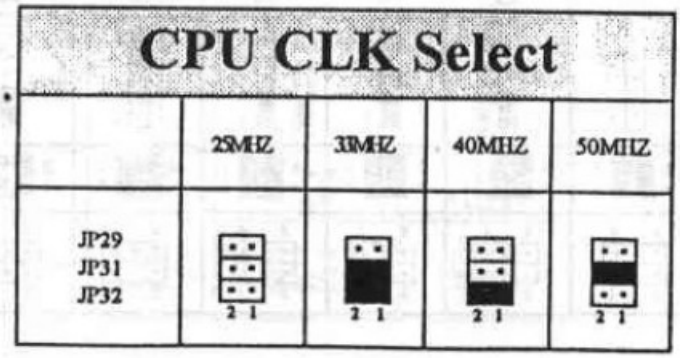
the SIMMs be installed into any siot location and any combinations.

PU INSTALLATION :

'U Voltage Select



'U CLK Select



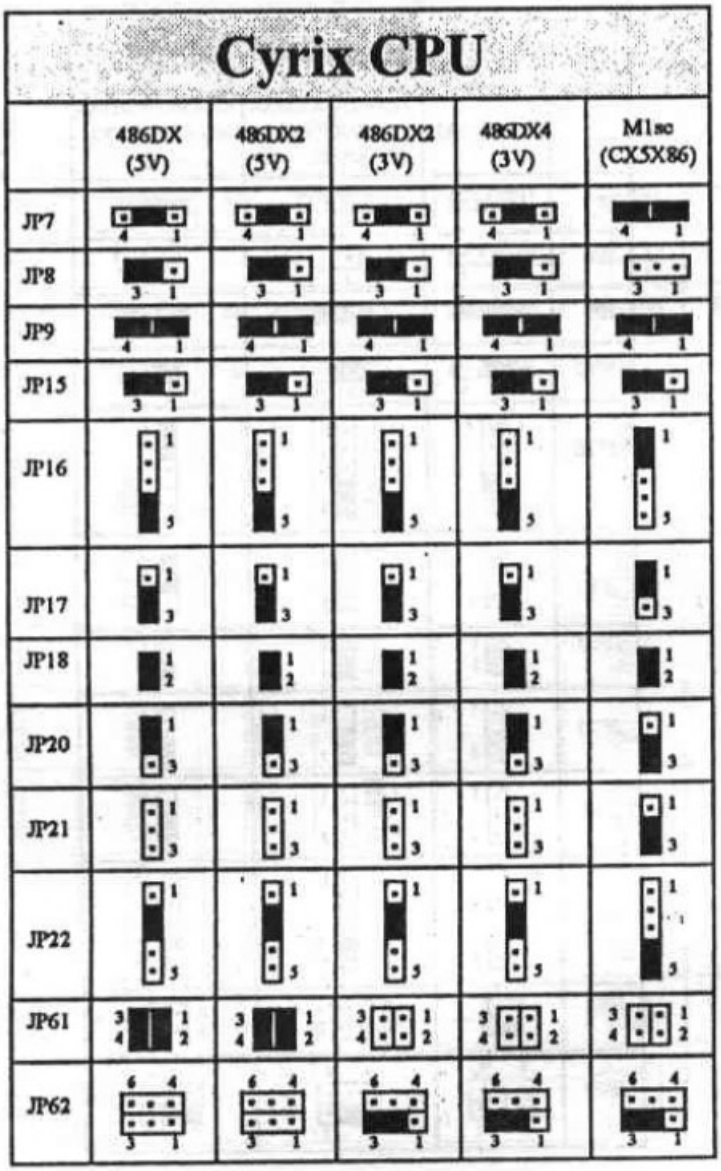
CPU Type select

Intel CPU

	486SX	486DX	SL Enhance 486SX	SL Enhance 486DX	SL Enhance 486DX2	P24T	P24D	P24C
JP7								
JP8								
JP9								
JP15								
JP16								
JP17								
JP18								
JP20								
JP21								
JP22								
JP61								
JP62								

AMD CPU

	Am486DXL	Am486DX2/DX4 -66/80/100 NV8T	Am486DX2/DX4 -66/80/100/120 SV8B
JP7			
JP8			
JP9			
JP15			
JP16			
JP17			
JP18			
JP20			
JP21			
JP22			
JP61			
JP62			


Cyrix CPU
486DX (5V)
486DX2 (5V)
486DX2 (3V)
486DX4 (3V)
Misc (CX5X86)
JP7
JP8
JP9
JP15
JP16
JP17
JP18
JP20
JP21
JP22
JP61
JP62

JUMPER:

(1) JP1 CX486S2 Select

Pin #	Assignment
SHORT	CX486S2 only
OPEN	OTHER CPU

(2) JP2 CLKMUL/WB_WT Select

* FOR AMD CPU :

Pin #	Assignment
1 - 2	3X
2 - 3	2X
OPEN	3X

* FOR P24D CPU :

Pin #	Assignment
1 - 2	Write-Back
2 - 3	Write-Through

(3) JP3 P24T WB_WT Select

Pin #	Assignment
1 - 2	Write-Back
2 - 3	Write-Through

(4) JP28 BIOS Type Selection

Pin#	Assignment
1 - 2,5 - 6	FLASH BIOS
2 - 3,4 - 5	EPROM BIOS

(5) JP33 PCI CLK Select

Pin #	Assignment
1 - 2	PCICLK = CPUCLK
2 - 3	PCICLK = 1/2 CPUCLK

(6) JP34 CPU CLK Delay Select

Pin #	Assignment
1 - 2	Normal
2 - 3	CPUCLK Delay

(7) JP6/JP35 RTC Discharge Select

Pin #	Assignment
1 - 2	Normal
2 - 3	Discharge RTC CMOS

NOTE : When you can't enter system setup, you must use JP6/JP35 to discharge RTC CMOS.

(8) JP38 GREEN control (SMOUT connector)

Pin#	Assignment
1 - 2	GREEN Outlet connector 1 (For Green Power-Supply)
3 - 4	GREEN Outlet connector 2 (For Green Power-Supply)

(9) JP39 Stop CPU Clock control

Pin#	Assignment
1 - 2	CPUCLK down by chipset
2 - 3	CPUCLK down by CPU (AMD486DXL is not included)

(10) JP41 DREQ signal control

Pin #	Assignment
1 - 2	DREQ pull-up
2 - 3	DREQ pull-down

(11) JP44 MONITOR Type selection

Pin#	Assignment
SHORT	COLOR Monitor
OPEN	MONO Monitor

(12) JP50 DX4/5x86/AmDX4 SV8B CLKMUL

Pin#	Assignment
1 - 2	2.5X(For DX4 only)
2 - 3	2X(DX4/5x86/AmDX4 SV8B)
OPEN	3X(DX4/5x86/AmDX4 SV8B)

CONNECTORS:

(1) BT1A Rechargeable Battery

Pin #	Assignment
1	Battery Positive
2	Ground

(2) J1 Keyboard

Pin #	Assignment
1	Keyboard Clock
2	Keyboard Data
3	No Connection
4	Ground
5	+ 5V DC

(3) J2 Power Connector

Pin #	Assignment
1	Power Good
2	+ 5V DC
3	+12V DC
4	- 12V DC
5	Ground
6	Ground
7	Ground
8	Ground
9	- 5V DC
10	+ 5V DC
11	+ 5V DC
12	+ 5V DC

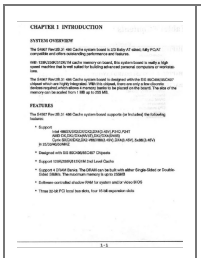
(4) J3 4.5V External Battery

Pin #	Assignment
1	Battery Positive
2	No Connection
3	Ground
4	Ground

(5) J6 Hardware SMI Break Switch

Pin#	Assignment
SHORT	Immediately into SMI mode
OPEN	Normal operation

Documents / Resources

	the retro web S4967 486 Cache System Board [pdf] User Manual S4967 486 Cache System Board, S4967, 486 Cache System Board, Cache System Board, System Board, Board