terasic TRDB-D5M Digital Camera Development Kit User Manual

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Contents

About the Kit

The TRDB_D5M Kit provides everything you need to develop a 5 Mega Pixel Digital Camera on the Altera DE4 / DE2_115 / DE2-70 / DE2 / DE1 boards. The kit contains hardware design (in Verilog) and software to load the picture taken into a PC and save it as a BMP or JPG file (DE2-70 only). The Getting Started User Guide enables users to exercise the digital camera functions. This chapter provides users key information about the kit.

Kit Contents

Figure 1-1 shows the photo of the TRDB_D5M package. The package includes:

1. The TRDB_D5M (D5M) board with one CMOS sensor.
2. A reference design CD.

Figure 1-1 The TRDB_D5M (D5M) Package Content (CD not including)

Assemble the Camera

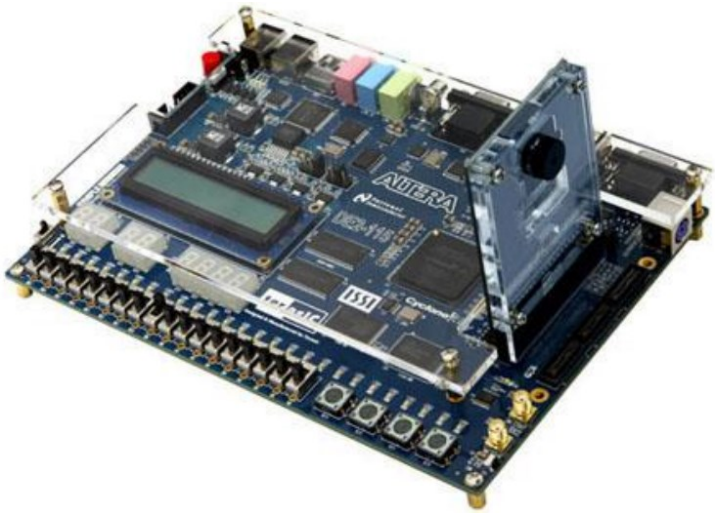
Please follow the step below to assemble your camera:

1. Connect the D5M to your DE4 board as shown in Figure 1-2.

Figure 1-2 Connect the D5M to DE4 board's expansion port (outermost port).

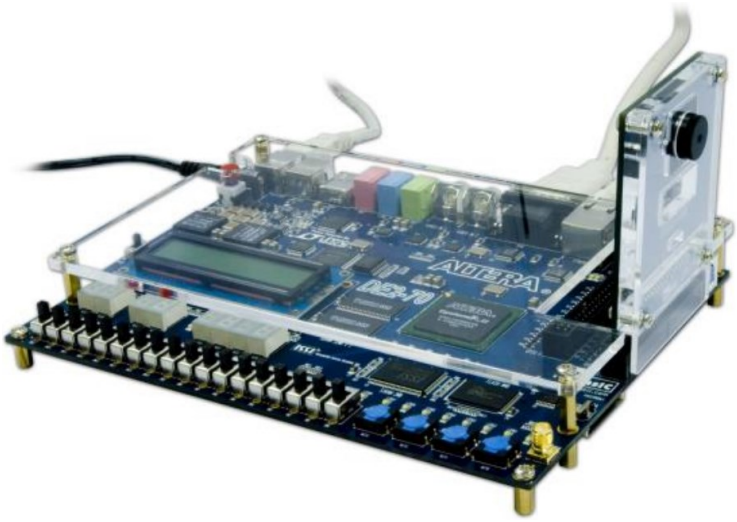
2. Connect the D5M to your DE2-115 board as shown in Figure 1-3.

Figure 1-3 Connect the D5M to DE2-115 board's expansion port



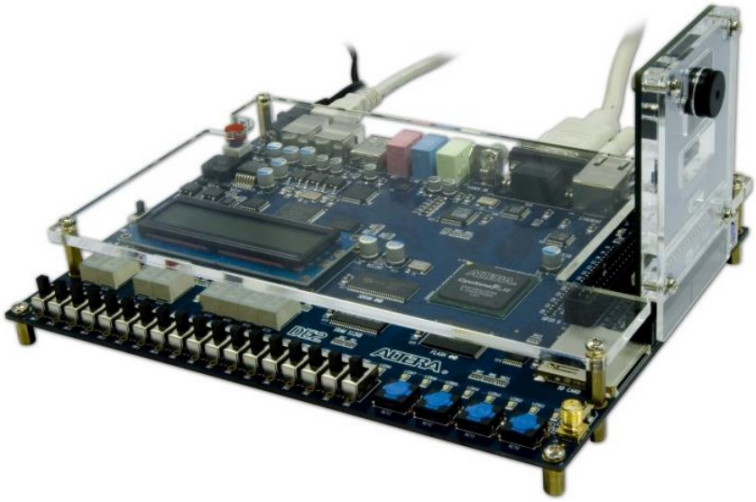
3. Connect the D5M to your DE2-70 board as shown in Figure 1-4.

Figure 1-4 Connect the D5M to DE2-70 board's expansion port (outermost port).

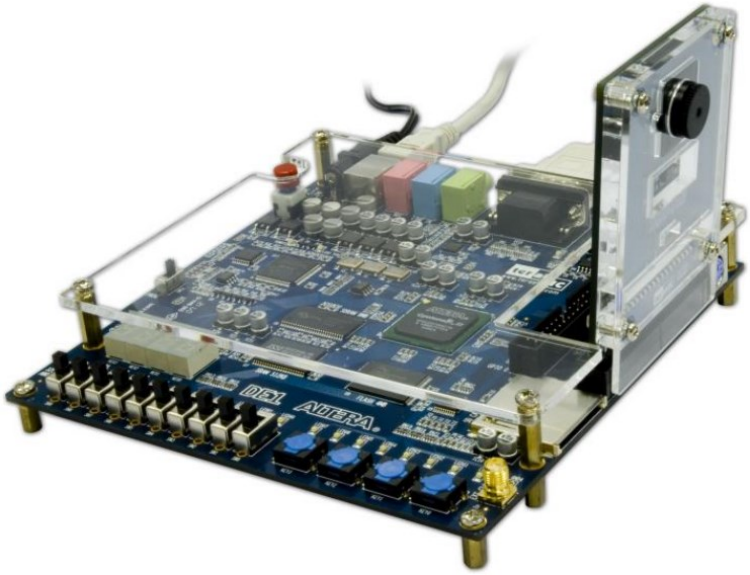


4. Connect the D5M to your DE2 board as shown in Figure 1-5.

Figure 1-5 Connect the D5M to DE2 board's expansion port (outermost port).



5. Connect the D5M to your DE1 board as shown in Figure 1-6.
   Figure 1-6 Connect the D5M to DE1 board's expansion port (outermost port).



Getting Help

Here are some places to get help if you encounter any problem:

- Email to **support@terasic.com**
- Taiwan & China: +886-3-5750-880
- Korea : +82-2-512-7661
- Japan: +81-428-77-7000
  English Support Line: +1-408-512-1336

TRDB_D5M

This chapter will illustrate the technical details users need to know to modify the reference design for their own purpose.

Features

The D5M kit is designed to use the same strict design and layout practices used in high-end consumer products. The feature set is listed below:

1. High frame rate
2. Superior low-light performance
3. Low dark current
4. Global reset release, which starts the exposure of all rows simultaneously
5. Bulb exposure mode, for arbitrary exposure times
6. Snapshot mode to take frames on demand
7. Horizontal and vertical mirror image
8. Column and row skip modes to reduce image size without reducing field-of-view
9. Column and row binning modes to improve image quality when resizing
10. Simple two-wire serial interface
11. Programmable controls: gain, frame rate, frame size, exposure
12. Automatic black level calibration
13. On-chip PLL

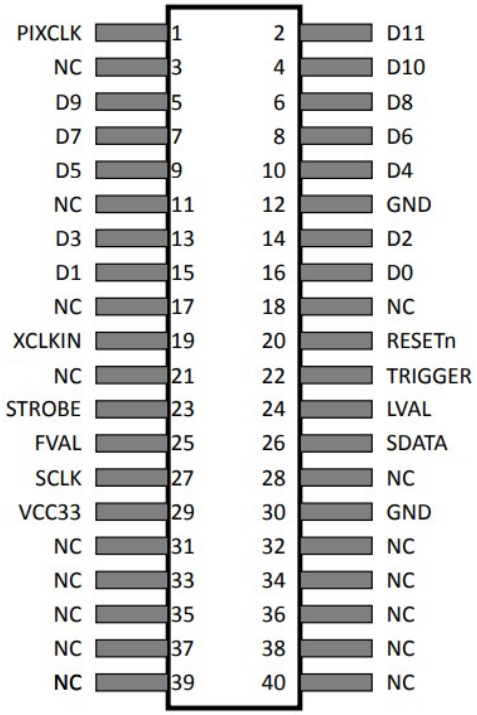
- Key Performance Parameters

Parameter		***Value***
Active pixels		2,592H x 1,944V
Pixel size		2.2µm x 2.2µm
Color filter array		RGB Bayer pattern
Shutter type		Global reset release (GRR),
Maximum data rate/master		96 Mp/s at 96 MHz
Frame rate	Full resolution	Programmable up to 15 fps
	VGA (640 x 480)	Programmable up to 70 fps
ADC resolution		12-bit
Responsivity		1.4 V/lux-sec (550nm)
Pixel dynamic range		70.1dB
SNRMAX		38.1dB
Supply Voltage	Power	3.3V
	I/O	1.7V **3.1V**

Note. For detail specification of D5M, please refer to TRDB-D5M_Hardware specification.PDF

Pin-out of the 40-pin connector on TRDB-D5M

Figure 2-1. The pin-out of the 40-pin connector on TRDB_D5M



Pin Description of the 40-pin Interface of TRDB_D5M

The TRDB_D5M has a 40-pin connector on the board. The pin description of the 40-pin connector follows

Pin Numbers	***Name***	***Direction***	***Description***
1	PIXCLK	Output	Pixel clock.
2	D[11]	Output	Pixel data Bit 11
3	NC	N/A	Not Connect
4	D[10]	Output	Pixel data Bit 10
5	D[9]	Output	Pixel data Bit 9
6	D[8]	Output	Pixel data Bit 8
7	D[7]	Output	Pixel data Bit 7
8	D[6]	Output	Pixel data Bit 6
9	D[5]	Output	Pixel data Bit 5
10	D[4]	Output	Pixel data Bit 4
11	NC	N/A	Not Connect
12	GND	N/A	Ground
13	D[3]	Output	Pixel data Bit 3
14	D[2]	Output	Pixel data Bit 2
15	D[1]	Output	Pixel data Bit 1
16	D[0]	Output	Pixel data Bit 0
17	NC	N/A	Not Connect
18	NC	N/A	Not Connect
19	XCLKIN	Input	External input clock
20	RESETn	Input	D5M reset
21	NC	N/A	Not Connect
22	TRIGGER	Input	Snapshot trigger
23	STROBE	Output	Snapshot strobe
24	LVAL	Output	Line valid
25	FVAL	Output	Frame valid
26	SDATA	I/O	Serial data
27	SCLK	Input	Serial clock
28	NC	N/A	Not Connect
29	VCC33	N/A	Power 3.3V

30	GND	N/A	Ground
31	NC	N/A	Not Connect
32	NC	N/A	Not Connect
33	NC	N/A	Not Connect
34	NC	N/A	Not Connect
35	NC	N/A	Not Connect
36	NC	N/A	Not Connect
37	NC	N/A	Not Connect
38	NC	N/A	Not Connect
39	NC	N/A	Not Connect
40	NC	N/A	Not Connect

Digital Camera Design Demonstration

This chapter illustrates how to exercise the digital camera reference design provided with the kit. Users can follow the instructions in this chapter to build a 5 Mega Pixel camera using their DE4 / DE2_115 / DE2-70 / DE2 / DE1 in minutes.

Demonstration Setup

The image raw data is sent from D5M to the DE4 / DE2_115 /DE2-70 / DE2 / DE1 board. The FPGA on the DE4 / DE2_115 /DE2-70 / DE2 / DE1 board is handling image processing part and converts the data to RGB format to display on the DVI / VGA monitor. For DE2-70, the image captured at SDRAM can be taken at anytime (snapshot) and uploaded to a PC as a BMP/JPG file.

Camera Demonstration Setup On DE4 Board

Locate the project directory from the CD-ROM included and follow the steps below:
Directory: Demonstration / DE4_230/530_D5M_DVI
FPGA Bitstream Used: DE4_230/530_ D5M_DVI.sof

1. Ensure the connection is made correctly as shown in Figure 3-1. Make sure the D5M is connected to JP4 (GPIO 1) and DVI daughter card is connected to J20 (HSMC PORT A) of the DE4 board with two THCB-HMF2 interface cards which are bundled in the DE4 kit.
2. Insert the DDR2 memory card into J9 (DDR2 SO-DIMM-1).
3. Connect the DVI TX output of the DVI daughter card to a DVI monitor.
4. Copy the directory DE4_230/530_D5M_VGA from D5M System CD-ROM to the host computer.
5. Download the bitstream (DE4_230/530_D5M_DVI.sof) to the DE4 board.
6. The system enters the FREE RUN mode automatically. Press BUTTON [0] on the DE4 board to reset the circuit.
7. User can use the SW[0] to set the DVI display mode. When SW [0] is set to Off, the DVI will display whatever the camera captures. when On, the DVI will display color pattern.
8. Press BUTTON [2] to take a shot of the photo; you can press BUTTON [3] again to switch back to FREE RUN mode and you should be able to see whatever the camera captures on the VGA display..
9. User can use the SLIDE_SW [0] with BUTTON [1] to set the exposure time for brightness adjustment of the image captured. When SLIDE_SW [0] is set to Off, the brightness of image will be increased as BUTTON [1] is pressed longer. If SLIDE_SW [0] is set to On, the brightness of image will be decreased as BUTTON [1] is pressed shorter.
10. Set the SLIDE_SW [1] to On (upper position), the captured image will be enlarged with BUTTON [0] and BUTTON [3] pressed in order.
11. Table 3-1 summarizes the functional keys of the digital camera.

Figure 3-1 The Connection Setup for DE4 users

12. User can revise the header file “vpg.h” in the project to select the system resolution between SXGA@1280*1024 and VGA@640*480 (note*).
13. After revision, regenerate the project and repeat above steps.

Note: users should revise the parameter ‘PORT_SIZE_BYTES’ of the DDR2_ODIMM_Read/Write_Port modules in SOPC Builder under each resolution (640*480*4, 1280*1024*4 respectively) .

Table 3-1 The functional keys of the digital camera demonstration

Component	***Function Description***
BUTTON [0]	Reset circuit
BUTTON [1]	Set the new exposure time (usewith SW[0])
BUTTON [2]	Trigger the Image Capture (take ashot)
BUTTON [3]	Switch to Free Run mode
SLIDE_SW [0]	Off: Extend the exposure timeOn: Shorten the exposure tim e
SLIDE_SW [1]	On: ZOOM inOff: Normal display
SW [0]	On: Color pattern display Off: Normal display
HEX[1:0]	Frame counter (Display the low 8bits ONLY)

Camera Demonstration Setup On DE2-115 Boar

Locate the project directory from the CD-ROM included and follow the steps below:
Directory: Demonstration / DE2_115_CAMERA
FPGA Bitstream Used: DE2_115_ CAMERA.sof

1. Ensure the GPIO voltage level is set to 3.3V via JP6 (GPIO_VCCIO) of the DE2-115 board.
2. Ensure the connection is made correctly as shown in Figure 3-2. Make sure the D5M is connected to JP5 (GPIO) of the DE2-115 board.
3. Connect the VGA output of the DE2-115 board to a VGA monitor.
4. Copy the directory DE2_115_D5M_VGA from D5M System CD-ROM to the host computer.
5. Download the bitstream (DE2_115_D5M_VGA.sof/pof) to the DE2_115 board.

6. The system enters the FREE RUN mode automatically. Press KEY[0] on the DE2-115 board to reset the circuit.
7. Press KEY[2] to take a shot of the photo; you can press KEY[3] again to switch back to FREE RUN mode and you should be able to see whatever the camera captures on the VGA display..
8. User can use the SW[0] with KEY[1] to set the exposure time for brightness adjustment of the image captured. When SW[0] is set to Off, the brightness of image will be increased as KEY[1] is pressed longer. If SW[0] is set to On, the brightness of image will be decreased as KEY[1] is pressed shorter.
9. Set the SW[16] to On (upper position), the captured image will be enlarged by pressing KEY[0].
10. Table 3-2 summarizes the functional keys of the digital camera.

Figure 3-2 The Connection Setup for DE2-115 users

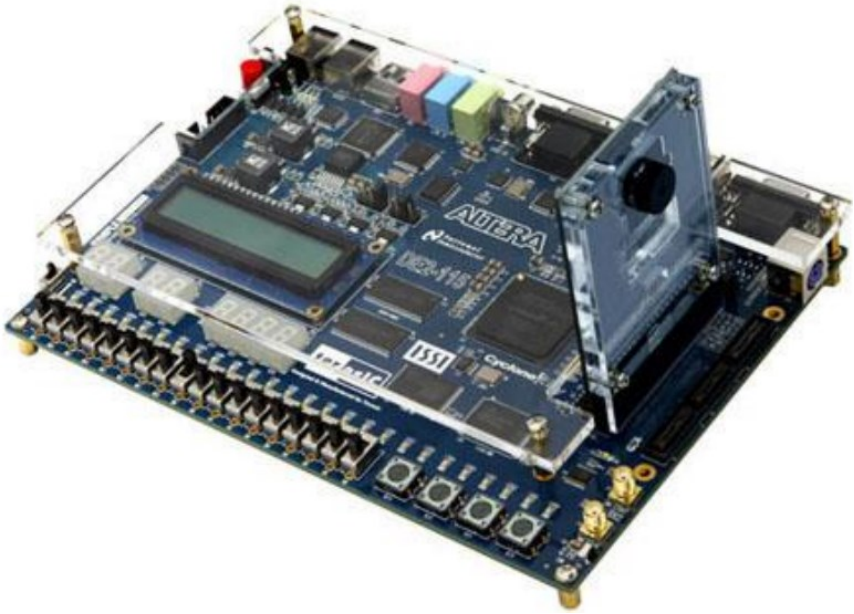


Table 3-2 The functional keys of the digital camera demonstration

Component	***Function Description***
KEY[0]	Reset circuit
KEY[1]	Set the new exposure time (use with SW[0])
KEY[2]	Trigger the Image Capture (take a shot)
KEY[3]	Switch to Free Run mode
SW[0]	Off: Extend the exposure timeOn: Shorten the exposure time
SW[16]	On: ZOOM inOff: Normal display
HEX[7:0]	Frame counter (Display ONLY)

11. User can revise the header file “VGA_Param.h” in the project to select the system resolution between SVGA@800*600 and VGA@640*480.
12. After revision, regenerate the project and repeat above steps.

Configuring the Camera and Load the Image Captured to Your PC (DE2-70 Board Users)

Locate the project directory from the CD-ROM included and follow the steps below:
Directory: Demonstration / DE2_70_CAMERA / SW
FPGA Bitstream Used: DE2_70_ CAMERA.sof

1. Ensure the connection is made correctly as shown in Figure 3-3. Make sure the D5M is connected to J5 (GPIO 1) of the DE2-70 board.
2. Copy the directory DE2_70_CAMERA from D5M System CD-ROM to the host computer.
3. Execute the DE2_70_CAMERA.exe form the directory DE2_70_CAMERA / SW.
4. Click the 'Download Code' button. (Error message will pop up for warning since the DE2-70 is loaded with factory default image, which cannot be transmitted. Click 'OK' button to skip the error message and click 'Download Code' to proceed.
5. Connect the VGA output of the DE2-70 board to a VGA monitor.
6. Press KEY0 on the DE2-70 board to reset the circuit.
7. You can press KEY3 to switch to the FREE RUN mode and you should be able to see whatever the camera captures on the VGA display.
8. Press KEY2 to take a shot of the photo; you can press KEY3 again to switch back to FREE RUN mode.
9. Users can use the SW[0] with KEY1 to set the exposure time for brightness adjustment of the image captured. When SW[0] is set to Off, the brightness of image will be increased as KEY1 is pressed longer. If SW[0] is set to On, the brightness of image will be decreased as KEY1 is pressed shorter.
10. Set the SW[16] to On (upper position), the captured image will be enlarged with KEY0 and KEY3 pressed in order.
11. Table 3-3 summarizes the functional keys of the digital camera

Figure 3-3 The Connection Setup for DE2-70 users

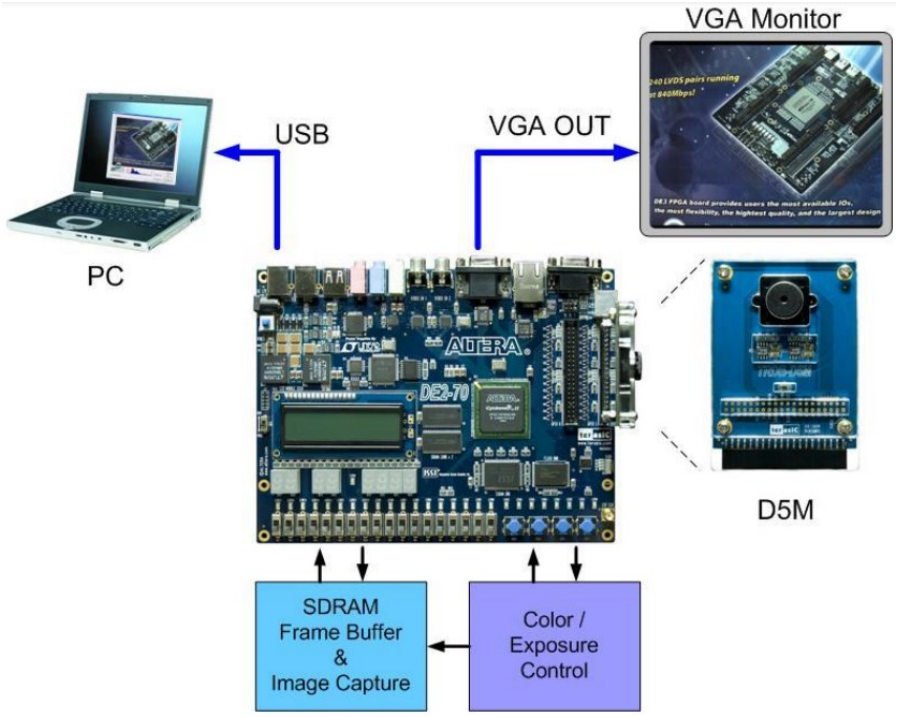
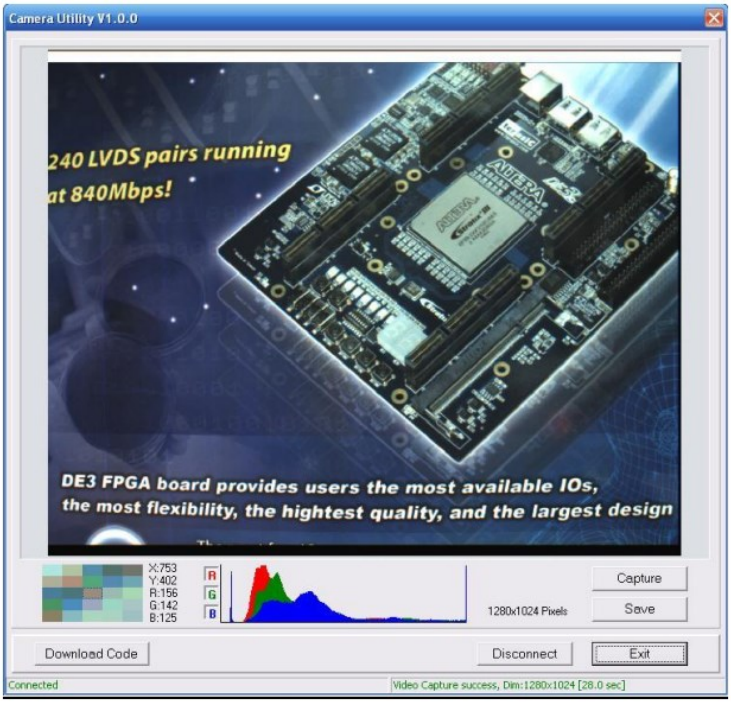


Table 3-3 The functional keys of the digital camera demonstration

Component	***Function Description***
KEY[0]	Reset circuit
KEY[1]	Set the new exposure time (use with SW[0])
KEY[2]	Trigger the Image Capture (take a shot)
KEY[3]	Switch to Free Run mode
SW[0]	Off: Extend the exposure timeOn: Shorten the exposure time
SW[16]	On: ZOOM inOff: Normal display
HEX[7:0]	Frame counter (Display ONLY)

12. Users can upload the captured image to PC by clicking the ‘Capture’ button of the ‘DE2_70_CAMERA.exe’ as shown in Figure 3-4. Meanwhile, the digital camera is set to photo-taking mode. Press KEY3 to switch back to FREE RUN mode.
13. Click ‘Save’ button to save the captured image as a JPG or BMP file

Figure 3-4 The DE2_70_camera tool



Configuring the Camera (DE2 Board Use

Locate the project directory from the CD-ROM included and follow the steps below:
Directory: Demonstration / DE2_CAMERA
FPGA Bitstream Used: DE2_D5M.sof or DE2_D5M.pof

1. Ensure the connection is set correctly as shown in Figure 3-5. Make sure the D5M is connected to JP2 (GPIO 1) of the DE2 board.
2. Connect the VGA output of the DE2 board to a VGA monitor.
3. Download the bitstream (DE2_D5M.sof/pof) to the DE2 board.
4. Press KEY0 on the DE2 board to reset the circuit.
5. You can press KEY3 to switch to the FREE RUN mode and you should be able to see whatever the camera sees on the VGA display.
6. Press KEY2 to take a shot of the photo; you can press KEY3 again to switch back to FREE RUN mode.
7. Users can use the SW[0] with KEY1 to set the exposure time for brightness adjustment of the image captured. When SW[0] is set to Off, the brightness of image will be increased as KEY1 is pressed longer. If SW[0] is set to On, the brightness of image will be decreased as KEY1 is pressed shorter.
8. Set the SW[16] to On (upper position), the captured image will be enlarged with KEY0 and KEY3 pressed in

order.

9. Table 3-4 summarizes the functional keys of the digital camera **Figure 3-5 The Connection Setup for DE2 users**

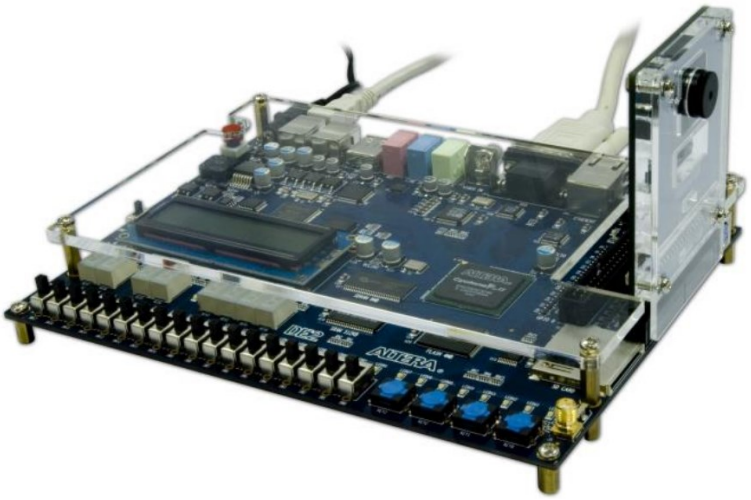


Table 3-4 The functional keys of the digital camera demonstration

Component	***Function Description***
KEY[0]	Reset circuit
KEY[1]	Set the new exposure time (use with SW[0])
KEY[2]	Trigger the Image Capture (take a shot)
KEY[3]	Switch to Free Run mode
SW[0]	Off: Extend the exposure timeOn: Shorten the exposure time
SW[16]	On: ZOOM inOff: Normal display
HEX[7:0]	Frame counter (Display ONLY)

Configuring the Camera (DE1 Board Users)

Locate the project directory from the CD-ROM included and follow the steps below:
Directory: Demonstration / DE1_CAMERA
FPGA Bitstream Used: DE1_D5M.sof or DE1_D5M.pof

1. Ensure the connection is set correctly as shown in Figure 3-6. Make sure the D5M is connected to JP2 (GPIO 1) of the DE1 board.
2. Download the bitstream (DE1_D5M.sof/pof) to the DE1 board.
3. Connect the VGA output of the DE1 board to a VGA monitor
4. Press KEY0 on the DE1 board to reset the circuit.
5. You can press KEY3 to switch to the FREE RUN mode and you should be able to see whatever the camera sees on the VGA display.
6. Press KEY2 to take a shot of the photo; you can press KEY3 again to switch back to FREE RUN mode.
7. Users can use the SW[0] with KEY1 to set the exposure time for brightness adjustment of the image captured. When SW[0] is set to Off, the brightness of image will be increased as KEY1 is pressed longer. If SW[0] is set to On, the brightness of image will be decreased as KEY1 is pressed shorter.
8. Set the SW[8] to On (upper position), the captured image will be enlarged with KEY0 and KEY3 pressed in order.
9. Table 3-5 summarizes the functional keys of the digital camera.

Figure 3-6 The Connection Setup for DE1 users

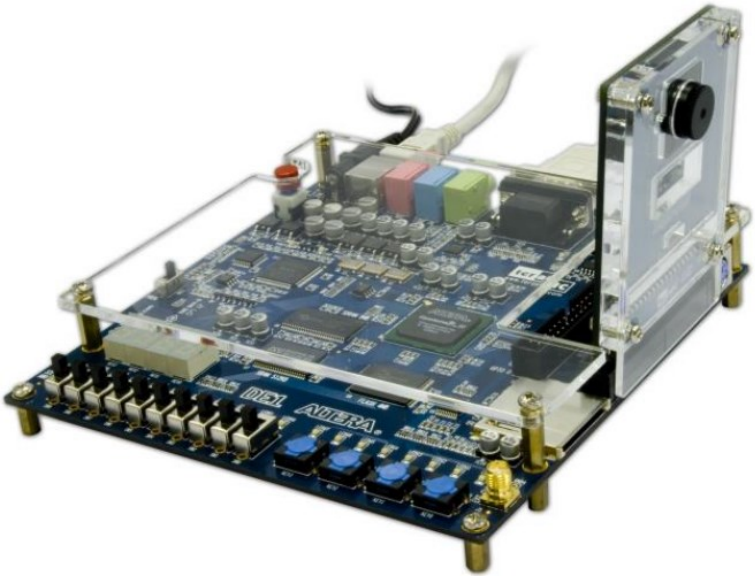


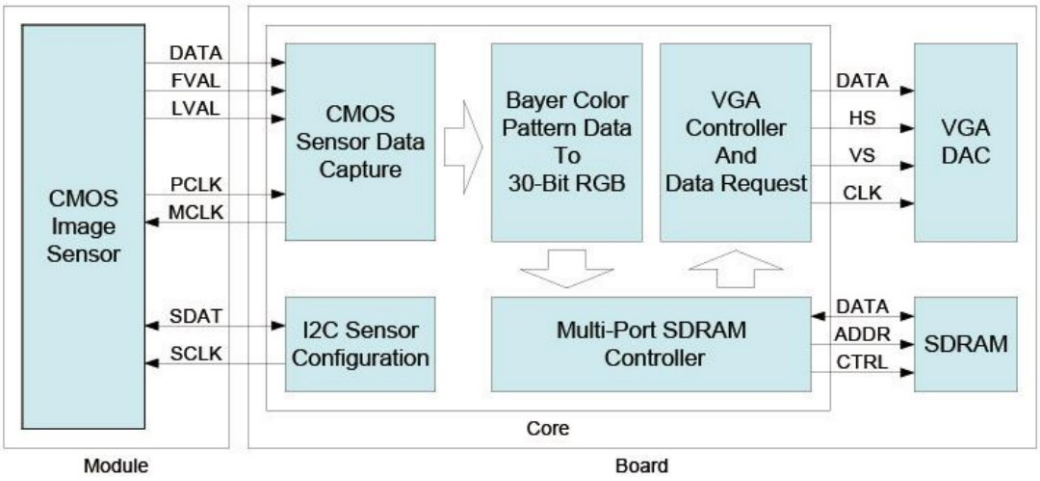
Table 3-5 The functional keys of the digital camera demonstration

Component	Function Description
KEY[0]	Reset circuit
KEY[1]	Set the new exposure time (use with SW[0])
KEY[2]	Trigger the Image Capture (take a shot)
KEY[3]	Switch to Free Run mode
SW[0]	Off: Extend the exposure timeOn: Shorten the exposure time
SW[8]	On: ZOOM inOff: Normal display
HEX[3:0]	Frame counter (Display ONLY)

Block Diagram of the Reference Design

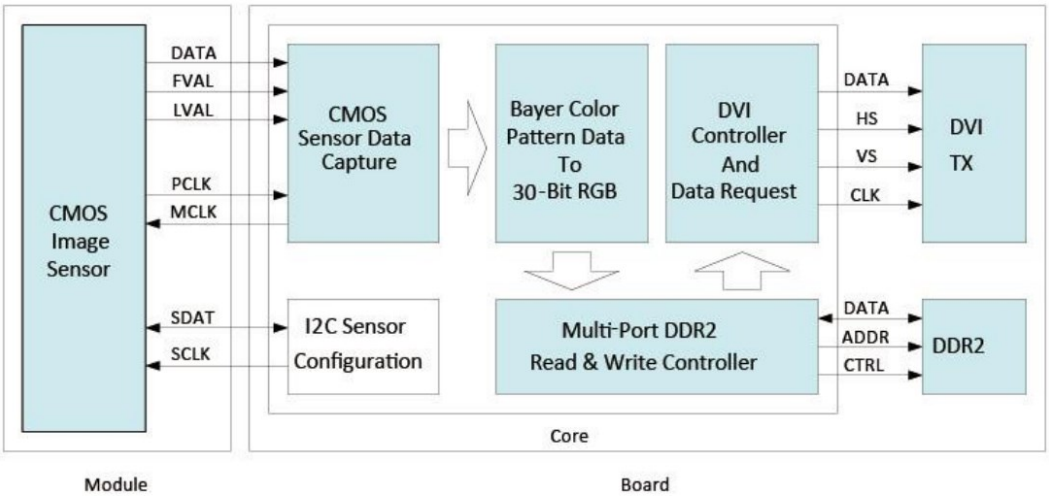
The complete reference design is also located in the CD-ROM attached. Please refer to the following diagram to help you in reading the code provided.

Figure 3-7 The block diagram of the digital camera design



The below figure for DE4 only.

Figure 3-8 The block diagram of the digital camera design for DE4



Appendix

Revision History

Date	Change Log
MAR, 24, 2008	Initial Version (Preliminary)
AUG, 03, 2009	revised
AUG, 10, 2010	D5M on DE4 and DE2-115 Board Added
June, 13, 2017	Modify DE2-115 demo

Always Visit TRDB_D5M Webpage for New

Applications

We will be continuing providing interesting examples and labs on our TRDB_D5M webpage.
Please visit **www.altera.com** or **d5m.terasic.com** for more information.

Documents / Resources

	terasic TRDB-D5M Digital Camera Development Kit [pdf] User Manual TRDB-D5M Digital Camera Development Kit, TRDB-D5M, Digital Camera Development Kit, Camera Development Kit, Development Kit

References

- Terasic - Phased Out - Daughter Cards - 5 Mega Pixel Digital Camera Package
- Intel® FPGAs and Programmable Devices-Intel® FPGA
- Terasic Inc. - Expertise in FPGA/ASIC Design