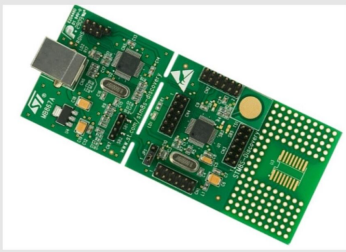
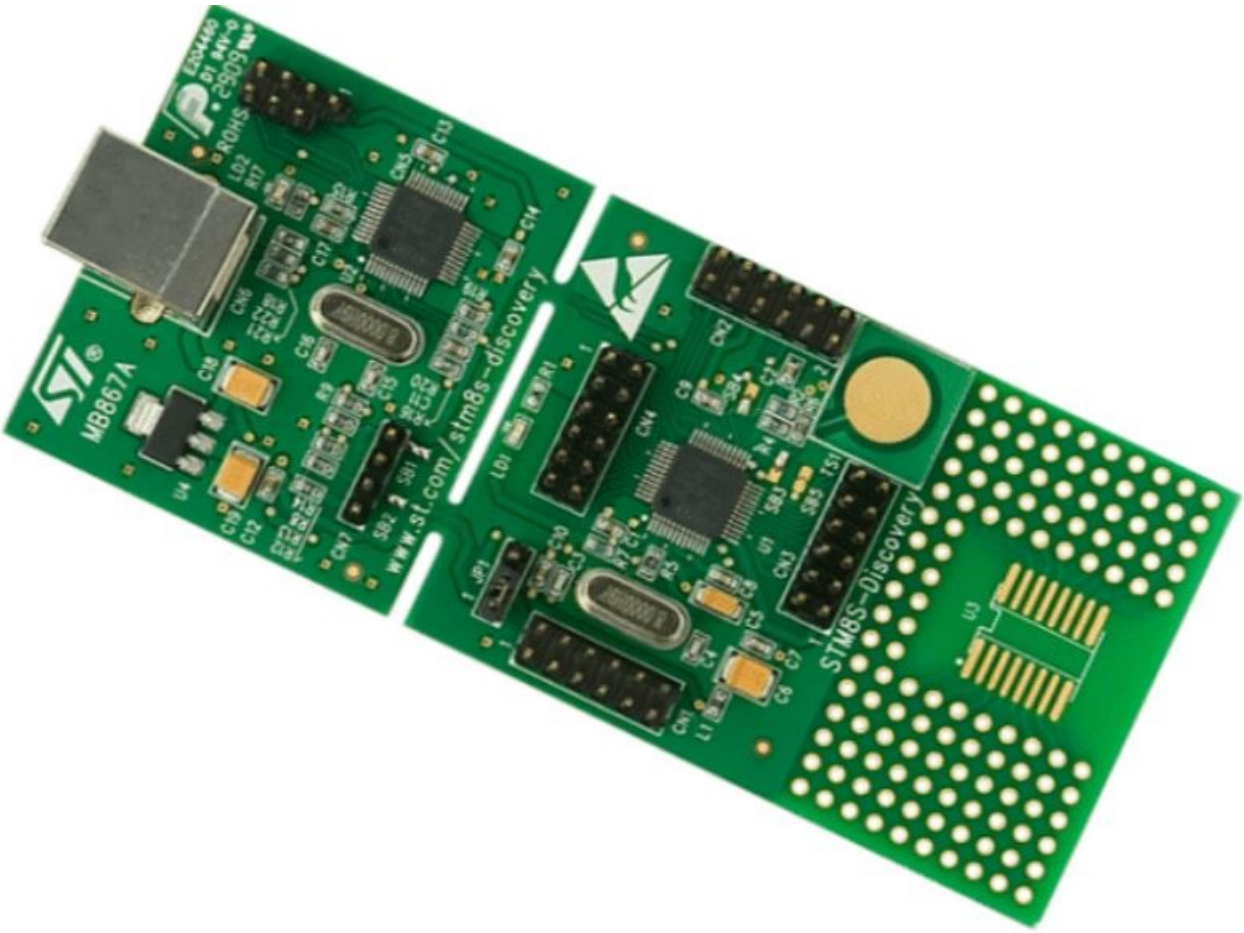


STMicroelectronics TN1317 Self Test Configuration for SPC58xNx Device User Manual

Contents

STMicroelectronics TN1317 Self Test Configuration for SPC58xNx Device



Introduction

This document provides the guidelines about how to configure the self-test control unit (STCU2) and start the self-test execution. The STCU2 on SPC58xNx device manages both Memory and Logic Built-In Self Test (MBIST and LBIST) of the device. The MBISTs and LBISTs can detect latent failures which affect the volatile memories and the logic modules. The reader should have a clear understanding of the usage of self-test. See Section Appendix A for Acronyms, abbreviations and reference documents for additional details.

Overview

- The SPC58xNx supports both the MBIST and LBIST.
- The SPC58xNx includes:
  - 92 memory cuts (from 0 to 91)
  - LBIST0 (the safety LBIST)
  - 6 LBIST for diagnostic(1) (from 1 to 6)

LBIST

LBIST for diagnostic should run when the vehicle is in the garage and not while the safety application is running. The reader can consult the complete list in the chapter 7 (Device configuration) of the RM0421 SPC58xNx reference manual.

Self-test configuration

Self-test can run either in online or offline mode.

MBIST configuration

- To reach the best trade-off in terms of consumption and execution time, we recommend dividing the MBISTs into 11 splits. The MBIST partitions belonging to the same split run in parallel.
- The 11 splits run in sequential mode. For example:
- all MBIST partitions belonging to the split_0 start in parallel;
- after their execution, all MBIST partitions belonging to the split_1 start in parallel;
- and so forth.
- The complete list of the splits and MBISTs is shown in the split and DCF Microsoft Excel® workbook attached files.

LBIST configuration

- In offline mode, generally only the LBIST0 runs, that is the safey bist (to guarantee the ASIL D). It's the first BIST in the self test configuration (pointer 0 in the LBIST_CTRL register).
- In online mode the user can choose to run the other LBISTs (from 1 to 6) for diagnostic use. They include:
  - LBIST1: gtm
  - LBIST2: hsm, sent, emios0, psi5, dspi
  - LBIST3: can1, flexray_0, memu, emios1, psi5_0, fccu, ethernet1, adcsd_ana_x, crc_0, crc_1, fosu, cmu_x, bam, adcsd_ana_x
  - LBIST4: psi5_1, ethernet0,adcsar_dig_x, adcsar_dig_x, iic, dspi_x, adcsar_seq_x, adcsar_seq_x, linlfex_x, pit, ima, cmu_x, adgsar_ana_wrap_x
  - LBIST5: platform
  - LBIST6: can0, dma

DCF list for offline configuration

MBISTs and LBIST0 can run in offline up to 100 MHz as max frequency. The DCF Microsoft Excel® workbook attached file reports the list of the DCF to be configured in order to start up the MBIST and LBIST during the boot phase (offline mode). They take around 42 ms.

Monitors during self-test

- Two different phases impact the self-test execution (See RM0421 SPC58xNx reference manual).
- Initialization (configuration loading). The SSCM (offline mode) or the software (online mode) configures the BISTs by programming the STCU2.
- Self-test execution. The STCU2 executes self-test.
- Two different watchdogs monitor these phases.
- Hard-coded watchdog monitors the "initialization" phase. It is a hardware watchdog configured at 0x3FF.
- The user cannot modify it. The clock of the hard-coded watchdog depends on the operating mode:
  - IRC oscillator in offline mode
  - STCU2 clock in online mode
- Watchdog timer (WDG) monitors the "self-test execution". It is a hardware watchdog configurable by the user (STCU_WDG register). The user can check the status of the "STCU WDG" after the BIST execution in the STCU_ERR_STAT register (WDTO flag).

The clock of “STCU WDG” depends on the operating mode:

- It is configurable by the STCU_PLL (IRC or PLL0) in offline mode;
- It is configurable by software in online mode.

Hard-coded watchdog refresh during initialization

The hard-coded watchdog timeout is 0x3FF clock cycles. The SSCM or the software must periodically refresh the hard-coded watchdog by programming the STCU2 key2. To perform this operation, the user must interleave the list of DCF records (offline mode) or the writing accesses to the STCU2 registers (online mode) with a write to the STCU2 key2 register. In the case of offline BIST, a single write of a DCF record takes around 17 clock cycles. Since the hard-coded watchdog expires after 1024 clock cycles, the user must refresh it every 60 DCF records. Note: The watchdog expires after 1024 clock cycles. A single DCF write takes 17 clock cycles. The STCU2 accepts up to 60 DCF records before the hard-watchdog expires (1024/17 = 60). In the case of online BIST, the refresh time (STCU2 key2 writing) is application dependent.

Online mode configuration

In online mode the MBIST split list remains the same with some limitations due to life cycle. All MBISTs can run in online mode only in ST production and failure analysis (FA). In the other life cycles, HSM/MBIST and Flash MBIST are not accessible. In this case, the maximum frequency for MBIST is 200 MHz and is provided by the sys_clock. The LBIST for diagnostic can run up to 50 MHz, while LBIST 0 can run up to 100 MHz. In that case, STCU2 registers can be configured with the “register value” column of the DCF list file.

Summary
In SPC58xNx both MBIST and LBIST can run. During offline, LBIST0 and all MBISTs can run according to the split configuration. During online mode, the LBIST for diagnostic can run as well.

Appendix A Acronyms, abbreviations and reference documents

Acronyms

Acronym	Name
MBIST	Memory Built-In Self Test
LBIST	Logic Built-In Self Test
STCU2	Self-test control unit
HSM	Hardware system module
LC	Life cycle
DCF	Device configuration format (DCF) records
UTest	User test flash block
FA	Failure analysis

Reference documents

Document name	Document title
RM0421	SPC58xNx 32-bit Power Architecture microcontroller for automotive ASILD applications
AN4551	SPC574K72xx self-test procedures

Document revision history

Date	Revision	Changes
30-Jun-2020	1	Initial release.
25-Feb-2022	2	Added Section 2.4 Monitors during self-test and Section 2.4.1 Hard-coded watchdog refresh during initialization. Updated split and DCF Microsoft Excel® workbook attached files. Replaced *Other information* chapter with Section Appendix A Acronyms, abbreviations and reference documents. Minor text changes.

Documents / Resources

	STMicroelectronics TN1317 Self Test Configuration for SPC58xNx Device [pdf] User Manual TN1317, Self Test Configuration for SPC58xNx Device, Configuration for SPC58xNx Device, Self Test Configuration, TN1317, Self Test

References

- STMicroelectronics: Our technology starts with you
- STMicroelectronics Trademark List - STMicroelectronics