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STMicroelectronics ST92F120 Embedded Applications Instructions

Contents

STMicroelectronics ST92F120 Embedded Applications

INTRODUCTION

Microcontrollers for embedded applications tend to integrate more and more peripherals as well as larger memories. Providing the right products with the right features such as Flash, emulated EEPROM and a wide range of peripherals at the right cost is always a challenge. That is why it is mandatory to shrink the microcontroller die size regularly as soon as the technology will allow it. This major step applies to the ST92F120. The purpose of this document is to present the differences between the ST92F120 microcontroller in 0.50-micron technology versus the ST92F124/F150/F250 in 0.35-micron technology. It provides some guidelines for upgrading applications for both its software and hardware aspects.

In the first part of this document, the differences between the ST92F120 and ST92F124/F150/F250 devices are listed. In the second part, the modifications required for the application hardware and software are described.

UPGRADING FROM THE ST92F120 TO THE ST92F124/F150/F250

ST92F124/F150/F250 microcontrollers using 0.35 micron technology are similar to ST92F120 microcontrollers using 0.50 micron technology, but shrinking is used to add some new fea-tures and to improve the performances of ST92F124/F150/F250 devices. Almost all periph-erals keep the same features, which is why this document focuses only on the modified sec-tions. If there is no difference between the 0.50 micron peripheral compared to the 0.35 one, other than its technology and design methodology, the peripheral is not presented. The new analog to digital converter (ADC) is the major change. This ADC uses a single 16 channel A/D converter with 10 bits resolution instead of two 8-channel A/D converters with 8-bit resolu-tion. The new memory organization, new reset and clock control unit, internal voltage regula-tors and new I/O buffers will almost be transparent changes for the application. The new pe-ripherals are the Controller Area Network (CAN) and the asynchronous Serial Communication Interface (SCI-A).

PINOUT

The ST92F124/F150/F250 was designed in order to be able to replace the ST92F120. Thus, pinouts are nearly the same. The few differences are described below:

- Clock2 was remapped from port P9.6 to P4.1
- Analog input channels were remapped according to the table below.

Table 1. Analog Input Channel Mapping

PIN	ST92F120 Pinout	ST92F124/F150/F250 Pinout
P8.7	A1IN0	AIN7
…	…	…
P8.0	A1IN7	AIN0
P7.7	A0IN7	AIN15
…	…	…
P7.0	A0IN0	AIN8

- RXCLK1(P9.3), TXCLK1/ CLKOUT1 (P9.2), DCD1 (P9.3), RTS1 (P9.5) were removed because SCI1 was replaced by SCI-A.
- A21(P9.7) down to A16 (P9.2) were added in order to be able to address up to 22 bits externally.
- 2 new CAN peripheral devices are available: TX0 and RX0 (CAN0) on ports P5.0 and P5.1 and TX1 and RX1 (CAN1) on dedicated pins.

RW RESET STATE
Under Reset state, RW is held high with an internal weak pull-up whereas it was not on the ST92F120.

SCHMITT TRIGGERS

- I/O ports with Special Schmitt Triggers are no longer present on the ST92F124/F150/F250 but are replaced by I/O ports with High Hysteresis Schmitt Triggers. The related I/O pins are: P6[5-4].
- Differences on the VIL and VIH. See Table 2.

Table 2. Input Level Schmitt Trigger DC Electrical Characteristics
(VDD = 5 V ± 10%, TA = –40° C to +125° C, unless otherwise specified)

Symbol	Parameter	Device	Value Min	Typ(1)	Max	Unit
VIH	Input High Level Standard Schmitt Trigger P2[5:4]-P2[1:0]-P3[7:4]-P3[2:0]- P4[4:3]-P4[1:0]-P5[7:4]-P5[2:0]- P6[3:0]-P6[7:6]-P7[7:0]-P8[7:0]- P9[7:0]	ST92F120	0.7 x VDD			V
		ST92F124/F150/F250	0.6 x VDD			V
VIL	Input Low Level Standard Schmitt Trigger P2[5:4]-P2[1:0]-P3[7:4] P3[2:0]- P4[4:3]-P4[1:0]-P5[7:4]-P5[2:0]- P6[3:0]-P6[7:6]-P7[7:0]-P8[7:0]- P9[7:0]	ST92F120			0.8	V
		ST92F124/F150/F250			0.2 x VDD	V
	Input Low Level High Hyst.Schmitt Trigger P4[7:6]-P6[5:4]	ST92F120			0.3 x VDD	V
		ST92F124/F150/F250			0.25 x VDD	V
VHYS	Input Hysteresis Standard Schmitt Trigger P2[5:4]-P2[1:0]-P3[7:4]-P3[2:0]- P4[4:3]-P4[1:0]-P5[7:4]-P5[2:0]- P6[3:0]-P6[7:6]-P7[7:0]-P8[7:0]- P9[7:0]	ST92F120		600		mV
		ST92F124/F150/F250		250		mV
	Input Hysteresis High Hyst. Schmitt Trigger P4[7:6]	ST92F120		800		mV
		ST92F124/F150/F250		1000		mV
	Input Hysteresis High Hyst. Schmitt Trigger P6[5:4]	ST92F120		900		mV
		ST92F124/F150/F250		1000		mV

Unless otherwise stated, typical data are based on TA= 25°C and VDD= 5V. They are only reported for design guide lines not tested in production.

MEMORY ORGANIZATION

External memory
On the ST92F120, only 16 bits were externally available. Now, on the ST92F124/F150/F250 device, the 22 bits of the MMU are externally available. This organization is used to make it easier to address up to 4 external Mbytes. But segments 0h to 3h and 20h to 23h are not ex-ternally available.

Flash Sector Organization
Sectors F0 to F3 have a new organization in the 128K and 60K Flash devices as shown in Table 5 and Table 6. Table 3. and Table 4 show the previous organization.

Table 3. Memory Structure for 128K Flash ST92F120 Flash Device

Sector	Addresses	Max Size
TestFlash (TF) (Reserved)	230000h to 231F7Fh	8064 bytes
OTP Area	231F80h to 231FFBh	124 bytes
Protection Registers (reserved)	231FFCh to 231FFFh	4 bytes
Flash 0 (F0)	000000h to 00FFFFh	64 Kbytes
Flash 1 (F1)	010000h to 01BFFFh	48 Kbytes
Flash 2 (F2)	01C000h to 01DFFFh	8 Kbytes
Flash 3 (F3)	01E000h to 01FFFFh	8 Kbytes
EEPROM 0 (E0)	228000h to 228FFFh	4 Kbytes
EEPROM 1 (E1)	22C000h to 22CFFFh	4 Kbytes
Emulated EEPROM	220000h to 2203FFh	1 Kbyte

Table 4. Memory Structure for 60K Flash ST92F120 Flash Device

Sector	Addresses	Max Size
TestFlash (TF) (Reserved)	230000h to 231F7Fh	8064 bytes
OTP Area	231F80h to 231FFBh	124 bytes
Protection Registers (reserved)	231FFCh to 231FFFh	4 bytes
Flash 0 (F0) Reserved Flash 1 (F1) Flash 2 (F2)	000000h to 000FFFh	4 Kbytes
	001000h to 00FFFFh	60 Kbytes
	010000h to 01BFFFh	48 Kbytes
	01C000h to 01DFFFh	8 Kbytes
EEPROM 0 (E0)	228000h to 228FFFh	4 Kbytes
EEPROM 1 (E1)	22C000h to 22CFFFh	4 Kbytes 1Kbyte
Emulated EEPROM	220000h to 2203FFh	

Sector	Addresses	Max Size
TestFlash (TF) (Reserved) OTP Area Protection Registers (reserved)	230000h to 231F7Fh	8064 bytes
	231F80h to 231FFBh	124 bytes
	231FFCh to 231FFFh	4 bytes
Flash 0 (F0)	000000h to 001FFFh	8 Kbytes
Flash 1 (F1)	002000h to 003FFFh	8 Kbytes
Flash 2 (F2)	004000h to 00FFFFh	48 Kbytes
Flash 3 (F3)	010000h to 01FFFFh	64 Kbytes

Sector	Addresses	Max Size
Hardware Emulated EEPROM sec-		
tors	228000h to 22CFFFh	8 Kbytes
(reserved)		
Emulated EEPROM	220000h to 2203FFh	1 Kbyte

Sector	Addresses	Max Size
TestFlash (TF) (Reserved)	230000h to 231F7Fh	8064 bytes
OTP Area	231F80h to 231FFBh	124 bytes
Protection Registers (reserved)	231FFCh to 231FFFh	4 bytes
Flash 0 (F0)	000000h to 001FFFh	8 Kbytes
Flash 1 (F1)	002000h to 003FFFh	8 Kbytes
Flash 2 (F2)	004000h to 00BFFFh	32 Kbytes
Flash 3 (F3)	010000h to 013FFFh	16 Kbytes
Hardware Emulated EEPROM sec- tors (reserved)	228000h to 22CFFFh	8 Kbytes
Emulated EEPROM	220000h to 2203FFh	1 Kbyte

Since the user reset vector location is set at address 0x000000, the application can use sector F0 as an 8-Kbyte user bootloader area, or sectors F0 and F1 as a 16-Kbyte area.

Flash & E3PROM Control Register Location
In order to save a data pointer register (DPR), the Flash and E3PROM (Emulated E2PROM) control registers are remapped from page 0x89 to page 0x88 where the E3PROM area is lo-cated. This way, only one DPR is used to point to both the E3PROM variables and Flash & E2PROM control registers. But the registers are still accessible at the previous address. The new register addresses are:

- FCR 0x221000 & 0x224000
- ECR 0x221001 & 0x224001
- FESR0 0x221002 & 0x224002
- FESR1 0x221003 & 0x224003

  In the application, these register locations are usually defined in the linker script file.

RESET AND CLOCK CONTROL UNIT (RCCU)
Oscillator

A new low power oscillator is implemented with the following target specifications:

- Max. 200 µamp. consumption in Running mode,
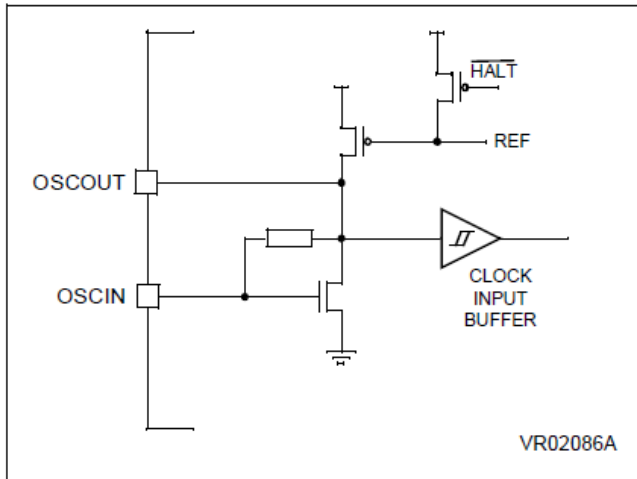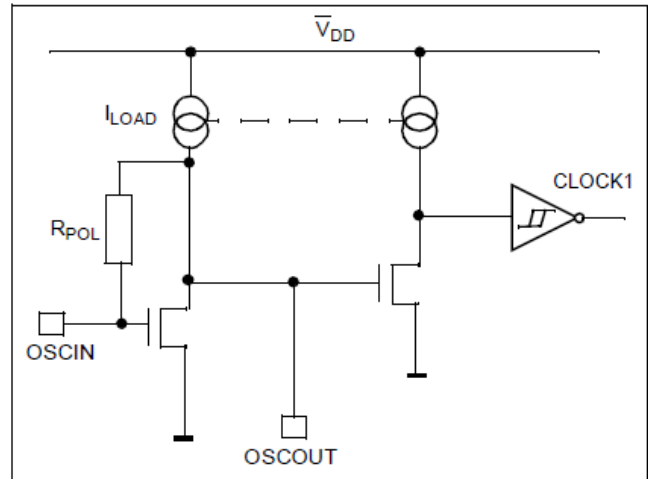- 0 amp. in Halt mode,

Figure 1. ST92F120 Internal Oscillator

Figure 2. ST92F124/F150/F250 Internal Oscillator

PLL

One bit (bit7 FREEN) has been added to the PLLCONF register (R246, page 55), this is to en-able Free Running mode. The reset value for this register is 0x07. When the FREEN bit is reset, it has the same behaviour as in the ST92F120, meaning that the PLL is turned off when:

- entering stop mode,
- DX(2:0) = 111 in the PLLCONF register,
- entering low power modes (Wait For Interrupt or Low Power Wait for Interrupt) following the WFI instruction.

When the FREEN bit is set and any of the conditions listed above occur, the PLL enters Free Running mode, and oscillates at a low frequency which is typically about 50 kHz.

In addition, when the PLL provides the internal clock, if the clock signal disappears (for in-stance due to a broken or disconnected resonator…), a safety clock signal is automatically provided, allowing the ST9 to perform some rescue operations.

The frequency of this clock signal depends on the DX[0..2] bits of the PLLCONF register (R246, page55).

Refer to the ST92F124/F150/F250 datasheet for more details.

INTERNAL VOLTAGE REGULATOR

In the ST92F124/F150/F250, the core operates at 3.3V, while the I/Os still operate at 5V. In order to supply the 3.3V power to the core, an internal regulator has been added.

Actually, this voltage regulator consists of 2 regulators:

- a main voltage regulator (VR),
- a low power voltage regulator (LPVR).

The main voltage regulator (VR) supplies the current required by the device in all operating modes. The voltage regulator (VR) is stabilized by adding an external capacitor (300 nF min-imum) on one of the two Vreg pins. These Vreg pins are not able to drive other external de-vices, and are only used for regulating the internal core power supply.

The low power voltage regulator (LPVR) generates a non-stabilized voltage of approximately VDD/2, with minimum internal static dissipation. The output current is limited, so it is not suffi-cient for full device operation mode. It provides reduced power consumption when the chip is in Low Power mode (Wait For Interrupt, Low Power Wait For Interrupt, Stop or Halt modes).

When the VR is active, the LPVR is automatically deactivated.

EXTENDED FUNCTION TIMER

The hardware modifications in the Extended Function Timer of the ST92F124/F150/F250 as compared to the ST92F120 only concern the interrupt generation functions. But some specific information has been added to the documentation concerning Forced Compare mode and One Pulse mode. This information may be found in the updated ST92F124/F150/F250 Datasheet.

Input Capture/Output Compare
On the ST92F124/F150/F250, the IC1 and IC2 (OC1 and OC2) interrupts can be enabled separately. This is done using 4 new bits in the CR3 register:

- IC1IE=CR3[7]: Input Capture 1 Interrupt Enable. If reset, Input Capture 1 interrupt is inhibit-ed. When set, an interrupt is generated if the ICF1 flag is set.
- OC1IE=CR3[6]: Output Compare 1 Interrupt Enable. When reset, Output Compare 1 interrupt is inhibited. When set, an interrupt is generated if the OCF2 flag is set.
- IC2IE=CR3[5]: Input Capture 2 Interrupt Enable. When reset, Input Capture 2 interrupt is inhibited. When set, an interrupt is generated if the ICF2 flag is set.
- OC2IE=CR3[4]: Output Compare 2 Interrupt Enable. When reset, Output Compare 2 Interrupt is inhibited. When set, an interrupt is generated if the OCF2 flag is set.
  Note: The IC1IE and IC2IE (OC1IE and OC2IE) interrupt are not significant if the ICIE (OCIE) is set. In order to be taken into account, the ICIE (OCIE) must be reset.

PWM Mode
The OCF1 bit cannot be set by hardware in PWM mode, but the OCF2 bit is set every time the counter matches the value in the OC2R register. This can generate an interrupt if the OCIE is set or if the OCIE is reset and OC2IE is set. This interrupt will help any application where pulse widths or periods need to be changed interactively.

A/D CONVERTER (ADC)
A new A/D converter with the following main features has been added:

- 16 channels,
- 10-bit resolution,
- 4 MHz maximum frequency (ADC clock),
- 8 ADC clock cycles for sampling time,
- 20 ADC clock cycle for conversion time,
- Zero input reading 0x0000,
- Full scale reading 0xFFC0,
- Absolute accuracy is ± 4 LSBs.

This new A/D converter has the same architecture as the previous one. It still supports the an-alog watchdog feature, but now it uses only 2 of the 16 channels. These 2 channels are con-tiguous and channel addresses can be selected by software. With the previous solution using two ADC cells, four analog watchdog channels were available but at fixed channel addresses, channels 6 and 7.
Refer to the updated ST92F124/F150/F250 Datasheet for the description of the new A/D Con-verter.
 I²C

I²C IERRP BIT RESET
On the ST92F124/F150/F250 I²C, the IERRP (I2CISR) bit can be reset by software even if one of the following flags is set:

- SCLF, ADDTX, AF, STOPF, ARLO and BERR in the I2CSR2 register

- SB bit in the I2CSR1 Register

It is not true for the ST92F120 I²C: the IERRP bit cannot be reset by software if one these flags is set. For this reason, on the ST92F120, the corresponding interrupt routine (entered fol-lowing a first event) is re-entered immediately if another event occurred during the first routine execution.

START EVENT REQUEST
A difference between the ST92F120 and the ST92F124/F150/F250 I²C exists on the START bit generation mechanism.
To generate a START event, the application code sets the START and ACK bits in the I2CCR register:
– I2CCCR |= I2Cm_START + I2Cm_ACK;

Without the compiler optimization option selected, it is translated in assembler the following way:

- – or R240,#12
- – ld r0,R240
- – ld R240,r0

The OR instruction sets the Start bit. On the ST92F124/F150/F250, the second load instruction execution results in a second START event request. This second START event occurs after the next byte transmission.
With any of the compiler optimization options selected, the assembler code does not request a second START event:
– or R240,#12

NEW PERIPHERALS

- Up to 2 CAN (Controller Area Network) cells have been added. Specifications are available in the updated ST92F124/F150/F250 Datasheet.
- Up to 2 SCIs are available: the SCI-M (Multi-protocol SCI) is the same as on the ST92F120, but the SCI-A (Asynchronous SCI) is new. The specifications for this new peripheral are available in the updated ST92F124/F150/F250 Datasheet.

2 HARDWARE & SOFTWARE MODIFICATIONS TO THE APPLICATION BOARD

PINOUT

- Due to its remapping, CLOCK2 can not be used in the same application.
- SCI1 can only be used in asynchronous mode (SCI-A).
- The modifications of the analog input channels mapping can be easily handled by software.

INTERNAL VOLTAGE REGULATOR
Due to the presence of the internal voltage regulator, external capacitors are required on the Vreg pins in order to provide the core with a stabilized power supply. In the ST92F124/F150/F250, the core operates at 3.3V, while the I/Os still operate at 5V. The minimum recommended value is 600 nF or 2*300 nF and the distance between the Vreg pins and the capacitors must be kept to a minimum.
No other modifications need to be made to the hardware application board.

FLASH & EEPROM CONTROL REGISTERS AND MEMORY ORGANIZATION
To save 1 DPR, the symbol address definitions that correspond to the Flash and EEPROM control registers can

be modified. This is generally done in the linker script file. The 4 registers, FCR, ECR, and FESR[0:1], have been defined at 0x221000, 0x221001, 0x221002 and 0x221003, respectively.

The 128-Kbyte Flash sector reorganization also affects the linker script file. It must be modified in compliance with the new sector organization.

Refer to Section 1.4.2 for the description of the new Flash sector organization.

RESET AND CLOCK CONTROL UNIT

Oscillator

Crystal Oscillator

Even if the compatibility with the ST92F120 board design is maintained, it is no longer recommended to insert a 1MOhm resistor in parallel with the external crystal oscillator on a ST92F124/F150/F250 application board.

Figure 3. ST92F120 Crystal Oscillator
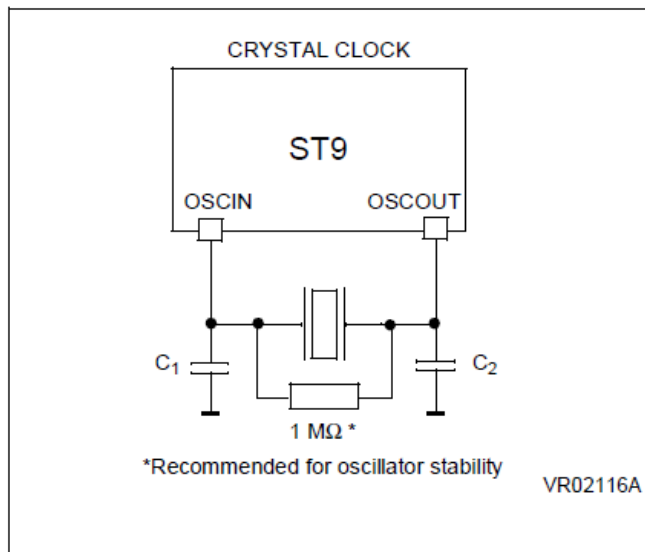
Figure 4. ST92F150 Crystal Oscillator
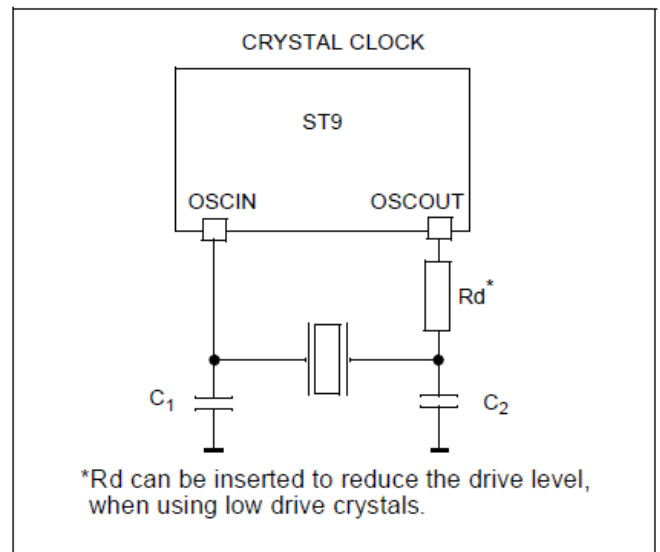
Leakages

While the ST92F120 is sensitive to leakage from GND to OSCIN, the ST92F124/F1 50/F250 is sensitive to leakage from VDD to OSCIN. It is recommended to surround the crystal oscil-lator by a ground ring on the printed circuit board and to apply a coating film to avoid humidity problems, if necessary.

External clock

Even if compatibility with the ST92F120 board design is maintained, it is recommended to apply the external clock on the OSCOUT input.

The advantages are:

- a standard TTL input signal can be used whereas the ST92F120 Vil on the external clock is between 400mV and 500mV.
- the external resistor between OSCOUT and VDD is not required.

Figure 5. ST92F120 External Clock
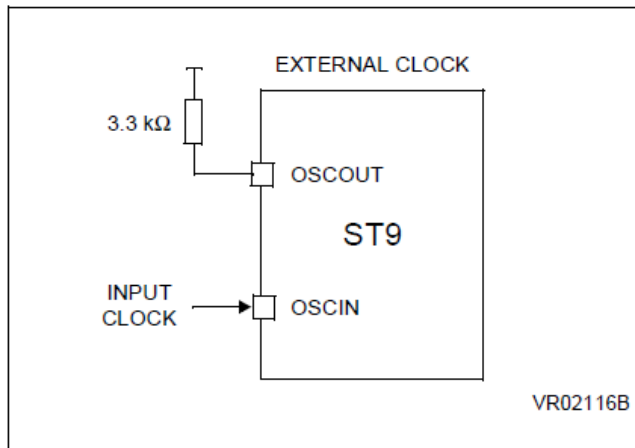
Figure 6. ST92F150 External Clock
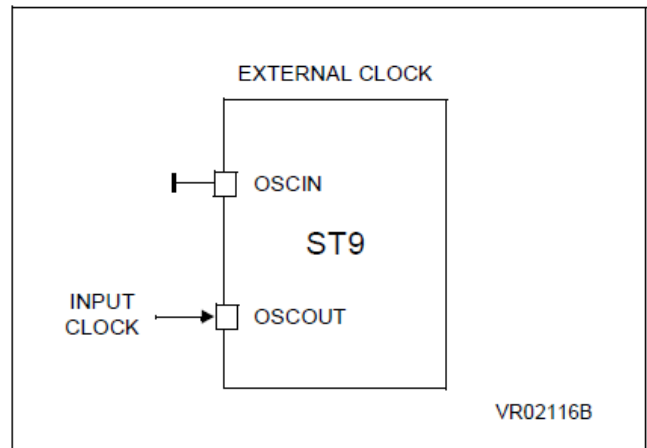
PLL
Standard Mode

The reset value of the PLLCONF register (p55, R246) will start the application in the same way as in the ST92F120. To use free running mode in the conditions described in Section 1.5, the PLLCONF[7] bit must be set.

Safety Clock Mode

Using the ST92F120, if the clock signal disappears, the ST9 core and peripheral clock is stopped, nothing can be done to configure the application in a safe state.

The ST92F124/F150/F250 design introduces the safety clock signal, the application can be configured in a safe state.

When the clock signal disappears (for instance due to a broken or disconnected resonator), the PLL unlock event occurs.

The safer way to manage this event is to enable the INTD0 external interrupt and to assign it to the RCCU by setting the INT_SEL bit in the CLKCTL register.

The associated interrupt routine checks the interrupt source (refer to the 7.3.6 Interrupt Generation Chapter of the ST92F124/F150/F250 datasheet), and configures the application in a safe state.

Note: The peripheral clock is not stopped and any external signal generated by the microcontroller (for instance PWM, serial communication…) must be stopped during the first instruc-tions executed by the interrupt routine.

EXTENDED FUNCTION TIMER
Input Capture / Output Compare

In order to generate a Timer Interrupt, a program developed for the ST92F120 may need to be updated in certain cases:

- If Timer Interrupts IC1 and IC2 (OC1 and OC2) are both used, ICIE (OCIE) of register CR1 has to be set. The value of the IC1IE and IC2IE (OC1IE and OC2IE) in the CR3 register is not significant. So, the program does not have to be modified in this case.

- If only one Interrupt is needed, ICIE (OCIE) must be reset and IC1IE or IC2IE (OC1IE or OC2IE) must be set depending on the interrupt used.

- If none of the Timer Interrupts are used, ICIE, IC1IE and IC2IE (OCIE, OC1IE and OC2IE) they must all be reset.

PWM Mode

A Timer Interrupt can now be generated each time Counter = OC2R:

- To enable it, set OCIE or OC2IE,
- To disable it, reset OCIE AND OC2IE.

10-BIT ADC

Since the new ADC is entirely different, the program will have to be updated:

- All data registers are 10 bits, which includes the threshold registers. So each register is divided into two 8-bit registers: an upper register and a lower register, in which only the 2 most significant bits are used:

Table 7. DiHR

7							0
Di.9	Di.8	Di.7	Di.6	Di.5	Di.4	Di.3	Di.2

Table 8. DiLR

7							0
Di.1	Di.0	0	0	0	0	0	0

- The start conversion channel is now defined by bits CLR1[7:4] (Pg63, R252).
- The analog watchdog channels are selected by bits CLR1[3:0]. The only condition is that the two channels must be contiguous.
- The ADC clock is selected with CLR2[7:5] (Pg63, R253).
- Interrupt registers have not been modified.

Because of the increased length of ADC registers, the register map is different. The location of the new registers is given in the description of the ADC in the updated ST92F124/F150/F250 Datasheet.

I²C

IERRP BIT RESET

In the ST92F124/F150/F250 interrupt routine dedicated to the Error Pending event (IERRP is set), a software loop must be implemented.
This loop checks every flag and executes the corresponding needed actions. The loop will not end until all flags are reset.
At the end of this software loop execution, the IERRP bit is reset by software and the code exits from the interrupt routine.

START Event Request

To avoid any unwanted double START event, use any of the compiler otpimization options, in the Makefile.

For instance:
CFLAGS = -m$(MODEL) -I$(INCDIR) -O3 -c -g -Wa,-alhd=$*.lis

UPGRADING AND RECONFIGURING YOUR ST9 HDS2V2 EMULATOR

INTRODUCTION

This section contains information about how to upgrade your emulator's firmware or recon-figure it to support a ST92F150 probe. Once you have reconfigured your emulator to support a ST92F150 probe you can configure it back to support an other probe (for example a ST92F120 probe) following the same procedure and choosing the suitable probe.

PREREQUISITES TO UPGRADING AND/OR RECONFIGURING YOUR EMULATOR

The following ST9 HDS2V2 emulators and emulation probes support upgrades and/or recon-figuration with new probe hardware:

- ST92F150-EMU2
- ST92F120-EMU2
- ST90158-EMU2 and ST90158-EMU2B
- ST92141-EMU2
- ST92163-EMU2

  Before trying to perform the upgrade/reconfiguration of your emulator, you must ensure that ALL of the following conditions are met:

- The monitor version of your ST9-HDS2V2 emulator is higher than or equal to 2.00. [You can see which monitor version your emulator has in the Target field of the About ST9+ Visual Debug window, which you open by selecting Help>About.. from the ST9+ Visual Debug's main menu.]
- If your PC is running on the Windows ® NT ® operating system, you must have the administrator privileges.
- You must have installed the ST9+ V6.1.1 (or later) Toolchain on the host PC connected to your ST9 HDS2V2 emulator.

HOW TO UPGRADE/RECONFIGURE YOUR ST9 HDS2V2 EMULATOR
The procedure tells you how to upgrade/reconfigure your ST9 HDS2V2 emulator. Be sure you meet all the prerequisites before starting, otherwise you could damage your emulator by performing this procedure.

1. Ensure that your ST9 HDS2V2 emulator is connected via the parallel port to your host PC running either Windows ® 95, 98, 2000 or NT ®. If you are reconfiguring your emulator to be used with a new probe, the new probe must be physically connected to the HDS2V2 main board using the three flex cables.
2. On the host PC, from Windows ®, select Start >Run….
3. Click the Browse button to browse to folder where you installed the ST9+ V6.1.1 Toolchain. By default, the installation folder path is C:\ST9PlusV6.1.1\… In the installation folder, browse to the ..\downloader\ subfolder.
4. Locate the ..\downloader\<ST9xxxx-EMU2>\ directory corresponding to the name of the emulator you want to upgrade/configure.
   For example, if you want to reconfigure your ST92F120 emulator to be used with the ST92F150-EMU2 emulation probe, browse to the ..\downloader\<ST92F150-EMU2>\ directory.
   5. Then select the directory corresponding to the version you wish to install (for example, the V1.01 version is found in ..\downloader\<ST92F150-EMU2>\v1.01\) and select the file <setup_st9xxxx.bat> (for example, setup_st92f150.bat).
   6. Click on Open.
   7. Click OK in the Run window. The update will begin. You have simply to follow the instructions displayed on your PC's screen.
   WARNING: Do not stop the emulator, or the program while the update is in progress! Your emulator may be damaged!

Documents / Resources

STMicroelectronics ST92F120 Embedded Applications [pdf] Instructions
ST92F120 Embedded Applications, ST92F120, Embedded Applications, Applications

References

- **STMicroelectronics: Our technology starts with you**

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