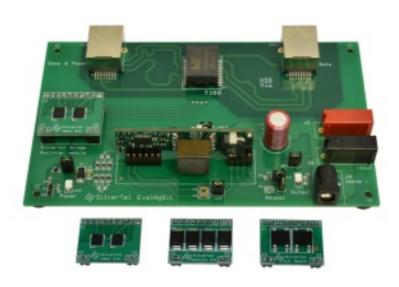


# Silvertel EvalAgSil SIL Module Evaluation Board User Manual

Home » Silvertel » Silvertel EvalAgSil SIL Module Evaluation Board User Manual

## Silvertel EvalAgSil SIL Module Evaluation Board



#### **Contents**

- 1 Kit Contents
- 2 Introduction
- 3 Board Layout
  - 3.1 Link Settings
- 4 Input
  - 4.1 Diode Bridge
  - **Selection**
  - 4.2 Input Signature
  - 4.3 PSE Detect
  - 4.4 Output
  - 4.5 Data Output
- **5 Operation** 
  - 5.1 LED output
  - **5.2 EMI**
- **6 Test Setup** 
  - **6.1 Data Throughput**
- 7 Additional information
- 8 Schematic
- 9 Bill of Materials
- 10 Documents / Resources
- 11 Related Posts

#### **Kit Contents**

- EvalAgSil Evaluation Board
- Bridge Rectifier Module
- · Schottky Bridge Rectifier Module
- Ideal Bridge Rectifier Module

## Introduction

This manual is intended to be a guide to using the "EvalAgSil Evaluation Board" with one of Silvertel's SIL (Single-In-Line) footprint PD (Powered Device) modules. The board is designed to handle 10/100/1000/10GBASE-T Ethernet data rates.

This board has been designed to assist with evaluating the use of Silvertel's SIL format modules in an application; as such it has been design to pass through Ethernet data signals (10/100/1000/10GBASE-T) from the Midspan PSE (Power Sourcing Equipment) or PoE enabled switch connected to J100, onto the system connected to J101.

## **Board Layout**

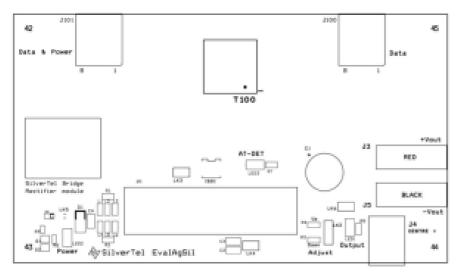


Figure 1: EvalAgSil Board Layout

## **Link Settings**

LK2 – Output Adjust Select

LK3 - AT-DET LED Enable

LK4 - 'V' cap Enable

LK5 – Input Power LED Enable

LK6 - Output Power LED Enable

Series	power CI ass	Variant	Voltage (V)	notes
Ag5400	4	Ag5405	5	
		Ag5412	12	
		Ag5424	24	
Ag5300	4	Ag5300	12	
		Ag5305	5	
		Ag5324	24	
Ag9200	3	Ag9205	5	Class Programming Is fixed to Class 0 Output Volatge Dow n Adjust Limited by default
	3	Ag9703-S	3	
Ag9700		Ag9705-S	5	Ag9700-2BR and Ag9700-FL models are not compatible O utput Volatge Down Adjust Limited by default
		Ag9712-S	12	

## Input

One of Silvertel's PD modules fitted to the EvalAgSil evaluation board will present a valid signature and classification request to an IEEE compliant PSE through its RJ45 connector J101.

#### **Diode Bridge Selection**

The EvalAgSil has the option to fit different bridge rectifier technologies. Supplied with the EvalAgSil are three bridge rectifier modules for evaluating the losses involved when using different rectifier technologies:

- Bridge Rectifier Module featuring 2x DF01S bridge rectifiers
- Schottky Bridge Rectifier Module featuring 8x SS36 Schottky rectifier diodes
- Ideal Bridge Rectifier Module featuring 2x FDMQ8205A MOSFET bridge rectifiers

A simple method of utilising the most power output on a PoE system is to reduce the losses involved in the rectification. Rectification is required to enable the PD to be insensitive to the polarity of the power on the pairsets in a PoE system.

Schottky rectifiers are an improvement over conventional bridge rectifiers due to their lower forward voltage drop, a greater improvement can be made by switching to an active bridge rectifier topology.

The chosen bridge rectifier module should inserted into to EvalAgSil board using the two 2 pin and one 10 pin headers on the left hand side of the board before power is supplied to the board.

Pairsets	Мо	de A	Mode B	
Pairs	Pair 1	Pair 2	Pair 3	Pair 4
Conductor	1 and 2	3 and 6	4 and 5	7 and 8
	Valid 2-pair configurations			
	Р	N	_	_
	N	Р	_	_
	_	_	Р	N
	_	_	N	Р
	Р	N	Р	_
	Р	N	_	Р
	N	Р	Р	_
	N	Р	_	Р
	Р	_	Р	N
	_	Р	Р	N
	Р	_	N	Р

_	Р	N	Р		
Valid 4-pair configurations					
N	Р	N	Р		
N	Р	Р	N		
Р	N	N	Р		
Р	N	Р	N		
P denotes a	pair connected to nega pair connected to posit a pair not connected to	tive potential			

#### **Input Signature**

The EvalAgSil board will automatically direct the power from J101 through the bridge rectifier module to the input of the Silvertel module fitted into U1.

This module will provide a 25K signature required to be powered from an IEEE compliant PSE.

The EvalAgSil has been designed to be powered by any compliant IEEE802.3 PSE such as Silvertel's Ag6120 PSE module.

#### **PSE Detect**

When U1 on the EvalAgSil board has been populated with a module that contains an `ATDET' feature, and it has detected it is being powered by an IEEE802.3 type 2 or greater PSE, the `at Flag' pin will be pulled low, and this will cause LED3 to become illuminated on the EvalAgSil board.

#### Output

The output voltage will be present on both the DC10 connector, J4 and the banana plug terminals J3 and J5. J3 and the centre pin of J4 are the positive outputs, with the outer ring of J4 and J5 being the negative output.

## **Output Adjust**

By default the nominal output voltage of the fitted module will be present on the output connectors. This can be adjusted up or down using the adjust connector, LK2.

The EvalAgSil is fitted with two adjust resistors. The down adjust resistor R3, is fitted with a 68k resistor. And the up adjust resistor R4, which is fitted with a 0 resistor. Depending on the module fitted the down adjust resistor, R3 may have to be replaced with a different value in order to provide the full down adjust stated in the corresponding datasheet.

To increase the output voltage, insert a jumper to LK2 in the upper position, so that the link is between the middle and upper pin.

To reduce the output voltage, insert a jumper to LK2 in the lower position, so that the link is between the middle

and lower pin.

If the output voltage needs to be set to a different value (within the adjustment range) then connect different value resistors in place of R3 (0) or R4 (68K) and connect the jumper into the corresponding link setting.

Note: ensure that the down adjust resistor is not shorted when connecting a module that has a higher stated resistance in the datasheet, as this could cause damage to the module.

#### **Data Output**

Any data that is provided over the PI (Ethernet cable) connected to the Data & Power port, J100 will be transposed onto the Data output port, J101 via the data transformer.

The data traces on the evaluation board have been designed to pass through 10/100/1000/10GBASE-T Ethernet data signals. No processing or amplification of this signal will be performed on the evaluation board

## Operation

To ensure that the PSE does not apply power to a non-PoE enabled device the output port first checks for a valid PoE signature. If the PSE does not see a valid signature then it will disconnect, wait approximately 2 seconds then try again. Once a valid signature has been detected the PSE will then perform classification to determine the power requirement of the PD, only after this has occurred will the PSE supply power to the powered device.

#### **LED** output

There are three LEDs fitted to the EvalAgSil board, each of these can be disabled by removing the associated link jumper.

Name	Locatio n	Enabl e Link	Description
Output	LED1	LK6	Illuminates with 3-30Vdc across the output
Power	LED2	LK5	Illuminates with 33-58Vdc across the output of the bridge rectifier module
AT-DET	LED3	LK3	Illuminates when a Type 2 or greater PSE is detected

#### ЕМІ

The EvalAgSil contains many of the recommended components for preliminary EMI testing of an application. `V' capacitors, C2 & C3, can be enabled by inserting a jumper on to LK4.

The board is fitted with ferrite beads, L1-6; if these are not required they can be effectively removed from the circuit by fitting R1 and R2 with 0 resistors.

With some of the newer Silvertel module designs an additional EMI filtration method is to fit a 68nF capacitor to C4. Silvertel recommend that this capacitor is rated to 250V so that it retains more of the rated capacitance in the operating voltage range.

#### **Test Setup**

Figure 2 shows the basic set up using the EvalAgSil evaluation board powered by Silvertel's EvalAg6120 PSE.

The equipment required: -

- EvalAgSil fitted with compatible Silvertel PD Sil Module.
- EvalAg6120 or other IEEE802.3 compliant PSE
- Power supply unit, +44-57V output e.g. 60V bench power supply
- CAT5e or greater cables
- · Application Circuit

## Optional equipment: -

• Data source e.g. PC

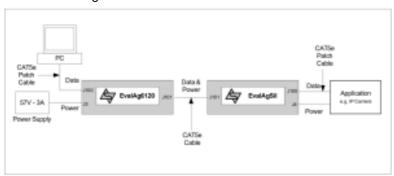


Figure 2 Basic Test Setup

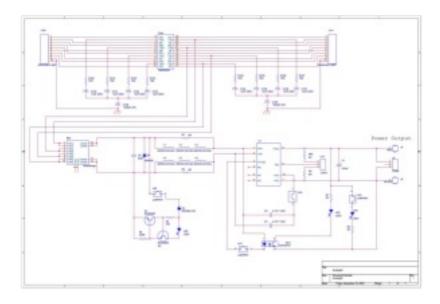
#### **Data Throughput**

To pass data via the Evaluation boards, the data input (e.g. Internet) can be connected to J100 on the EvalAg6120 Board using a cat5e cable. The data is then passed through the data transformer, where power is added and sent out via connector J101 of the EvalAg6120 Board. The Data and power is extracted through J101 of the EvalAgSil board and then divided into its separate power and data through the data transformer. The data output is then available from J100 of the EvalAgSil Board, which can then be connected to the application device.

### **Additional information**

Full operating conditions and features of the Silvertel module set can be found in the relevant product datasheet, available from www.silvertel.com.

#### **Schematic**



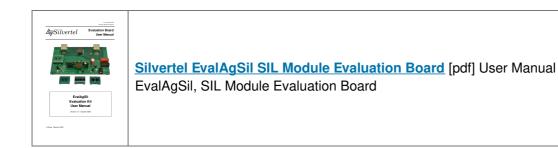
## **Bill of Materials**





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## **Documents / Resources**



Manuals+,