SILICON LABS EFR32 Series 2 Long Range User Guide

UG460.2: EFR32 Series 2 Long Range Configuration Reference

Contents

EFR32 Series 2 Long Range

To help customers achieve the crucial design element of maximum effective range, Silicon Labs has a Long Range radio profile for the EFR32 Series 2 family of Wireless MCU devices, fully compatible with the existing solution on Series 1. From the current lineup, only SubGHz capable ones are supported, namely FG23/FG25/FG28. This guide introduces the profile, describes its development, and examines underlying details that enable it to realize extended range. It also includes an exercise to build a Range Test example using Simplicity Studio 5 and to explore the Long Range profile, so that you can quickly begin implementation in your next project.
This guide is designed for developers who would like to test long range performance on EFR32 Series 2 devices using Simplicity Studio 5 and Silicon Labs development hardware. It provides instructions to get started using the example applications provided with the Gecko SDK Suite (GSDK) v4.

KEY FEATURES

- Learn about DSSS
- Learn about the Long Range Profile
- Learn about the Radio Configurator
- Create a Range Test application with a long range PHY
- Overview measured performance metrics

Introduction

One of the most important performance metrics for an IoT application is maximum usable range. Practically speaking, this refers to the maximum distance at which messages can be received without a loss of information. The achievable range is impacted by many different factors:

- Hardware influences, including:
  - Antenna physical parameters (size, shape, directivity, gain)
  - Battery physical parameters (size, capacity, load current, and so on)
- Propagation attributes of the radio signal (carrier frequency, humidity, obstacles, and so on)
- Transmit power
- Receiver sensitivity

To maximize usable range, when developing the Long Range (LR) profile Silicon Labs targeted the last item above, receiver sensitivity, which is affected by multiple input parameters:

- Frame length: The amount of data to be transported
- Data rate: The timeframe available to transport the data
- Baud rate offset tolerance: How much the data rate can change during reception
- Frequency offset tolerance: How severely the carrier frequency can vary during the reception
- Selectivity and blocking: Robustness against interferer signals

Though many paths can be taken to improve RX sensitivity, Silicon Labs avoided hardware changes and instead focused on radio configuration modifications. This reliance on PHY development insulated the Long Range profile from additional external hardware dependencies, making the LR PHY benefits available to a broader selection of applications.
The construction of these PHYs is detailed in the next chapter. Chapter 3 provides instructions on evaluating the Long Range Profile using new Silicon Labs development tools and hardware. Chapter 4 reviews real-world measured performance with the LR PHYs.

Development of the EFR32 Long Range PHYs

The fundamental approach to extend usable range is to decrease receiver bandwidth, while keeping key signal parameters for the demodulator, such as modulation index for FSK, intact. A few rules of thumb help to visualize what is possible by this effort:

- Reducing bandwidth by half improves sensitivity by 3 dB
- Reducing bandwidth by 90% (to 1/10th of the original) boosts sensitivity by 10 dB

A straightforward compromise to achieve bandwidth reduction is to decrease the data rate. By cutting bandwidth

in favor of sensitivity, one has to also contend with the resulting degradation in frequency offset tolerance. Therefore, such narrow-band PHYs require very accurate and stable clock references (for example, a 0.5 ppm TCXO), and those elements are more costly. In terms of RF immunity, the effect of going narrow band is mixed, with some improvement in selectivity and blocking offset by extended packet time and exposure to interferers due to the reduced data rate.

Importantly, all of these drawbacks can be mitigated by using Direct Sequence Spectral Spreading (DSSS). This technique, which is available for all major modulation formats on the EFR32, is explored in the following section.

2.1 DSSS: Theory of Operation

DSSS is a technique to increase the bandwidth of a transmitted signal, and thereby decrease its power spectral density. It is beneficial for the receiver side as well, as the robustness (immunity against interferer signals) significantly improves. This section reviews the DSSS implementation on EFR32 Series 2 devices.

2.1.1 TX Side

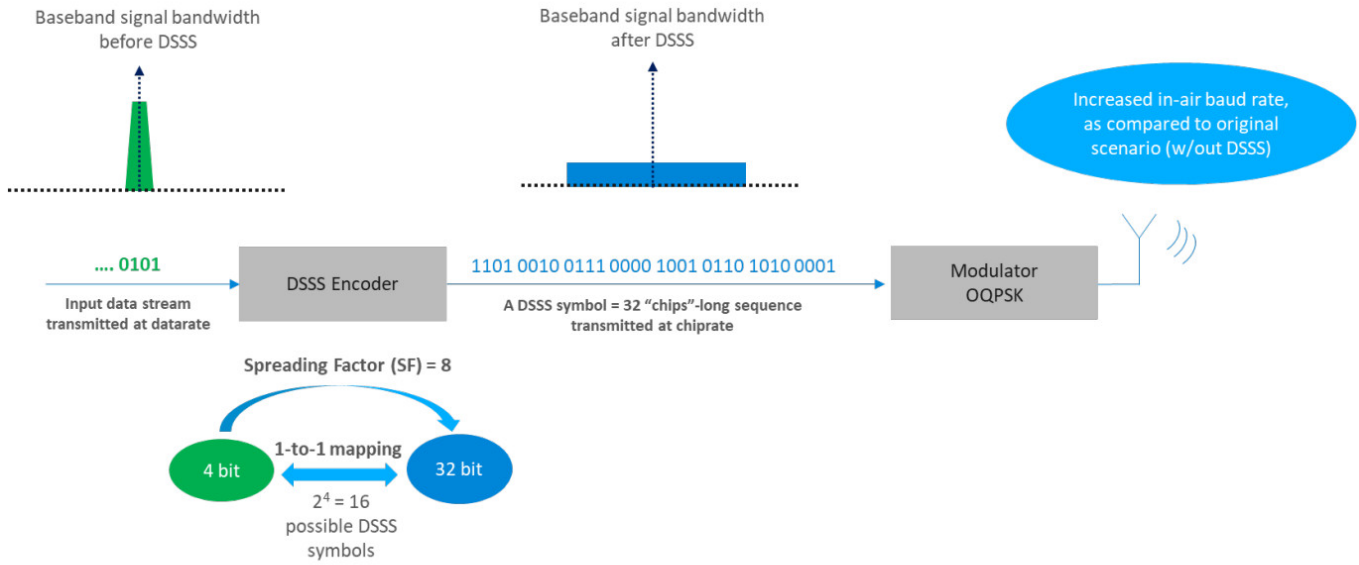


Figure 2-1. Transmission of 802.15.4 Signals Using DSSS

The above figure shows how a DSSS-based signal is constructed. As a practical demonstration vehicle, this example uses the 802.15.4 Zigbee packet format.

The baseband input signal is a narrow band, low data rate signal stream (its spectrum plot represented by the green cone). This bitstream is fed into a DSSS encoder, which replaces every 4 bits of the bitstream with a 32-bit symbol, often referred to as 32 "chips".

Transmitting 1 symbol takes the same amount of time as transmitting 4 bits of the original data stream. This means that the "chip rate" is 8x higher than the original data rate, a multiplier often referred to as the Spreading Factor.

The blue rectangle (spectrum plot of baseband input signal after DSSS encoding) demonstrates that the original narrow band signal has become much wider (though not quite 8x), with less power density. The resulting data stream with the chip rate is then fed into the modulator and radiated over the air. Therefore, by increasing the link's in-air baud rate, the same data can be transmitted with the same net data rate, over the same period of time, but using a much wider band and lower power spectral density.

2.1.2 RX Side

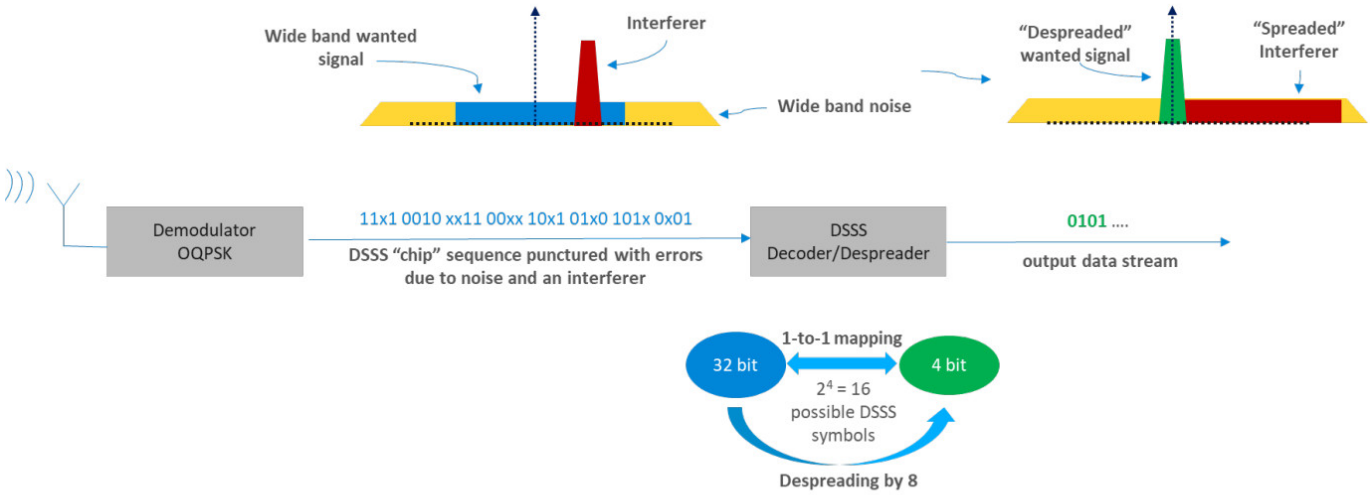


Figure 2-2. Reception of 802.15.4 Signals Using DSSS

The above figure shows reception of the DSSS-encoded transmission detailed in the previous section. The demodulator retrieves the data stream from the OQPSK signal. The bits are changing with the chip rate, and the stream may contain errors due to the presence of noise and interferers in the air.
The plot at the top left corner of the above figure demonstrates the spectral conditions while receiving a DSSS packet. The red pyramid indicates the presence of a strong narrowband interferer, while the yellow trapezium represents the wideband noise.
This corrupted chip stream is fed into the DSSS Decoder, which replaces every 32-chip long symbol with a 4-bit pattern in restoring the original data stream. Up to a given error rate in the chip stream, the decoder can still identify the correct 32-chip symbols due to the 8x redundancy presented by the scaling factor.
The spectrum plot at the top right corner of the figure shows that the original green cone has been restored by this de-spreading procedure, while the red cone has been "smeared" with the noise. As a result, SNR is increased, which compensates for the increased noise power experienced by the demodulator due to the high in-air bandwidth.

2.2 DSSS: Practical Impacts

As a result of using DSSS, an application is subject to the following considerations:

- Co-channel and adjacent channel selectivity improve by a factor of the coding gain (3 to 8 dB, depending on spreading factor).
- A less accurate (cheaper) crystal can be used for the clock reference.
- Higher TX power can be used in cases where the regulatory limit is defined as maximum allowed power spectral density.
- DSSS alone does not technically improve RX sensitivity to in-air signals:
- Receiving a 1 kbps data stream exhibits the same RX sensitivity whether or not the signal content is DSSS-encoded.
- DSSS increases the symbol rate and bandwidth of the signal physically present in the air, which actually degrades reception at the RX side, but this consequence is compensated by the DSSS processing gain in the receiver.

2.3 Scaling Down the 802.15.4 O-QPSK PHY

To leverage the benefits of DSSS and develop Long Range options for EFR32 Series 2 devices, Silicon Labs began with the highly optimized 2.4 GHz 802.15.4 Zigbee OQPSK PHY and derived a series of radio configurations to serve a variety of sensitivity and tolerance requirements. Essentially, the data rate (and therefore the occupied bandwidth) has been scaled down, while retaining the same Zigbee coding scheme: OQPSK, DSSS SF=8, and 32-bit symbol length with a 4-bit symbol map. The resulting PHY configurations are currently available

for FG23 / FG25 / FG28 variants of the Series 2 family.
The following table shows one group of PHYs optimized for a lower frequency band, and another group optimized at a higher frequency band. Notably, the stated performance is maintained when setting the carrier frequency to anywhere within each band.

The table indicates the required XO accuracy for the TX and RX side combined, an offset budget of a given LR link. This presents a cost savings opportunity on nodes manufactured in large quantities vs low volume base stations, where you can asymmetrically distribute the XO accuracy budget to reduce the cost of high-volume elements. Most commonly in practice, the value in the table is split between TX and RX devices.

Note: The last item, 80 kbps for 915MHz, can be used to pass FCC 15.247 requirements without the need for frequency hopping, as the occupied bandwidth (- 6 dB) of the signal is >= 500 kHz.

Table 2-1. PHY Configuration Options on the Long Range Profile

Frequency Band[MHz]	Data Rate [kbps]	(TX + RX) XO Accuracy [ppm +/-]
434/490	1.2	2.5
434/490	2.4	5
434/490	4.8	10
434/490	9.6	20
434/490	19.2	40
868/915	2.4	2.5
868/915	4.8	5
868/915	9.6	10
868/915	19.2	20
868/915	38.4	40
868/915	80	80

2.4 Radio Boards Supporting Long Range PHY Evaluation

Many configurations within the Long Range Profile can be successfully demonstrated on any radio board with a supported EFR32 Series 2 SoC and suitable sub-GHz band support.

- Please note that Silicon Labs typical radio boards have a +/- 10ppm crystal as a reference.
- Refer to PHY config XO tolerances in Table 2-1. PHY Configuration Options on the Long Range Profile above to verify support for your preferred PHY using two (2) +/- 10ppm radio boards (+/- 20ppm combined).
- If your PHY of choice requires tighter tolerance applying a TCXO is recommended

For reference, the following table specifies development boards Silicon Labs used for testing, but as said, any sub-GHz capable board with FG23/FG25/FG28 on it can be used. For the test, Silicon Labs used 0.5 ppm TCXO.

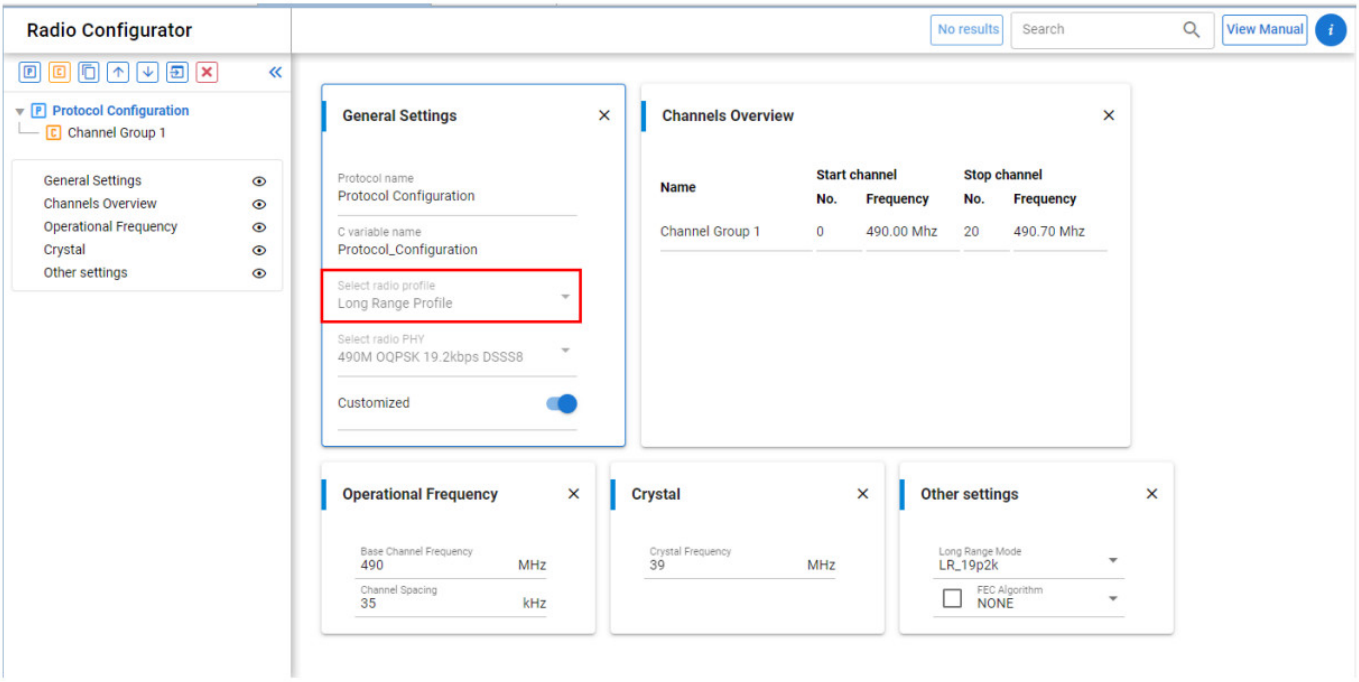
Table 2-2. Radio Boards Used During Testing

Ordering Part Number	Board ID	Board Configuration
xG23-RB4204D	BRD4204D	EFR32ZG23 868-915 MHz 14 dBm Radio Board
FG23-RB4265A	BRD4265A	EFR32FG23 433 MHz 10 dBm Radio Board

Using the Long Range Profile in Simplicity Studio 5

3.1 Long Range Profile in the Radio Configurator

Simplicity Studio 5 (SSv5) makes it easy to access Long Range PHY configurations by selecting the Long Range profile in the Radio Configurator interface. If you need a refresher, please see the **Simplicity Studio 5 User's Guide** and **AN1253: EFR32 Radio Configurator** Guide for Simplicity Studio 5 for more information on building an example wireless application with the Radio Configurator.



Click the Select radio profile dropdown and select Long Range Profile. Note that PHYs in this profile have reduced configuration options (carrier frequency, and FEC enable), described here:

- Carrier frequency can be set to anywhere within each band – baseband performance will be sustained at all frequencies within a given band. However, be aware that external components (antenna matching for example) can exhibit a frequency dependence.
- FEC (Forward Error Correction) can be enabled for any of the PHY configurations:
  - Current FEC options in EFR32 Series 2 are convolutional codes with a rate of ½, doubling the number of transmitted symbols after the sync word. Enabling FEC does not automatically adjust the data rate. To maintain the original effective throughput, manually select a data rate that is twice the original rate.
  - FEC does not increase sensitivity, but it can protect against bit errors over the payload due to interferer signals.

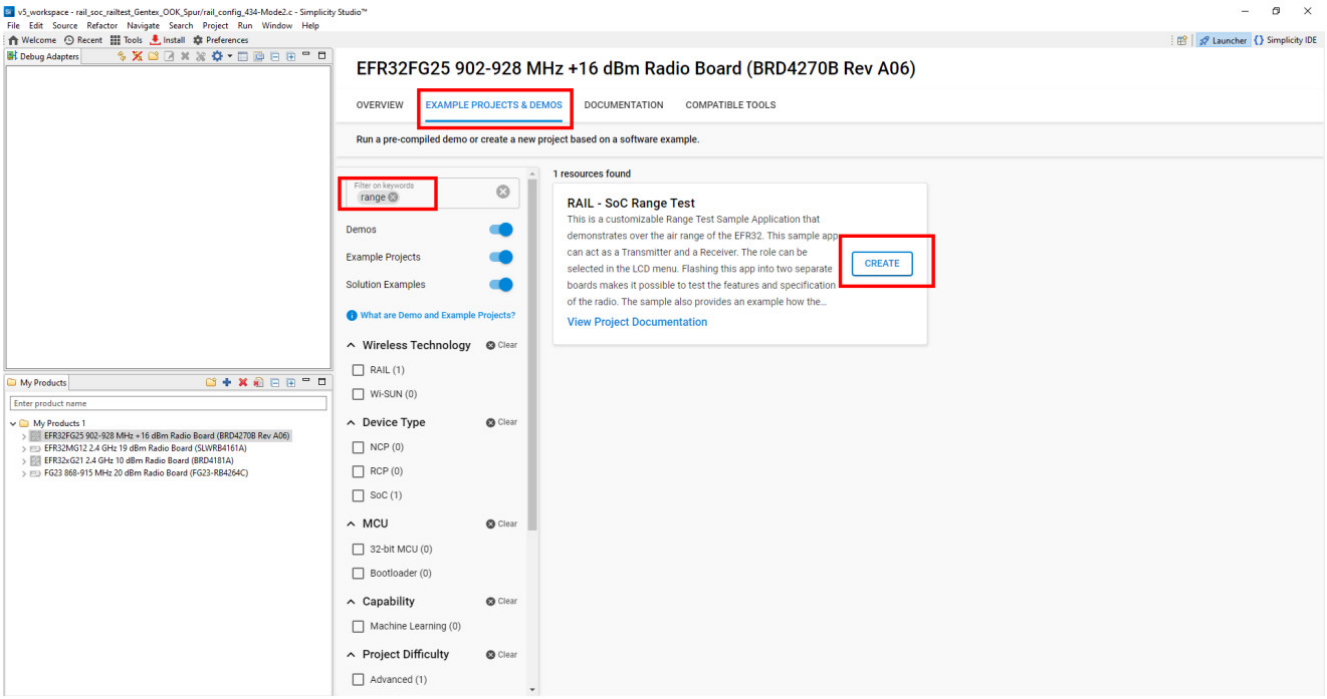
The next section provides a procedure to construct a complete example application with which to evaluate PHYs in the Long Range Profile using two EFR32 radio boards.

3.2 Build a Range Test Example Application

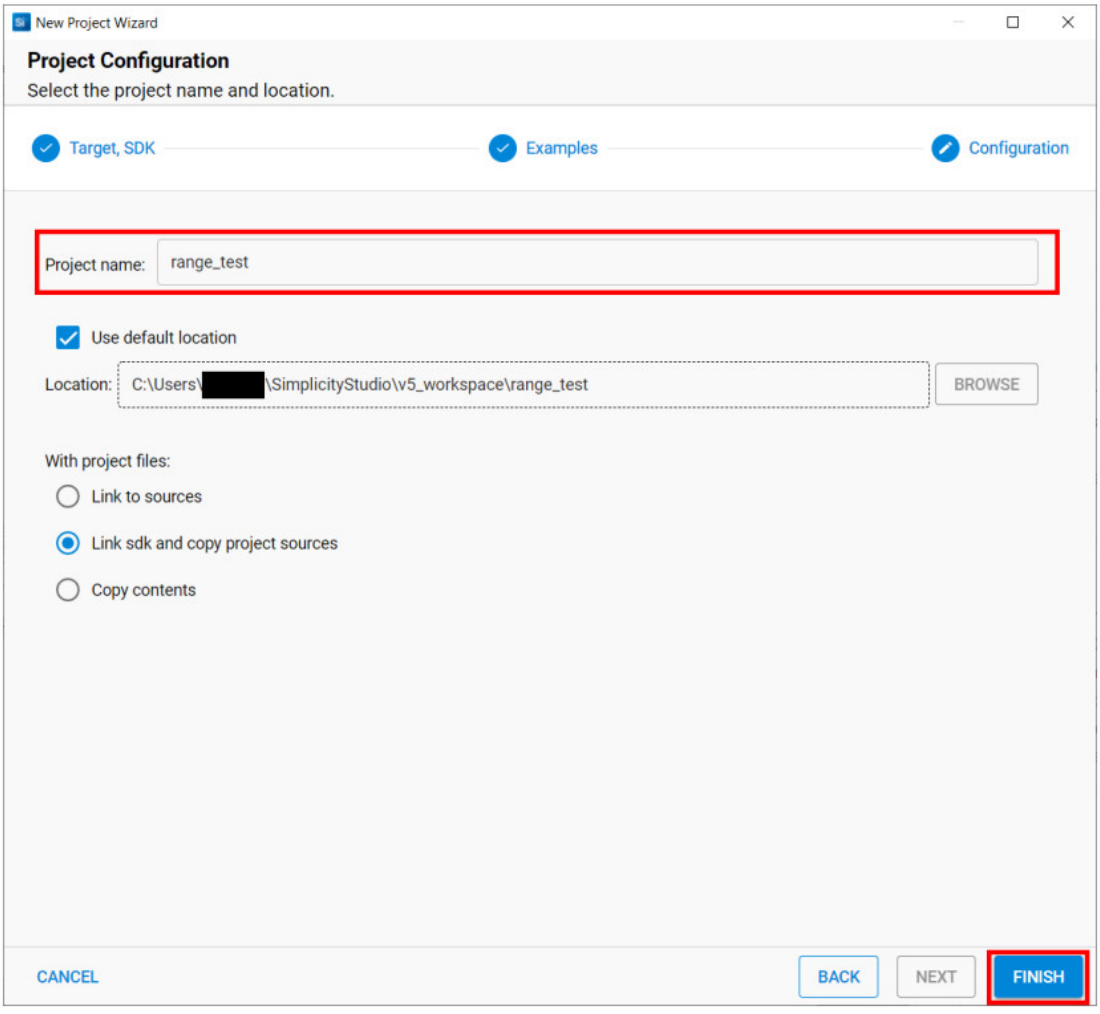
This section describes the steps to build a Range Test application, and is based on **UG147: Range Test Demo**

User's Guide. Additional guidance on using the Range Test application can be found in this article. The procedure assumes that you have downloaded the Flex SDK, and have connected the two boards required for this example, as described in the Simplicity Studio 5 User's Guide.

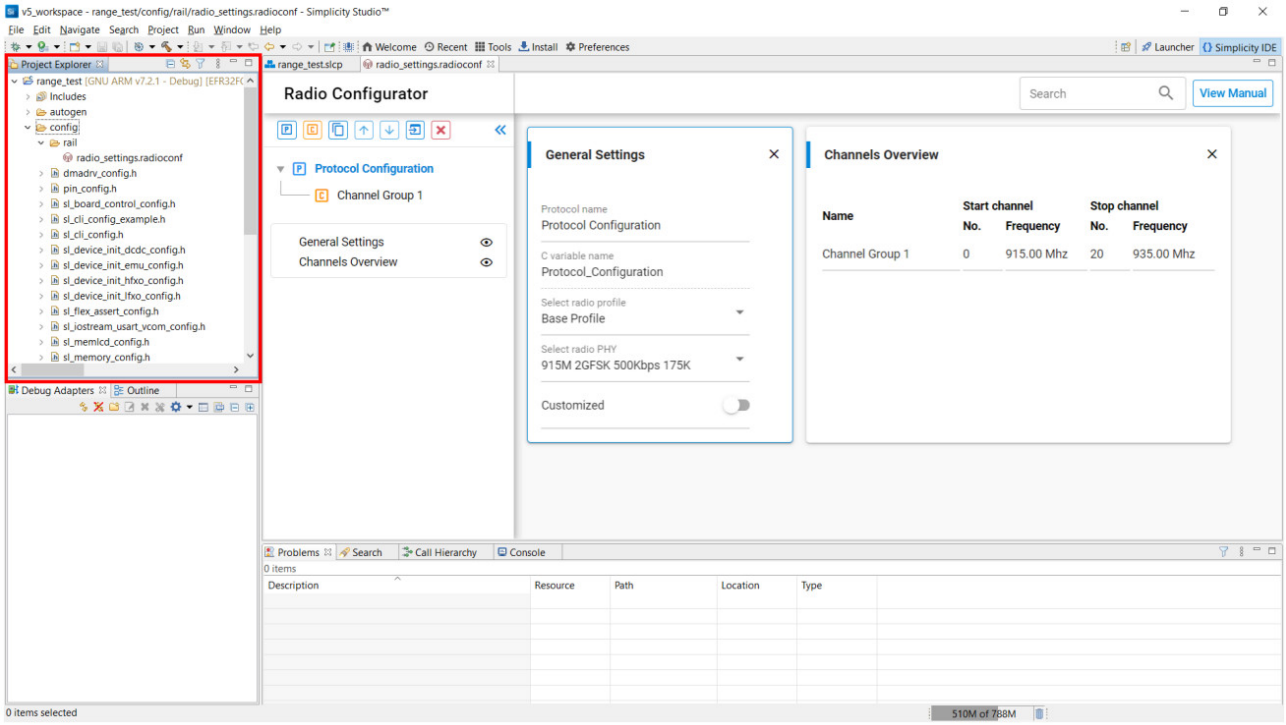
1. Click the "Example Projects & Demos" tab to see the projects available for the selected target hardware.
2. Scroll down or use the example filter to locate the "RAIL – SoC Range Test" project, and then click CREATE.



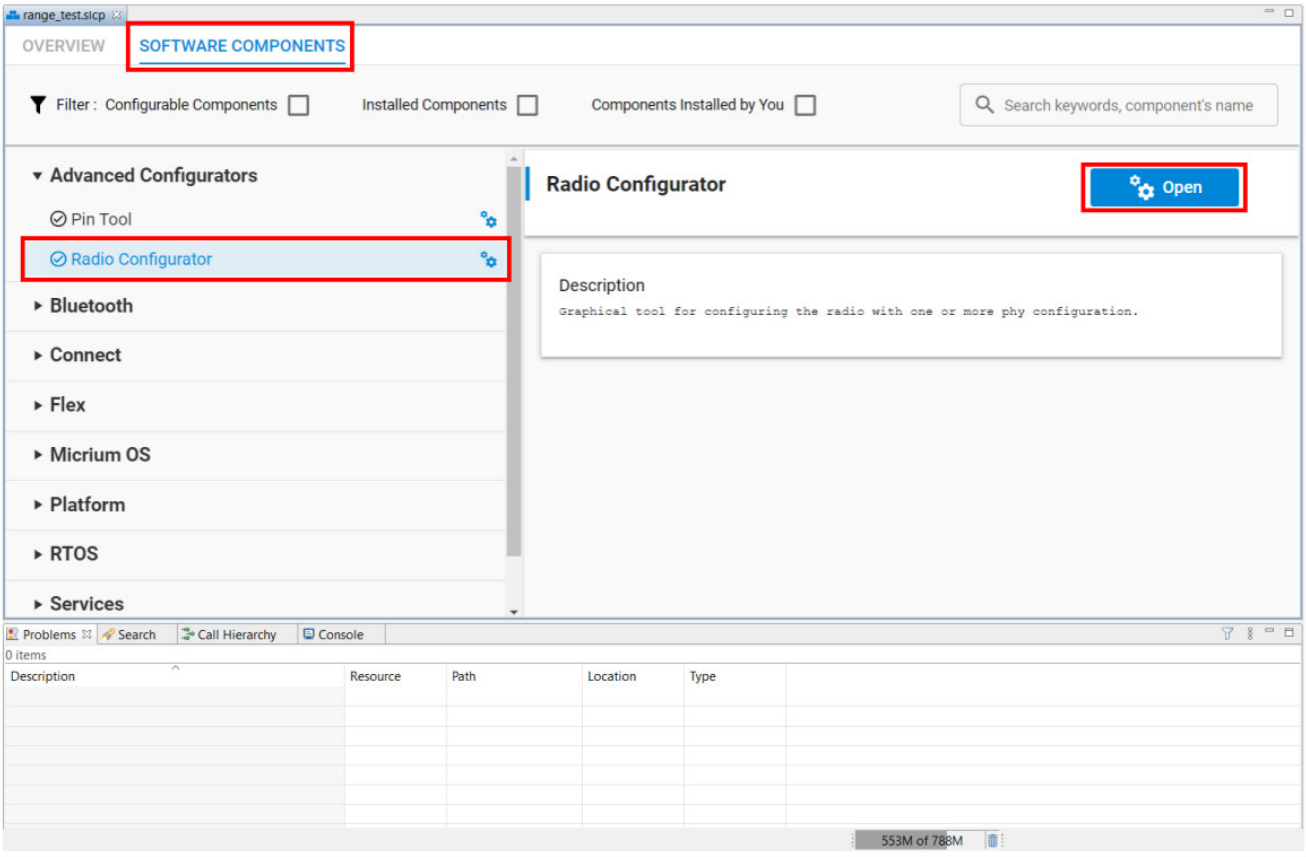
3. Enter the name of the project you want to create, or just leave it as the default, "range_test".
4. Click FINISH to create the new project.



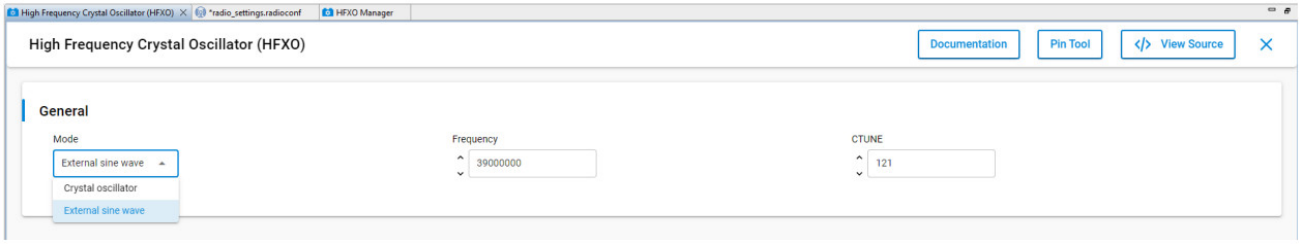
5. Once the project is created, SSv5 opens the Simplicity IDE perspective, and the radio configuration GUI appears. From the Project Explorer view, you can see the project files that have been generated.



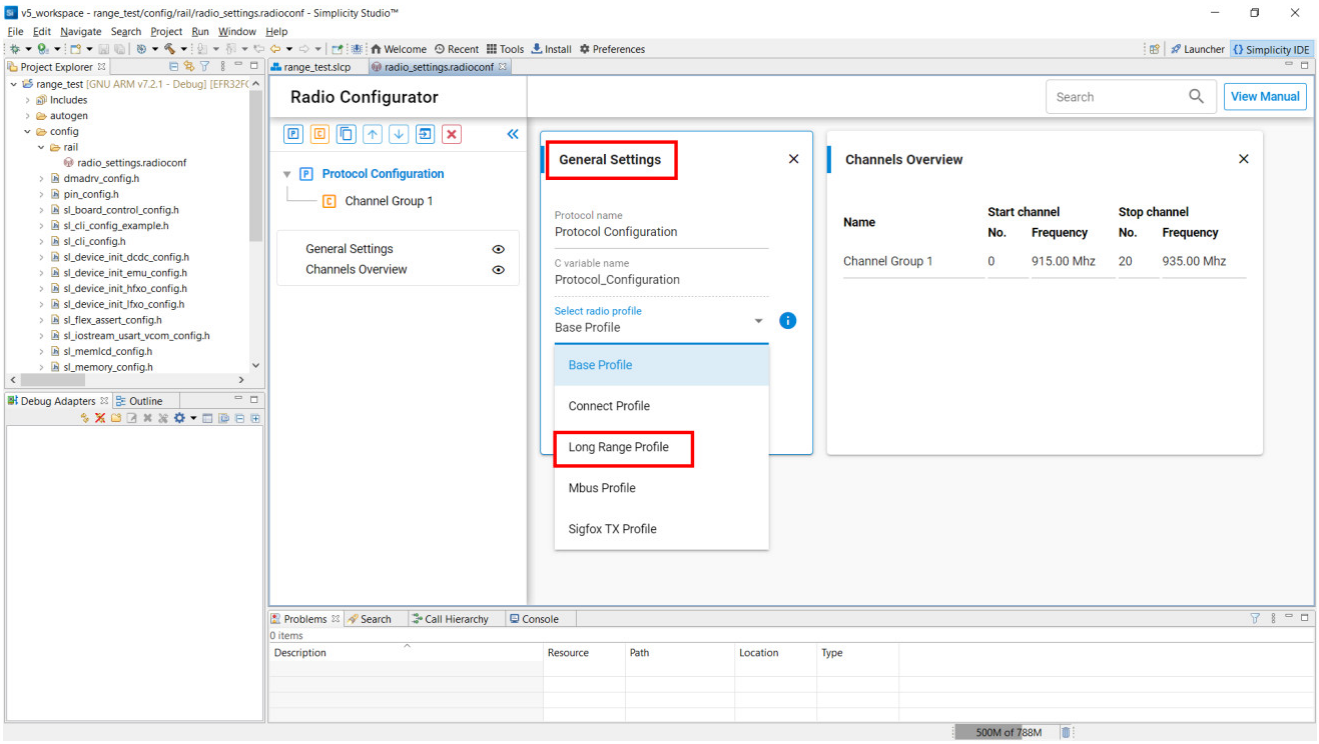
If you close this tab, the Radio Configurator can be accessed again at any time via the Software Components tab. Click the Advanced Configurators item, then Radio Configurator (alternatively, you can simply search for configurator using the search input at the top right of the .slcp frame). Once this Radio Configurator gateway element has been located, simply click OPEN to its right and proceed to the next step.



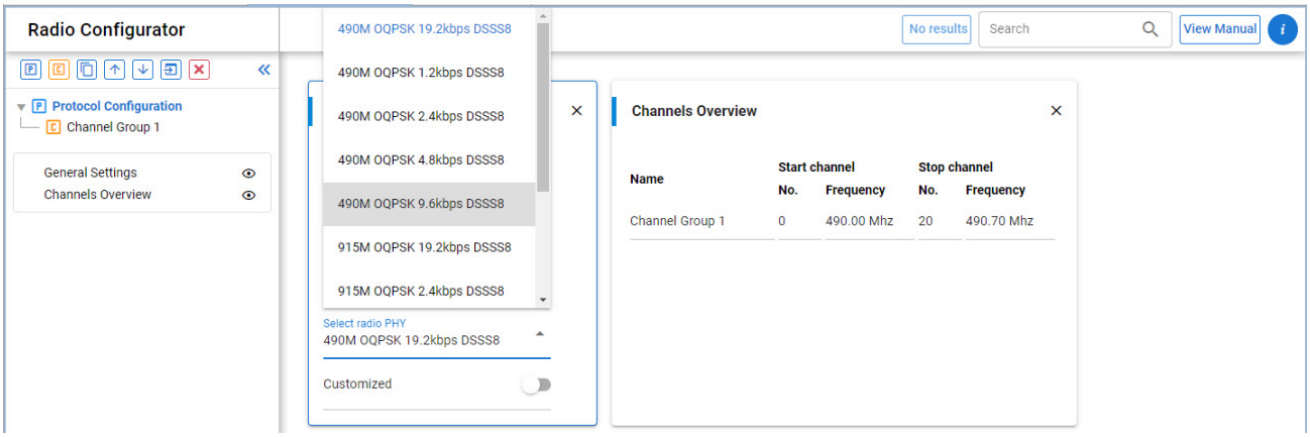
If you have a radio board with a TCXO on it, change the HFXO software component's Mode to External sine wave.



6. Before configuring a Long Range PHY, you must adjust the selected radio profile for the project. On the Navigation Panel, click Protocol Configuration. You should see the General Settings and Channel Overview cards open in the editor window on the right.
7. On the General Settings card, click the Select radio profile drop-down field, and select Long Range Profile.

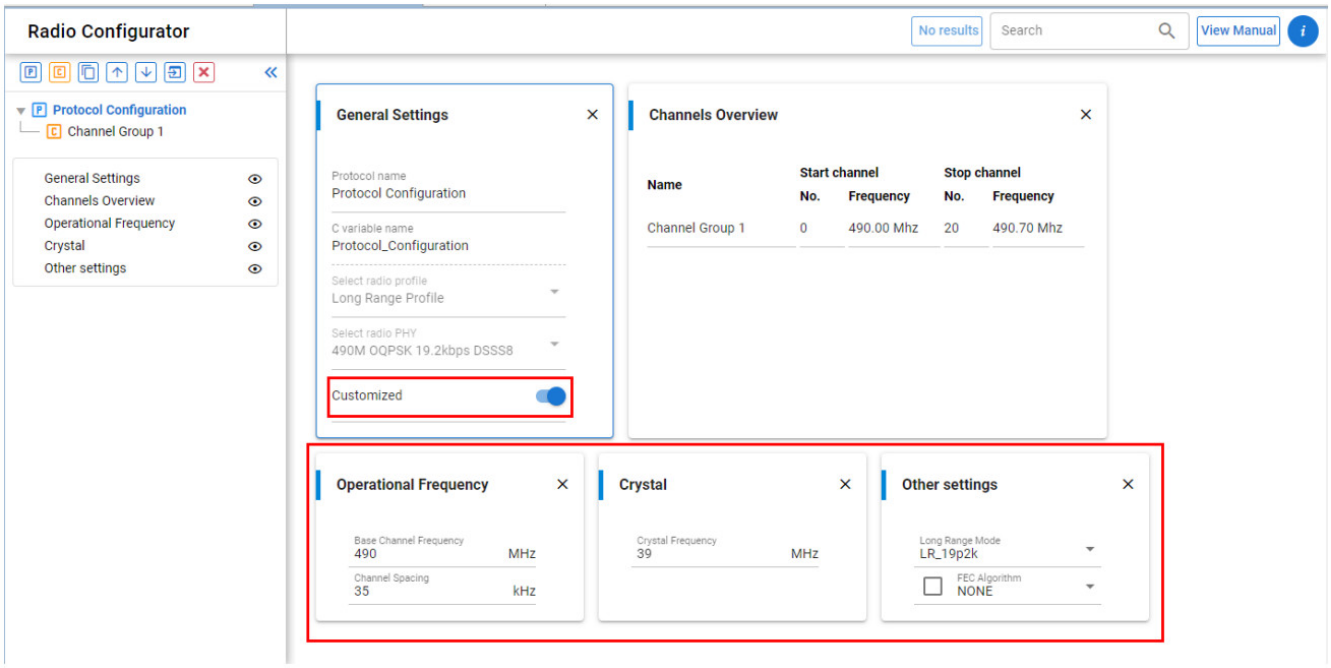


8. On the Select radio PHY field, choose one of the predefined long range configurations, keeping the following guidance in mind:
   • For 434-490 MHz boards, select a 490 MHz config.
   • For 868-915 MHz boards, select a 915 MHz config.

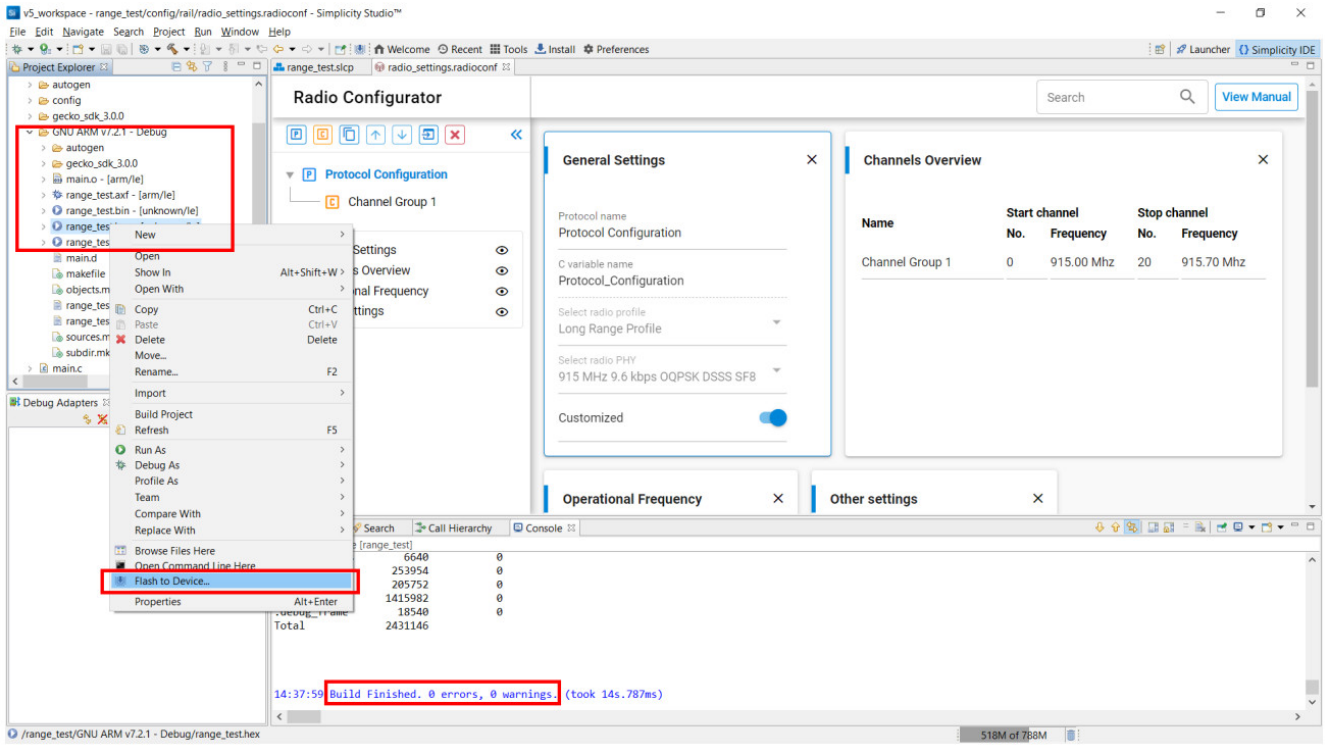


9. Enable the Customized switch to allow fine tuning of the selected PHY config.
10. On the Operational Frequency card, set the Base Channel Frequency according to your planned operating band.
11. On the Crystal card, set the XO frequency.
12. On the Other settings card, you have the option to override the data rate selection and/or to enable FEC.

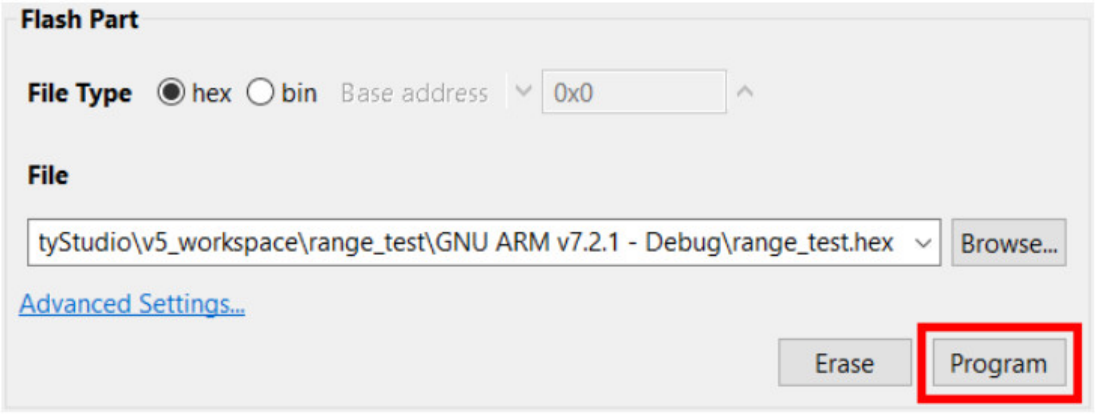
(**Note:** On an EFR32, enabling FEC doubles the number of transmitted symbols after the sync word, but does not automatically adjust the data rate. To retain the original (before enabling FEC) effective throughput with FEC, you must manually select a doubled data rate.)



13. Build the project by clicking the hammer toolbar button.
14. Once built, flash the generated hex file to the target by right-clicking the <project name>.hex file in the “GNU ARM v7.2.1 – Debug” folder, and selecting Flash to Device…



15. The Flash Programmer will open. Click Program to download the code to the target.



16. Now flash the same .hex file to your second radio board. Select the other WSTK mainboard as the target device, and click Program.

Measured Performance of the Long Range PHYs on FG23

4.1 Conducted Testing

The following table presents the following measurement results collected on real silicon with the PHYs available in the LR Profile:

- Receiver sensitivity corresponding to 1% packet error rate (PER) with 22 byte payload (CRC incl.)
- No FEC applied due to the short payload
- Similar or better sensitivity numbers can be expected on FG25 and FG28 for the current LR profile PHYs
- Overall required link (Rx + Tx) XO accuracy requirement calculated from frequency offset tolerance captures with wanted signal at 3 dB above sensitivity level
- 0.5 ppm, 39 MHz TCXO was used on our dev boards listed in Table 2-2. Radio Boards Used During Testing used during testing

Table 4-1. LR PHY Parameters

Frequency Band [MHz]	Data Rate[kbps]	Measured Sensitivity [dBm]	(TX + RX) XO Accuracy [ppm +/-]
434/490	1.2	-131.5	2.5
434/490	2.4	-129	5
434/490	4.8	-126	10
434/490	9.6	-123	20
434/490	19.2	-120	40
868/915	2.4	-128	2.5
868/915	4.8	-125	5
868/915	9.6	-122	10
868/915	19.2	-119.5	20
868/915	38.4	-116.5	40
868/915	80	-113.5	80

The following tables present basic blocking performance metrics for the 4.8 kbps and the 80 kbps LR PHYs as reference, measured with CW tone as interferer with wanted signal at 3 dB above sensitivity levels. The accuracy of the results is <= +/- 1 dB.

Table 4-2. CW blocking performance of 4.8 kbps LR PHY @ 915 MHz

	CW blocker offset [MHz]							
PER [%]	1	-1	3	-3	10	-10	20	-20
<= 1	79 dB	80 dB	87 dB	87 dB	87 dB	86 dB	88 dB	88 dB
>= 95	85 dB	85 dB	92 dB	92 dB	92 dB	92 dB	94 dB	94 dB

Table 4-3. CW blocking performance of 80 kbps LR PHY @ 915 MHz

	CW blocker offset [MHz]							
PER [%]	1	-1	3	-3	10	-10	20	-20
<= 1	54 dB	65 dB	71 dB	73 dB	76 dB	76 dB	77 dB	77 dB
>= 95	58 dB	69 dB	74 dB	77 dB	82 dB	82 dB	84 dB	84 dB

Note: the 80 kbps PHY, as all others, has a spreading factor of 8, resulting in a 640 kcps with an Rx BW of 800 kHz. The IF frequency is 450 kHz, injection side is high-side, therefore the image frequency is located at 900 kHz above the carrier. This means that we have a ~800 kHz wide region around 900 kHz above the carrier where the image rejection performance is the dominant factor in blocking performance This explains the asymmetric results at +1 / -1 MHz.

As a reference, packet error rate-based waterfall and frequency offset tolerance curves are provided in the following two figures for the 4.8 and 19.2 kbps PHYs in the 490 and 915 MHz bands.

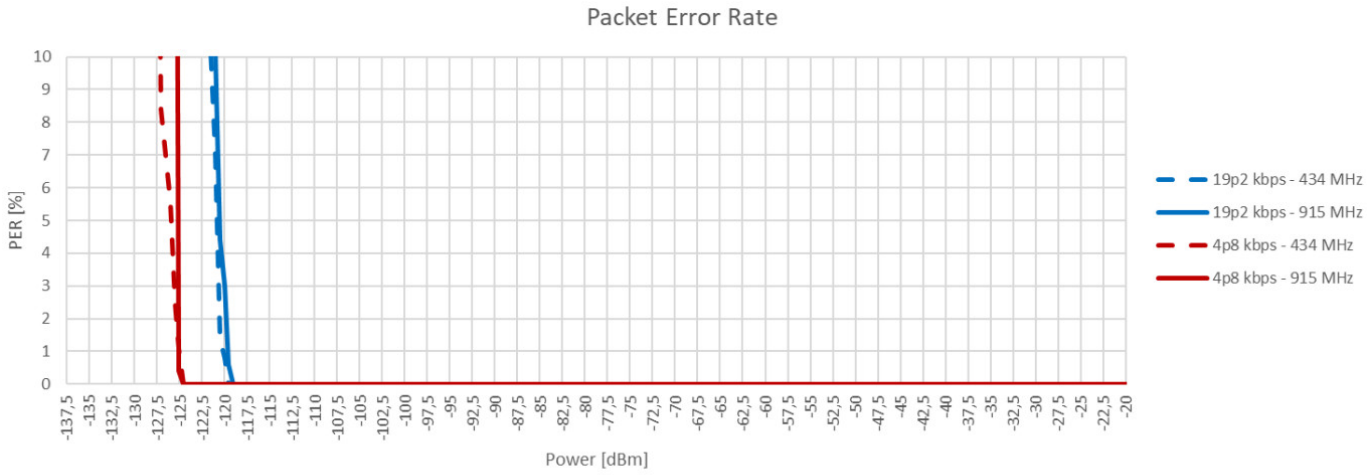


Figure 4-1. LR PHY Packet Error Rate (PER) Waterfall Curves

In the offset tolerance capture below, wanted signal was at sensitivity level and TCXO – generator residual frequency offset was compensated.

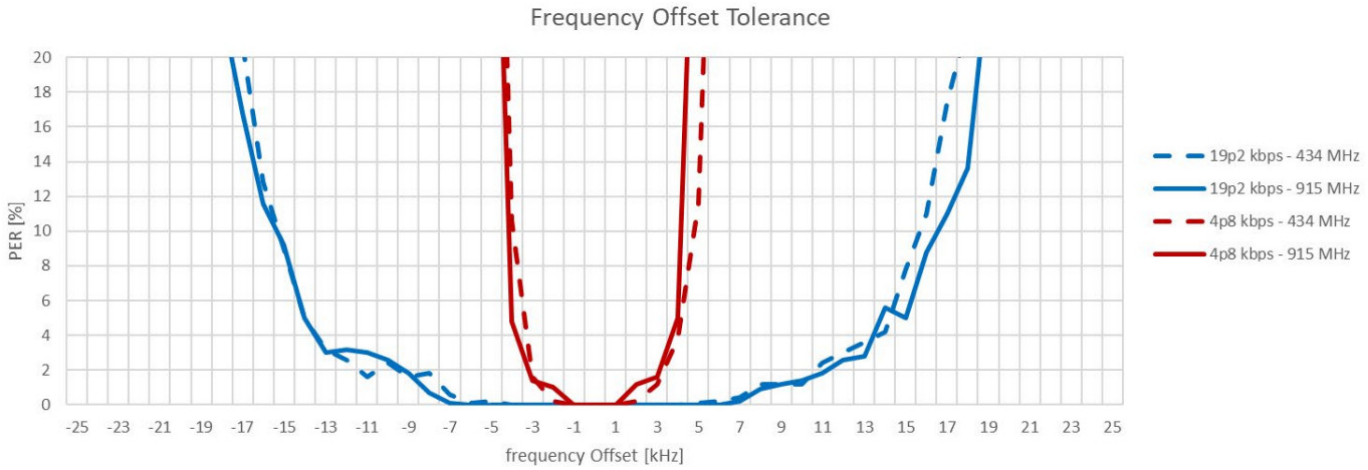


Figure 4-2. LR PHY Frequency Offset Tolerance Measurement Results at Sensitivity Level

Note: in general, the expected tolerable frequency offset across LR PHYs, at 3 dB above sensitivity levels is +/- symbol rate in Hz. For example, the 4.8 kbps PHY should tolerate +/- 4.8 kHz frequency offset with wanted signal at 3 dB above sensitivity level. The required XO accuracy reflects this fact.

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