SEQUANS COMMUNICATIONS CA410A M.2 Model Owner's Manual

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SEQUANS COMMUNICATIONS CA410A M.2

Power Supply Connection

Connect the VBAT, SIM_VCC, USB, and UART power supply pins to the corresponding power sources within the specified voltage ranges.

(U)SIM Signals Connection

Connect the (U)SIM signals including SIM_RST, SIM_CLK, SIM_IO, SIM_VCC, and SIM_DETECT according to the pin configuration provided in the manual.

USB Signals Connection

Connect the USB signals USB_D+ and USB_D- to the appropriate USB ports with a supply voltage of 3.3V.

UART Signals Connection

Connect the UART signals UART0_SOUT and UART0_SIN to the UART interface with a supply voltage of 1.8V.

Power

Table 5: Power Pads Operational Values

Pin	Name	Supply	Dir.	Min Value	Typical Operational Value	Max Value	
						3GPP RF Compliant	5 Functional
2, 4, 70, 72, 74	VBAT	N/A	In	3.2 V	3.3 V	4.4 V	4.6 V
36	SIM_VCC 4	1.8 V	Out	1.62 V	1.8 V	1.98 V	
		3.0 V		2.7 V	3.0 V	3.3 V	

(U)SIM

Table 6: (U)SIM Signals

Pin	Name	Supply	Direction
30	SIM_RST	1.8 V/3.0 V	Out
32	SIM_CLK	1.8 V/3.0 V	Out
34	SIM_IO	1.8 V/3.0 V	In/Out
36	SIM_VCC 6	1.8 V/3.0 V	Out
66	SIM_DETECT 7	1.8 V	In

USB

Table 7: USB Signals

Pin	Name	Supply	Direction
7	USB_D+	3.3 V	In/Out
9	USB_D-	3.3 V	In/Out

UART

Table 8: UART Signals

Pin	Name	Supply	Direction	8 Pad type	Reset State
63	UART0_SOUT	1.8 V	Out	BIDIR_PU	OUTPUT
65	UART0_SIN	1.8 V	Out	BIDIR_PU	INPUT

4. See also Section (U)SIM.

5. Functional behavior of the module with possible degradation of RF performances.

6. See range of values in Table 5.

7. SIM_DETECT is active HIGH (HIGH when a card is present, LOW when no card is present)

8. UART pad types are BIDIR_PU as detailed in Table 12. All their electrical characteristics are detailed in Table 13.

Non Interfacing Signals

Table 9: Non Interfacing Signals

Pin	Name	Supply	Direction	9 Pin Type	Output Class	Reset State	Default Setting
6	MODULE_PWR_EN	VDD_PWR_EN (see Table 11)	In	N/A	N/A	N/A	N/A
10	NETWORK_LED_N	1.8 V	Out	BIDIR_PU	4 mA	INPUT	INPUT, PULL-UP
23	WAKE_ON_WAN_N (see below)	1.8 V	Out	See below	N/A	N/A	N/A
67	RESET_N (see below)	1.8 V	In	N/A	N/A	N/A	N/A

RESET_N Active low (RESET). This signal is used to reset the module.

The following timing requirement applies to the signals VBAT1, MODULE_PWR_EN and RESET_N. It must be respected for proper module behaviour.

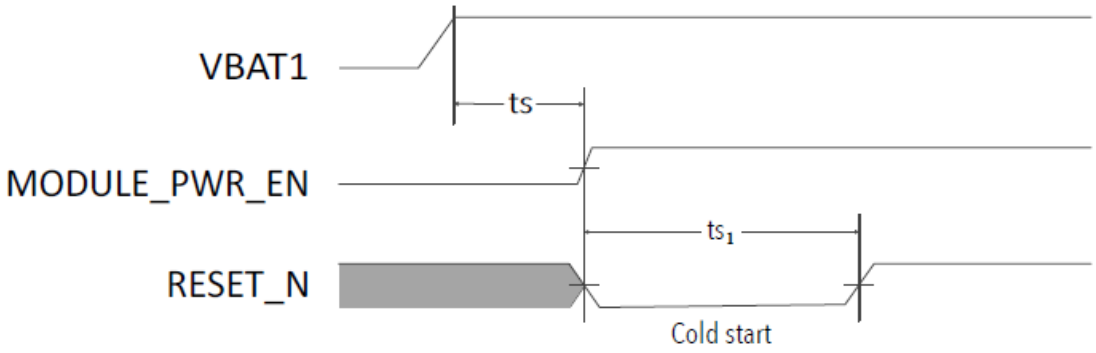

Figure 4: VBAT1, MODULE_PWR_EN and RESET_N Signals Timing Requirement for Cold Start

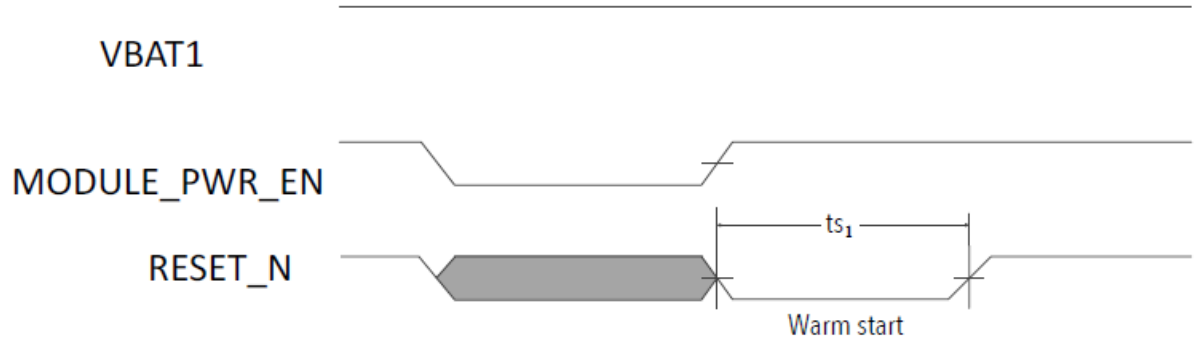

Figure 5: VBAT1, MODULE_PWR_EN and RESET_N Signals Timing Requirement for Warm Start

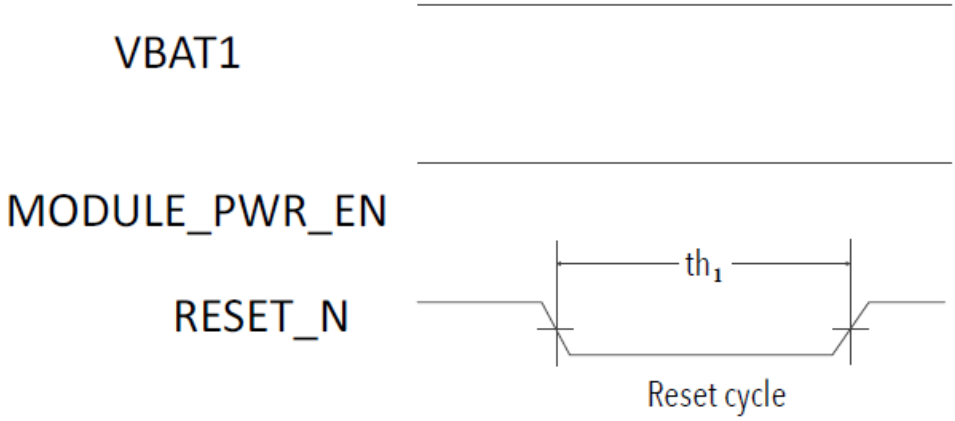

Figure 6: VBAT1, MODULE_PWR_EN and RESET_N Signals Timing Requirement for Reset Cycle

Table 10: VBAT1, MODULE_PWR_EN and RESET_N Timing Values

Symbol	Description	Minimum Duration	Maximum Duration
ts	VBAT1 setup time	0 ms	–
ts1	RESET_N setup time	1 ms	–
th1	RESET_N hold time	1 µs	–

WAKE_ON_WAN_N Open drain, active low. This pad wakes up the host. Requires a 10 kΩ pull-up resistor on host side. If unused, do not connect.

If the host does support USB suspend-resume but not remote wake-up function, the WoWWAN# M.2 signal is needed to wake up the host.

Table 11: DC Characteristics for MODULE_PWR_EN, Voltage VDD_PWR_EN

Parameter	Min.	Nom.	Max.	Unit
VIL Input Low Voltage	-0.3		0.4	V
VIH Input High Voltage	1.1		VBAT	V

Interfaces Description for the LCC Model

Data for the LCC model will be provided in a future edition of this document.

Digital I/O Characteristics

The voltage and current characteristics of the various I/O pads of the CA410 are given in the tables below.

Table 12 details the various pad types listed in CA410 signals list.

Table 12: Pad Types Detail

Pad Type	Description	Maximum Input High Voltage
Analogue	Analogue (or power for powers and ground for grounds)	Not Applicable
BIDIR_PD	1.8 V in/out with software controlled internal pull- down. Refer to Table 13 for DC I/O characteristics.	VIH max = 3.6 V
BIDIR_PU	1.8 V in/out with software controlled internal pull- up. Refer to Table 13 for DC I/O characteristics.	VIH max = 3.6 V
IN	1.8V input.	VIH max = 3.6 V

Pad Type	Description	Maximum Input High Voltage
IN_PD	1.8 V input with software controlled internal pull- down. Refer to Table 13 for DC I/O characteristics.	VIH max = 3.6 V
IN_PU	1.8V input with software controlled internal pull-up.	VIH max = 3.6 V
OUT	1.8 V output. Refer to Table 13 for DC I/O characteristics.	VIH max = 3.6 V

Refer to CA410 pin list for the type of I/O pad used on every termination.

- The Minimum values for IOL and IOH should not be exceeded to guarantee that the logical level are not spoiled for each pad type.
- The Nominal values for IOL and IOH represent the nominal values for the pad type. They are provided for information only.
- The Maximum values for IOL and IOH represent the maximal values for the pad type. They are provided for information only.

Table 13: DC Characteristics for Digital I/Os, Voltage 1.8 V

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
VIL Input Low Voltage		-0.3		0.63	V
VIH Input High Voltage		1.17		3.6	V
VT Threshold Point		0.79	0.87	0.94	V
VT+ Schmitt Trigger Low to High Threshold Point		1	1.12	1.22	V
VT- Schmitt Trigger High to Low Threshold Point		0.61	0.71	0.8	V
VT PU Threshold Point with Pull-up Resistor Enabled		0.79	0.86	0.93	V
VT PD Threshold Point with Pull-down Resistor Enabled		0.8	0.87	0.95	V
VT+ PU Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled		1	1.12	1.21	V
VT- PU Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled		0.61	0.7	0.8	V
VT+ PD Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled		1.01	1.13	1.23	V

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
VT- PD Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled		0.62	0.72	0.81	V
II Input Leakage Current @ VI=1.8V or 0V				±10	µA
IOZ Tri-state Output Leakage Current @ VO=1.8V or 0V				±10	µA
Input Capacitance			3		pF
RPU Pull-up Resistor		56	89	148	kΩ
RPD Pull-down Resistor		52	90	167	kΩ
VOL Output Low Voltage				0.45	V
VOH Output High Voltage		1.35			V
IOL Low Level Input Current at VOL(max)	2 mA	1.2	2.2	3.6	mA
	4 mA	2.3	4.3	7.1	mA
	8 mA	4.6	8.6	14.3	mA
IOH High Level Output Current at VOH(max)	2 mA	1.0	2.4	4.6	mA
	4 mA	2.0	4.7	9.2	mA

	8 mA	4.0	9.4	18.4	mA

Reliability and Radio performance

Reliability Figures

The reliability test plan for the CA410 comprises the steps below:

Item	DQA Test Stress Conditions	Standards	Results
Pro-con		JESD22-A113	*
TC 1000	Temperature Cycling (TC): -40°C to +85°C Air to air 23 min Ramp rate 20°C / min 1000 cycles	JESD22-A104	*
THB	Temperature Humidity Bias Test: 85°C, 85% RH Vcc max 1000 h +168/-24 h	JESD22-A101	*
Environmental Testing A Cold	Environmental Testing – Test A Cold -40 °C, 96 h	IEC60068-2-1	*
Environmental Testing B Dry Heat	Environmental Testing – Test B Dry Heat +85 °C, 1000 h	IEC60068-2-2	*
HTOL	High Temperature Operation Test: 75°C Vcc max Tx: 50% and Rx: 50% 283 h	N/A	*
HTS	High Temperature Storage Test: +85°C, 1000 h	IEC60068-2-2	*

LTS	Low Temperature Storage Test: -40°C, 1000 h	IEC60068-2-1	*
Micro Analysis (MA)	Micro analysis X-ray SAT, CSA TC = 0 TC = 1000 cycles	N/A	*
Shock	Mechanical Shock (MS): Half Sine 500 m/s2 11 ms 6 shocks (one for each ± axis)	DIN IEC68-2-27	*

1. Bake: 125°C / 24 h
2. MSL3: 30°C / 60% RH, 192 h
3. SAT (CSAM & TSCAN)
4. X-ray
5. Reflow 3 cycles @ Tp: 250 ± 2°C
6. SAT (CSAM & TSCAN)

Reliability and Radio performance RF Performance

Item	DQA Test Stress Conditions	Standards	Results
Drop	Drop Test:	DIN IEC68-2-31 ETS 300019-2-7	*
Vibration	Vibration Test (Vib): Sweep-Sine Vibration: Sinusoidal 10 to 500 Hz 1.0 octave/min 10 sweep cycles for 2h on each axis (X, Y, Z)	DIN IEC68-2-6 EIA/TIA 571 §4.1.1.2	*
Human Body Model ESD	TA = 25 °C ± 1000 V → ± 2000V	JS-001 JESD 22-A114	*
Charged Device Model ESD	TA = 25 °C ± 250 V→ ± 500 V	JS-002 STM5.3.1	*
Dimensions	Package Physical Dimensions (including ‘warpage’)	N/A	*
TCT	Temperature Change Test: 10 cycles One cycle follows these steps (roughly 7+ h): Ramp ambient (23°C) to -40°C at 3°C / min 3 h at -40°C Ramp to 85°C at 3°C / min 3 h at 85°C Ramp 85°C to 23°C at 3°C / min	IEC60068-2-14	*
Drop (Transportation)	Free Fall: 1 corner 3 edges and 6 faces at a height of 76 cm.	ASTM D5276	*

1. Height: 80 cm
2. Concrete or steel

3. All surfaces and edges

*: All results will be included in a future version of this document.

RF Performance

The RF performance figures of the CA410 M will be given in a future edition of this document.

Power Consumption

The power consumption figures for the CA410 M will be given in a future edition of this document.

Mechanical Characteristics

Device Marking

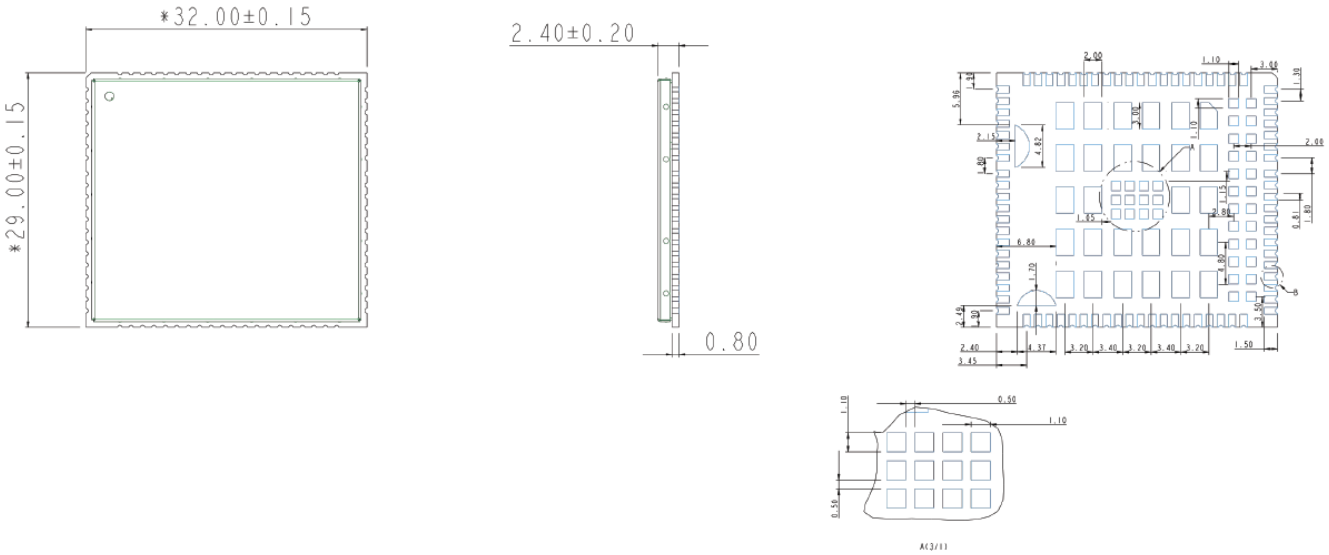

Figure 10: CA410 Shield Marking Description

The elements marked on the package are:

- Sequans’s logo
- CA410 product name
- Cassiopeia platform name
- RoHS logo
- FCC ID: 2AAGMCA410A
- IC/ISED: 12732A-CA410A
- IMEI as digits and QR code
- The module Serial Number as digits and QR code:
    - VVV: 4MA
    - YYMMDD: Manufacturing date

- LLLL: tracking batch number
- SSS: three-digits serial number (HEX format 000 to FFF)

- Manufacturing country (VN: Vietnam)

M.2 Device

1. Mechanical Characteristics

Figure 8: Mechanical Description

The dimensions shown in Figure 8 are in millimeters.

The CA410 M.2 complies to the M.2 specification, type 3042-S3-B.

2. Packing

The CA410 M.2 is delivered in tray. One tray can hold up to 40 pieces. 1 box can contain 10 trays, thus up to 400 pieces. This is represented on Figure 9.

Figure 9: CA410 M.2 Packing

LCC Device

1.Mechanical Characteristics

Figure 10: Mechanical Description

The dimensions shown in Figure 10 are in millimeters.

2. Packing

The CA410 LCC is delivered in reels. One reel can hold up to 500 pieces. 1 box can contain 2 reels, thus up to 1000 pieces. This is represented on Figure 11.

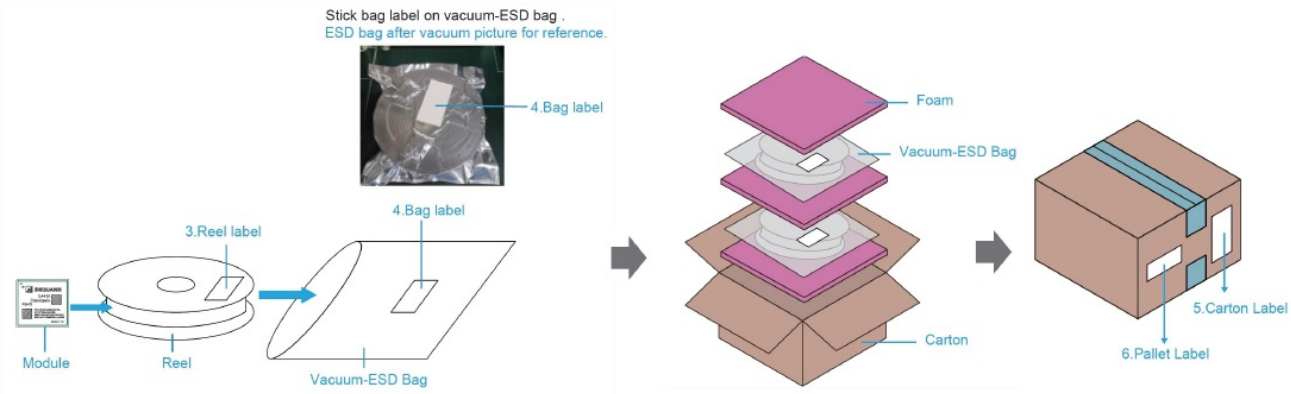

Figure 11: CA410 LCC Packing

Figure 11: CA410 LCC Packing

Specifications

- RF Connector: FoxconnTM KK12011-02-7H
- Power Supply:
  - VBAT: 1.8V to 3.3V
  - SIM_VCC: 1.8V to 3.0V
  - USB: 3.3V
  - UART: 1.8V
- (U)SIM Signals:
  - SIM_RST, SIM_CLK, SIM_IO, SIM_VCC, SIM_DETECT
  - Supply: 1.8V/3.0V
- USB Signals:
  - USB_D+, USB_D-
  - Supply: 3.3V
- UART Signals:
  - UART0_SOUT, UART0_SIN
  - Supply: 1.8V

FAQ

What is the purpose of the WAKE_ON_WAN_N signal?

The WAKE_ON_WAN_N signal is an open drain, active low signal that wakes up the host. It requires a 10k pull-up resistor on the host side. If unused, it should not be connected. This signal is necessary to wake up the host if the host supports USB suspend-resume but not remote wake-up function.

Documents / Resources

	SEQUANS COMMUNICATIONS CA410A M.2 Model [pdf] Owner's Manual CA410A M.2 Model, CA410A, M.2 Model, Model

References

- User Manual