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ROHM LogiCoA001-EVK-001 Synchronous Buck DCDC Converter Evaluation Board



## **Specifications**

 Product Name: LogiCoATM Power Solutions Synchronous Buck DCDC Converter Evaluation Board

Model: LogiCoA001-EVK-001

Input Voltage: 12VOutput Voltage: 5V

• Output Current: 5A

#### Introduction

LogiCoATM Power is a solution adopting analog-digital hybrid control to a switching power supply. This user's guide will provide the steps necessary to operate the evaluation board of LogiCoATM Power Solution Synchronous buck DCDC converter, LogiCoA001-EVK-001. Bill of materials, operating procedures and application data are included.

"LogiCoATM" is a trademark or a registered trademark of ROHM Co., Ltd.

## Overview of LogiCoATM Power Solution

Figure 1-1 shows the overview of LogiCoATM Power Solution. LogiCoATM Power is a solution adopting analog-digital hybrid control to a switching power supply and consists

from 3 elements, (1) Microcontroller for Power Supply Control (LogiCoATM Microcontroller) ML62Q203x/ML62Q204x (hereinafter referred to ML62Q20xx group), (2) Operating System for Power Supply Control Microcontroller, RMOS, and (3) Power Supply Application. Refer to the explanation application note [1] for detail information of analog-digital hybrid control.

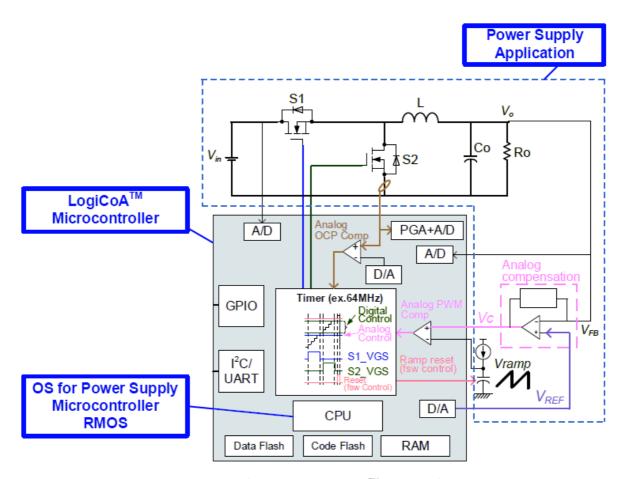


Figure 1-1. System overview of LogiCoA<sup>TM</sup> Power Solution

## 1. Microcontrollers for Power Supply Control (LogiCoATM Microcontroller)

LogiCoATM Microcontrollers are suitable ones for power supply control with those analog-digital hybrid control is adopted and ML62Q2033/2035 and ML62Q2043/2045 are released. (at the time of this document's release) On this EVK, ML62Q2035 is mounted. Refer to 4.2 MCU, the datasheet of ML62Q2033/2035/2043/2045 [2] and the user's manual of ML62Q2033/2035/2043/2045 [3] for more detail information about ML62Q2035.

# 2. Operating System for Power Supply Control Microcontroller RMOS (Real time Micro Operating System)

RMOS is a multi-task and real-time operating system developed to control switching power supplies and operates on ML62Q20xx group. Refer to the explanation

application note [4] for more detail information about RMOS.

## 3. Power Supply Application

Power Supply Applications are application circuits correspond to each power supply topology. On this EVK external components such as LDO, gate driver, operational amplifier, MOSFET inductor and so on are mounted as an application circuit of synchronous buck converter.

## **Operating Conditions**

(Unless otherwise specified Ta=25°C, Vin=12V)

Parameter	Symb	Min	Тур	Max	Un it	Conditions
Input Voltage	Vin	7.5	12. 0	38. 0	V	
Control Block Supply Volta ge(LDO)	Vcc5 Vldo	4.9	5.0	5.1	V	Vcc5V=LDO Output
Control Block Supply Volta ge(USB)	Vcc5 Vusb	4.2 5	5.0 0	5.7 5	V	Vin=open, Vcc5V=US B VBUS Output
Driver Block Supply Voltag	Vcc12 V	11. 4	12. 0	12. 6	V	Vin>13V
Output Voltage	Vo	_	5.0	_	V	default setting, variable with serial co mmunication
Output Voltage Range	Vo_r	1.0	_	8.0	V	variable with serial co mmunication
Output Current	lo	_	_	5.0	Α	

Switching Frequency	fsw	_	160	_	kH z	default setting
Switching Frequency Rang	fsw_r	80	_	500	kH z	
Maximum Duty	Dmax	_	80	_	%	default setting
Soft Start Time	Tsstar t	_	5	_	ms	Io=0A
Efficiency	η	_	92	_	%	Vo=5V, Io=5A
Startup Voltage	Vstart	_	9.0	_	V	Vin rise, default setting , variable with serial co mmunication
Startup Voltage Range	Vstart _r	7.5	-	38. 0	V	
Stop Voltage	Vstop	_	8.0	_	V	Vin fall, default setting, variable with serial co mmunication
Stop Voltage Range	Vstop _r	7.5	_	38. 0	V	
Startup Delay Time	Tstart	_	100 0	_	ms	Vin rise, default setting
Startup Delay Time Range	Tstart _r	10	_	_	ms	

Input Voltage Protection	Vivp	_	38. 0	_	V	default setting
Input Voltage Protection R ange	Vivp_	7.5	_	38. 0	V	
Over Current Protection	locp	_	6.0	_	Α	default setting
Over Current Protection R ange	locp_r	2.5	_	8.0	A	
Output Low Voltage Protection	Vlvp	_	3.0	_	V	Vo fall, default setting
Output Low Voltage Protection Range	VIvp_	1.0	_	7.0	V	
Output Low Voltage Protection Mask Time	Tlvp	_	500	_	ms	Vo fall, default setting
Output Low Voltage Protection Mask Time Range	Tlvp_r	10	_	_	ms	
Output Over Voltage Prote ction	Vovp	_	6.0	_	V	Vo rise, default setting
Output Over Voltage Prote ction Range	Vovp_	1.0	_	10. 0	V	

## **Firmware**

For this EVK, in addition to the evaluation board, the source code of RMOS and power supply control are supplied. And those can be downloaded from the URL below.

Table 3-1. RMOS download URL and the file name

Download URL <a href="https://www.rohm.com/reference-designs/ref66009">https://www.rohm.com/reference-designs/ref66009</a>	
--	--

Reference Program Name	LogiCoA <sup>TM</sup> Solution Buck Converter Reference Program
File Name	RMOS100-PSFW001.zip

## **Block Diagram and Description**

## **Block Diagram**

Figure 4-1 shows the application block diagram of this EVK.

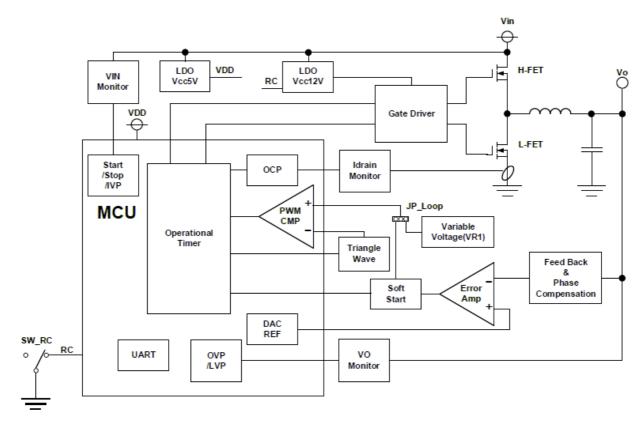


Figure 4-1. Application Block Diagram

#### **MCU**

On this EVK, MCU ML62Q2035 is mounted as a power supply controller. VDD voltage of MCU is supplied from the control block power supply Vcc5V, and after supplied voltage becomes over 4.10V (typ) of the threshold voltage of POR, the microcontroller startup and RMOS starts its operation. Each pin's function of ML62Q2035 and selected function in this EVK is listed in Table 4-1.

#### Table 4-1. Pin list of ML62Q2035

Pin N	Pin Na	1 <sup>st</sup> Fu nction	2 <sup>nd</sup> Fu	3 <sup>rd</sup> Fu	4 <sup>th</sup> Fu	5 <sup>th</sup> Fu	6 <sup>th</sup> Fu	7 <sup>th</sup> Fu	8 <sup>th</sup> Fu
0.	me	GPI/E XI	UART	I <sup>2</sup> C	ОТМ	CMP/ DAC	ADC	СМР	CMP/ ADC
19	VDD	_	_	_	_	_	_	_	_
18	VSS	_	_	_	_	_	_	_	_
17	VDDL	_	_	_	_	_	_	_	_
16	P01	_	_	_	_	CMP0 P	_	CMP0 P /CMP 1P	CMP0 P
15	P02	_	_	_	OTO4 B	CMP0 M	_	CMP0 M /CMP 1M	CMP0 M
14	P03	EXI0	_	_	OTO0 A	_	_	_	_
13	P04	EXI1	_	_	OTO0 B	_	_	_	_
12	P05	EXI1	_	_	OTO1	_	_	_	_
11	P06	EXI2			OTO2 A				

10	P10	EXI3	RXD1 , (/TXD 1)	_	ОТОЗ		_		
9	P11	_	_	_	OTO4 A	CMP2	_	CMP2	CMP2
8	P12	_	RXD0 , (/TXD 0)	SDAU 0	OTO1	_	_	_	_
7	P00/T EST0	EXI3	_	_	_	_	_	_	_
6	P13	EXI2	TXD0	SCLU 0	ОТО5 В	_	AIN4	_	_
5	RESE T_N	_	_	_	_	_	_	_	_
4	P14	_	_	_	_	CMP1	AIN0	CMP1 P /CMP 2P	AIN0 /CMP 1P
3	P15	_	_	_	_	CMP1	AIN1	CMP1 M /CMP 2M	AIN1 /CMP 1M

									AIN2
2	P16	_	_	_	_	CMP2 M	AIN2	CMP2 M	/CMP 2M
1	P17	EXI0	_	_	_	_	AIN3	_	_
20	P23	_	TXD1	_	OTO5	DACO UT0	_	_	_

Table 4-2 listed the typical specifications of ML62Q2035. Refer to [2] and [3] for more detail information about ML62Q2035.

Table 4-2. Typical specifications of ML62Q2035

Part Number	ML62Q2035
CPU	16bit RISC CPU Core(nx-U16/100), Max operating frequenc y 16MHz
Memory	Code Flash: 32KB, Data Flash: 4KB(Erase Unit:128B), RAM : 2KB
Analog Comparator	3ch(asynchronous to clock), Response time: Max 100ns
Timer	16bit timer with PWM/Capture × 6 counters, 10 outputs
Timei	Max 64MHz operation(Resolution 15.625ns)
AD Converter	12bit SA-ADC: 5ch
DA Converter	8bit, 2ch
Programmable Gain A mplifier	1ch, Gain Setting: 4 steps (×4/×8/×16/×32)
Serial I/F	I <sup>2</sup> C×1, UART×2

I/O Port		I: 1, I/O: 15				
External I	nterrupt	4				
Other		Multiplication/Division Unit, Temperature Sensor, Power ON Reset				
	Low	Internal RC Oscillator: 32.768kHz ± 1.5%*				
Clock	Lliah	PLL: 64MHz ± 1.5%*, CPU: 16MHz to 125kHz ± 1.5%*				
	High	PWM/Capture: 64MHz to 500kHz ± 1.5%*				
Current C	onsumption(	Stop: 80μA, Halt: 90μA, Active: 3.3mA@16MHz				
Operating Supply Volta		4.5V to 5.5V				
Operating Temperature		Ta=-40°C to +105°C(Tj=115°C) (Absolute maximum ratings:Tjmax=125°C)				
Package		TSSOP20				

## **Control Block Power Supply**

On this EVK, a fixed 5V output LDO BD950N1WG-C is mounted as a power supply (Vcc5V) for control block (MCU and analog control circuit). BD950N1WG-C has standby control function, but in this EVK, VIN pin and EN pin are shorted and so when Vin voltage is applied and VIN pin of BD950N1WG-C voltage is over UVLO rise voltage (typ 2.6V), Vcc5V turns on. Refer to the datasheet of BD9xxN1-C series [5] for more detail information about BD950N1WG-C.

## **Driver Block Power Supply**

On this EVK, a 12V output LDO BD900N1WG-C is mounted as a power supply (Vcc12V) of the gate driver to drive output FET. BD900N1WG-C has standby control function and can be controlled turning ON/OFF by a remote control switch described later. Refer to the datasheet of BD9xxN1-C series [5] for more detail information about BD900N1WG-

#### **Remote Control Switch**

This EVK has RC (RC: Remote Control) function for external turning ON/OFF control. DCDC operates as the setting below by turning the mechanical switch (SW\_RC) connected P10 pin of ML62Q2035 to OPEN or short to GND. To avoid a false detection by noise, there are mask time of 150 $\mu$ s at RC=H detection and 1.25ms at RC=L. P10 pin is set as a GPIO with internal 40 $\mu$ C(typ) pulled-up. Refer to [2] about the threshold of operating state because it depends on input/output characteristics of ML62Q2035.

Table 4-3. Operating state of Remote Control Switch

SW_RC	P10 pin	DCDC
OPEN	VDD	ON
GND SHORT	GND	OFF

## **Error Amplifier and Reference Voltage**

- Figure 4-2 shows the error amplifier and surrounding circuits. BU7481SG is mounted
  on as an error amplifier. As control block power supply Vcc5V is supplied, the error
  amplifier starts to operate but startup of the error amplifier output is controlled by the
  soft start circuit. Refer to the datasheet of that [6] for more detail information about
  BU7481SG.
- The reference voltage of error amplifier Vo\_REF is generated by the 8-bits DA converter built-in in the MCU (1.973V at VDD=5V). Output voltage Vo is calculated as following equation.

Ex.) When Vo\_REF=1.973V, R29=51 $\Omega$ , R30=3.3k $\Omega$  and R31=2.2k $\Omega$ , output voltage is as below.

$$Vo = 1.973V \times \frac{51\Omega + 3.3k\Omega + 2.2k\Omega}{2.2k\Omega} \cong 4.9782V$$

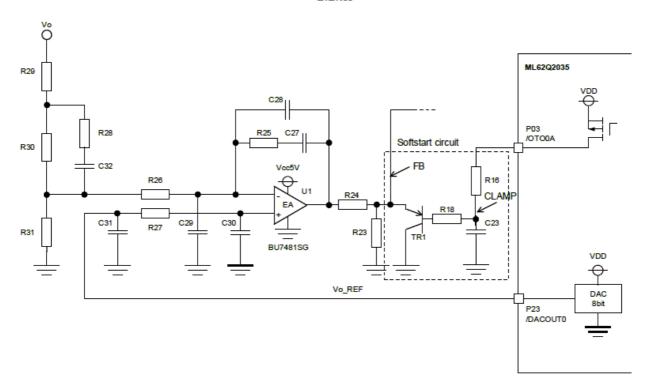


Figure 4-2. Error amplifier and surrounding circuits

#### **Soft Start**

- In this EVK, to avoid an overshoot and rush current, output of the error amplifier (FB) is clamped while starting up, thus ramp up speed of DCDC output is controlled and starts softly.
- The FB voltage is clamped by the CLAMP voltage + VBE of TR1 because the voltage generated at both ends of R18 can be considered minute due to R18=100Ω and TR1 base current. P03/OTO0A pin has been set as PMOS open drain, and while in startup, clamped voltage rise up slowly by controlling the ON duty of the PMOS. In the steady state, the CLAMP voltage is equal to VDD and thus the FB voltage is not clamped.

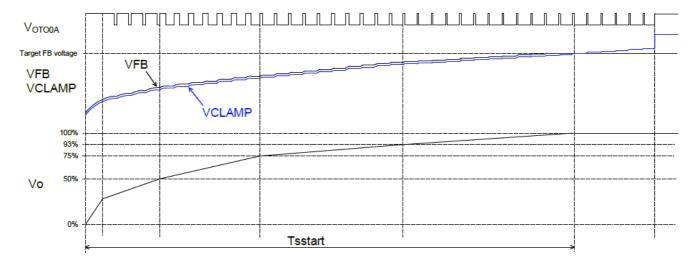


Figure 4-3. Soft start operation timing chart

## **Triangle Waveform Generator and PWM Comparator**

- Figure 4-4 and 4-5 shows the triangle waveform generator and surrounding circuits, and timing chart. Triangle waveform is generated at P02/CMP0M pin by clock pulse output from P04/OTO0B pin. P01/CMP0P pin and P02/CMP0M pin have been set as an input of analog comparator and the build-in analog comparator operate as the PWM comparator.
- As shown in Figure 4-5, the frequency of clock pulse output from P04/OTO0B pin is
  the switching frequency of the DCDC converter fsw (160kHz). And while the output of
  the clock pulse is H, the voltage of TRNGL becomes also H, so the output of the PWM
  comparator is L. This leads that the L duty of the clock pulse is the Max Duty Dmax
  (80% typ) of the DCDC converter.

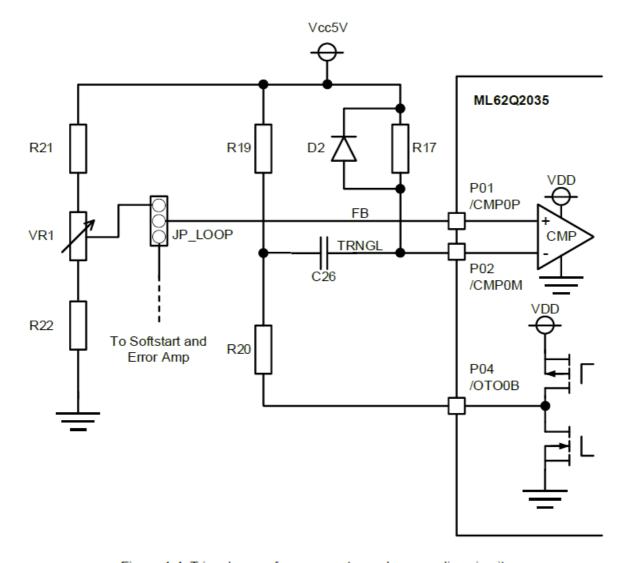


Figure 4-4. Triangle waveform generator and surrounding circuit

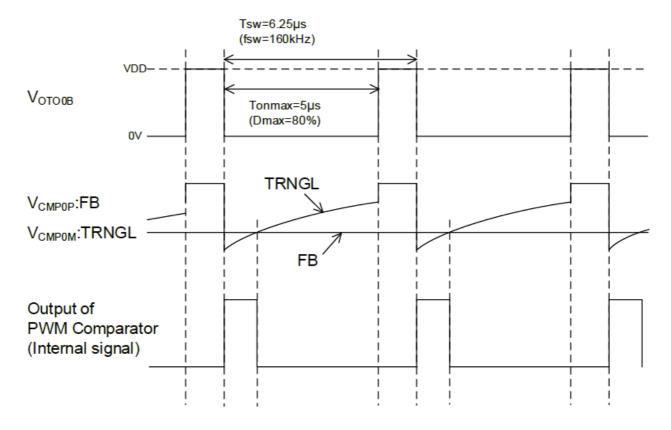


Figure 4-5. Triangle waveform generator timing chart

## Volume Resistor for open loop operation (for debug)

This EVK can be operated in open loop without feedback control for debugging. Open loop and closed loop operation can be exchanged by the jumper connection of JP\_Loop (refer to Figure 4-1. Application Block Diagram and Figure 4-4. Triangle waveform generator and surrounding circuit.) When open loop operation is selected, the input voltage of the PWM comparator can be tuned using volume resistor VR1. The divided voltage from Vcc5V by R21 and  $10k\Omega$  volume resistor VR1 will be the FB voltage ( $0\Omega$  is mounted on R22.)

## **Output Stage**

In output stage, the control signals of H-side/L-side FET from the MCU level shifted by the gate driver drive output FETs, and stable voltage smoothed by the LC filter is supplied. BD2320EFJ-LA is mounted on as a gate driver. Refer to the datasheet of that [7] for more detail information of BD2320EFJ-LA.

## **Input Voltage Detection Block**

Figure 4-6 shows the input voltage detection block. The divided Vin voltage by R6 and R7 is input to the P15/AIN1 pin of ML62Q2035, and the digital value of pin input voltage converted by the 12bits AD converter is obtained.

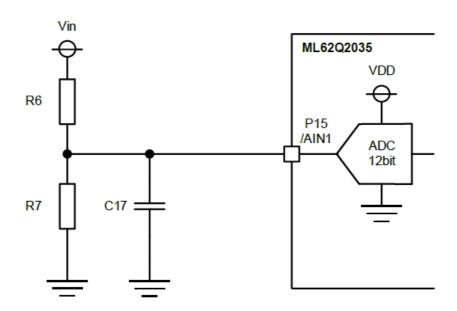


Figure 4-6. Input voltage detection block

## 1. Startup/Stop Voltage Check

In this EVK, Vin input voltage is monitored by the input voltage detection block described above and when the voltage is over the startup voltage of 9V, DCDC

startups after the 1s of the startup delay time. When the input voltage is below 8V, DCDC stops. For a noise reduction, there is a 150µs of mask time in voltage detection.

## 2. Input Voltage Protection

This EVK has an input over voltage protection function (IVP: Input Voltage Protection). Vin input voltage is monitored by the input voltage detection block described above and when the voltage is over the detect voltage of 38V, the protection works and DCDC stops output switching. For a noise reduction, there is a 250µs of mask time in voltage detection. When the input voltage is below the detect voltage in the normal operation state, count of the mask time is reset. When protection works, DCDC stops latched, and restarts after turning on RC again in the condition that Vin input voltage is under the detection threshold voltage.

## **Output Voltage Detection Block**

Figure 4-7 shows the output voltage detection block. The divided Vo voltage by R32 and R33 is input to the P14/AIN0 pin of ML62Q2035, and the digital value of pin input voltage converted by the 12bits AD converter is acquired.

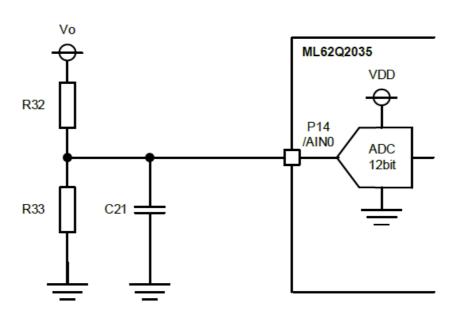


Figure 4-7. Output voltage detection block

## 1. Low Voltage Protection

This EVK has an output low voltage protection function (LVP: Low Voltage Protection). Vo output voltage is monitored by the output voltage detection block described above and when the voltage drops less than the detect voltage of 3.0V, timer count starts.

When the output voltage remains below the detect voltage and 500ms has passed, protection works and DCDC stops output switching. The timer counter is incremented from the initial value by every 500µs, and when the output voltage becomes over the detect voltage while in timer counting, the counter value is decremented. When DCDC stops by the protection or RC, the timer counter is reset. When protection works, DCDC stops latched, and restart after turning on RC again.

## 2. Over Voltage Protection

This EVK has an output over voltage protection function (OVP: Over Voltage Protection). Vo output voltage is monitored by the output voltage detection block described above and when the voltage is over the detect voltage of 6.0V, the protection works, and DCDC stops output switching. For a noise reduction, there is a 250µs of mask time in voltage detection. When the output voltage drops less than the detect voltage in the normal operation state, count of the mask time is reset. When protection works the DCDC stops latched, and restart after turning on RC again.

## **Drain Current Detection Block**

Figure 4-8 shows the drain current detection block. The drain current Id flows through low side FET, FET2, is converted to the voltage VSNS in the current sense resistor R5. VSNS divided from Vcc5V by R8, R9 and R10, R11, and added certain offset voltage to meet the input voltage range of AD converter/analog comparator, are input to P16/AIN2 pin and P11/CMP2P pin of ML62Q2035 each. By the built-in AD converter in P16/AIN2 pin, the digital value of the current is acquired and the built-in comparator in P11/CMP2P pin detect the overcurrent.

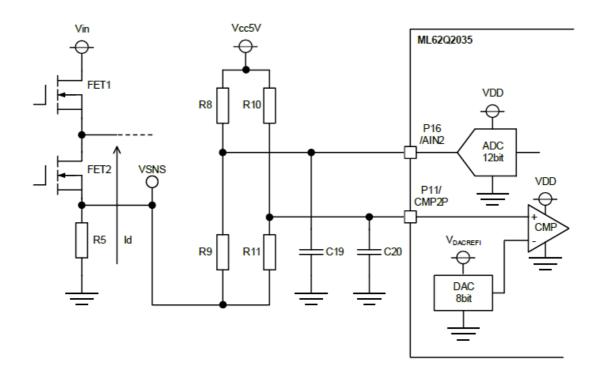


Figure 4-8. Drain current detection block

#### **Over Current Protection**

This EVK has a pulse-by-pulse over current protection function (OCP: Over Current Protection). The drain current of low side FET is monitored by the analog comparator in the drain current detection block described above. When the current exceeds the detect threshold value of 6.0A, protection works and turning off the FET. After the detection, DCDC restarts from protection automatically, but if the overload state continues, OCP is detected again.

#### **LED Indicator**

In this EVK, 2 LEDs of LED1(red) and LED2(green) are mounted on. And each blinking pattern indicates below operating state.

Table 4-4. LED1 Blinking pattern and operating state

LED1	State
Off	
Blinking	Program writing/Accessing to MCU

Table 4-5. LED2 Blinking pattern and operating state

LED2	State
1 time short blink(100ms x 1) in 1.6ms period	Vin input voltage is below startup voltage(Vin stop state)
2 times short blink(100ms x 2) i n 1.6ms period	Vin input voltage is over startup voltage and standb y with RC control(RC standby state)
1 time blink(700ms x 1) in 1.6ms period	Normal operation state
5 times short blink(100ms x 5) i n 1.6ms period	Abnormal stop state

## **Serial Communication**

In this EVK, modification of power supply control parameter and recording the operating log are capable of by a serial communication via the on-board USB-UART covert module from such as an external Windows PC. (Logging function is not implemented at the time of this document's release.) Refer to the explanation application note of communication function and GUI[8] for more detail information about the serial communication and communication commands.

#### View of EVK

Figure 6-1 and Figure 6-2 shows the view of EVK.



Figure 6-1. LogiCoA001-EVK-001(Top View)



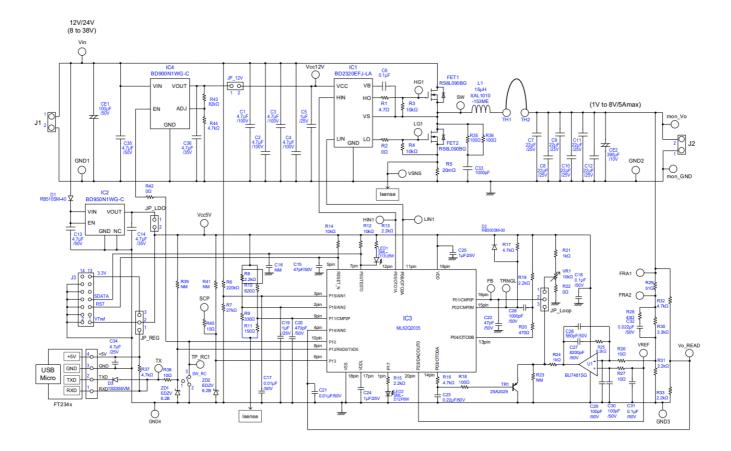
Figure 6-2. LogiCoA001-EVK-001(Bottom View)

## **Operating Procedure**

- 1. Short 1-2 pins of the jumper JP\_LDO, 1-2 pins of JP\_12V, 2-3 pins of JP\_Loop and open JP\_REG on the EVK.
- 2. Turn the SW\_RC to connect 1-2pins on EVK. (Turn the switch to upper side in the board direction of Figure 6-1.)
- 3. Turn off the DC power supply and connect it's GND pin to 2 pin of J1 on the EVK.
- 4. Connect DC power supply's VCC pin to 1 pin of J1 on the EVK.
- 5. Connect the load between 1 pin and 2 pin of J2 on the EVK. When an electric load is used, turn off the output before connecting to the board.
- 6. Connect the voltmeter to the mon Vo pin and mon GND pin on the EVK.
- 7. Turn on the DC power supply. Check if the measured value of the voltmeter is 5V.
- 8. If an electric load is used, turn on the electric load.

**Notes**: This EVK does not support hot plugging protection. Do not perform hot plugging on this board.

#### **Board Schematic**



## **Board Information and Layout**

The board information of this EVK is listed in Table 9-1.

## **Table 9-1. Board information**

Below are EVK layouts.

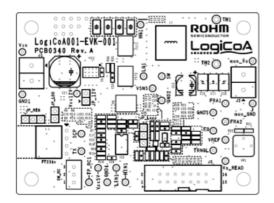


Figure 9-1. Top Silk Screen (Top View)

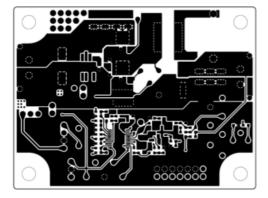


Figure 9-3. Top Layer Layout (Top View)



Figure 9-5. Middle2 Layer Layout (Top View)

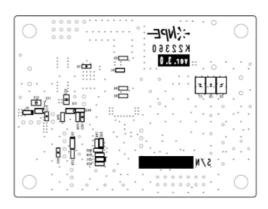


Figure 9-2. Bottom Silk Screen (Top View)

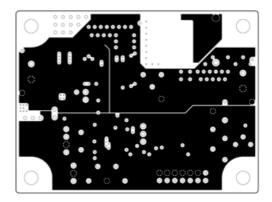


Figure 9-4. Middle1 Layer Layout (Top View)

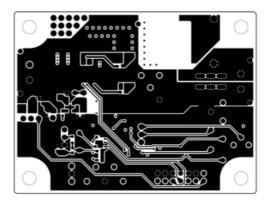


Figure 9-6. Bottom Layer Layout (Top View)

## **Bill of Materials**

Table 10-1 shows the bill of materials of this EVK.

## Table 10-1. Bill of Materials

Qu anti ty	Reference D esignator	Part Number	Manufacturer	Value	Description [Unit: inch(m m)]
IC					

1	IC1	BD2320EFJ- LAE2	ROHM	_	Gate Driver,14.5V,2024( 4960)
1	IC2	BD950N1WG -CTR	ROHM	_	LDO, 42V, 5V/150mA,11 12(2829)
1	IC3	ML62Q2035- NNNTDZWA TZ	LAPIS Techn ology	_	MCU, 5.5V, 32kbyte,252 6(6465)
1	IC4	BD900N1WG -CTR	ROHM	_	LDO, 42V, 150mA,1112( 2829)
1	U1	BU7481SG-T R	ROHM	_	1ch-OPAMP,5.5V,1112( 2829)
Resi	stor				
1	R1	_	_	4.7Ω	0.1W,±1%,0603(1608)
3	R2,R22,R42	_	_	0Ω	1A,0.1W,0603(1608)
4	R3,R4,R12, R14	_	_	10kΩ	0.1W,±1%,0603(1608)
1	R5	LTR100LJZP FSR020	ROHM	20mΩ	4W,±1%,1225(3264)
1	R6	_	_	220k Ω	0.1W,±1%,0603(1608)
1	R7	_	_	27kΩ	0.1W,±1%,0603(1608)
6	R8,R13,R15, R19,R31,R3	_	_	2.2kΩ	0.1W,±1%,0603(1608)
1	R9	_	_	330Ω	0.1W,±1%,0603(1608)

1	R10	_	_	820Ω	0.1W,±1%,0603(1608)
1	R11	_	_	150Ω	0.1W,±1%,0603(1608)
4	R16,R17,R3 2,R44	_	_	4.7kΩ	0.1W,±1%,0603(1608)
3	R18,R35,R3	_	_	100Ω	0.1W,±1%,0603(1608)
1	R20	_	_	470Ω	0.1W,±1%,0603(1608)
2	R21,R24	_	_	1kΩ	0.1W,±1%,0603(1608)
0	R23	No mount	_	_	_
1	R25	_	_	8.2kΩ	0.1W,±1%,0603(1608)
4	R26,R27,R3 8,R40	_	_	10Ω	0.1W,±1%,0603(1608)
1	R28	_	_	43Ω	0.1W,±1%,0603(1608)
1	R29	_	_	51Ω	0.1W,±1%,0603(1608)
1	R30	_	_	3.3kΩ	0.1W,±1%,0603(1608)
0	R39,R41	No mount	_	_	_
1	R43	_	_	82kΩ	0.1W,±0.5%,0603(1608)
1	R44	_	_	4.7kΩ	0.1W,±0.5%,0603(1608)
1	VR1	CT-6EP103	Nidec Copal Electronics	10kΩ	70.7V,0.5W,±10%,2828( 7070)
Capa	acitor				
4	C1,C2,C3,C 4	C3225X7S2A 475K200AE	TDK	4.7µF	100V,X7S,±10%,1210(3 225)

4	C5,C19,C24, C25	CGA3E1X7R 1E105K080A C	TDK	1μF	25V,X7R,±10%,0603(16 08)
3	C6,C18,C31	CGA3E2X7R 1H104K080A A	TDK	0.1µF	50V,X7R,±10%,0603(16 08)
6	C7,C8,C9,C 10,C11,C12	GRM32ER71 E226ME15L	Murata	22µF	25V,X7R,±20%,1210(32 25)
2	C13,C35	GRM21BR61 H475ME51L	Murata	4.7µF	50V,X5R,±20%,0805(20 12)
2	C14,C36	GRM188R6Y A475ME15D	Murata	4.7µF	35V,X5R,±20%,0603(16 08)
2	C15,C22	CC0603JRN PO9BN470	Yageo	47pF	50V,C0G,±5%,0603(160 8)
0	C16	No mount	_	_	_
2	C17,C21	GRM188B11 H103K	Murata	0.01μ F	50V,B,±10%,0603(1608)
1	C20	CGA3E2C0G 1H471J080A A	TDK	470pF	50V,C0G,±5%,0603(160 8)
1	C23	CGA3E3X7R 1H224K080A B	TDK	0.22μ F	50V,X7R,±10%,0603(16 08)
2	C26,C33	CGA3E2X7R 1H102K080A A	TDK	1000p F	50V,X7R,±10%,0603(16 08)

1	C27	CGA3E2C0G 1H822J080A A	TDK	8200p F	50V,C0G,±5%,0603(160 8)
1	C28	CGA3E2C0G 1H561J080A A	TDK	560pF	50V,C0G,±5%,0603(160 8)
2	C29,C30	CGA3E2C0G 1H101J080A A	TDK	100pF	50V,C0G,±5%,0603(160 8)
1	C32	CGA3E2X7R 1H223M080A A	TDK	0.022 μF	50V,X7R,±15%,0603(16 08)
1	C34	C1608X5R1 E475M080A C	TDK	4.7µF	25V,X5R,±20%,0603(16 08)
1	CE1	UCDH101M CL6GS	Nichicon	100µF	50V,±20%,0.36Ωmax,Φ 10
1	CE2	APXT100AR A391MF80G	Chemi-con	390µF	10V,±20%,22mΩmax,Φ 6.3
Diod	le				
1	D1	RB510SM-40 T2R	ROHM	_	40V,100mA,0603(1608)
1	D2	RB500SM-30 T2R	ROHM	_	30V,100mA,0603(1608)
1	D3	1SS355VMT E-17	ROHM	_	80V,100mA,1005(2513)

2	ZD1,ZD2	EDZVT2R6.2 B	ROHM	_	6.2V,5mA,150mW, 0603 (1608)		
Tran	Transistor						
1	TR1	2SA2029T2L R	ROHM	_	-50V,150mA,0505(1211)		
2	FET1,FET2	RS6L090BG TB1	ROHM	_	60V,90A,4.7mΩmax,202 4(4960)		
Indu	ctor						
1	L1	XAL1010-15 3MED	Coilcraft	15µH	60V,9.9A,18.6mΩmax,± 20%,(10.0 x 11.3)		
LED							
1	LED1	SML-D13U8 WT86	ROHM	_	RED,2.1V,20mA,52mW, 0603(1608)		
1	LED2	SML-D12P8 WT86	ROHM	_	GRN,2.2V,20mA,54mW, 0603(1608)		
Othe	ers						
1	J3	HIF3FC-14P A-2.54DSA(7 1)	Hirose Electr	_	200V,1A,IMD14-2.54-H9 .3-HIF3FC_DSA,200Vac ,1A		
2	JP_LDO,JP_ 12V	61300211121	Wurth Elektr onik	_	250V,3A,2.54,5.08*2.54		
2	JP_Loop,JP _REG	61300311121	Wurth Elektr onik	_	250V,3A,2.54,7.62*2.54		
1	SW_RC	ATE1E-2M3- 10-Z	Nidec Copal Electronics	_	ON-OFF-ON,2.54-ATE1, 60V,50mA,0.4VA		

2	J1,J2	XW4E-02C1- V1	Omron	_	250V,13.5A,5.08-XW4E, 250V,13.5A
1	FT234x	AE-FT234X	AKIZUKI DE NSHI TUSH O	_	5V, 2.54, FT234XD

# **Reference Application Data**

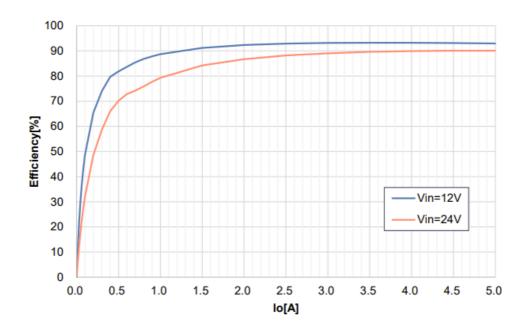


Figure 11-1. Efficiency vs lo

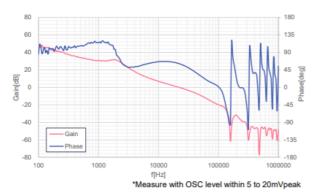


Figure 11-2. Frequency Characteristics (Vin=12V, Vo=5V, Io=5A, OSC:20mVpeak)

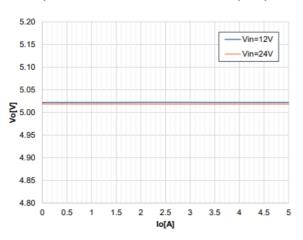
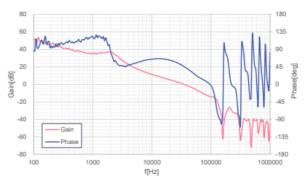


Figure 11-4. Load Regulation



\*Measure with OSC level within 5 to 20mVpeak Figure 11-3. Frequency Characteristics (Vin=24V, Vo=5V, Io=5A, OSC:20mVpeak)

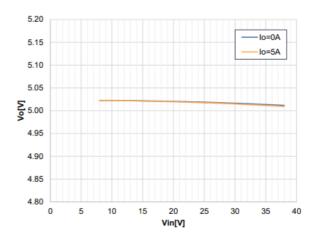


Figure 11-5. Line Regulation

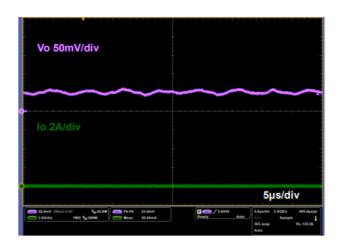


Figure 11-6. Output Ripple Voltage (Vin=12V, Vo=5V, Io=0A)

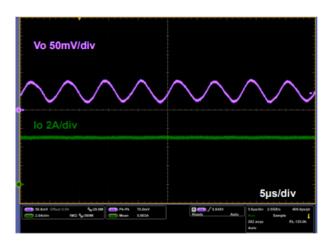


Figure 11-7. Output Ripple Voltage (Vin=12V, Vo=5V, Io=5A)

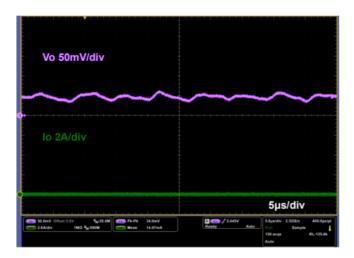


Figure 11-8. Output Ripple Voltage (Vin=24V, Vo=5V, Io=0A)

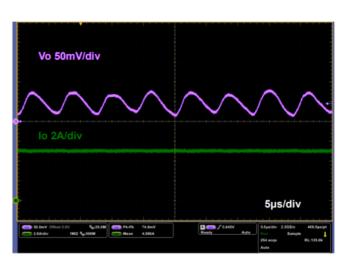


Figure 11-9. Output Ripple Voltage (Vin=24V, Vo=5V, Io=5A)

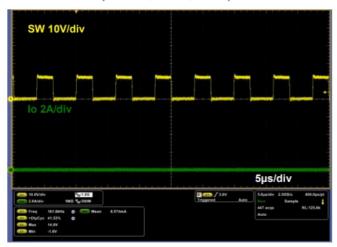


Figure 11-10. Switching Waveform (Vin=12V, Vo=5V, Io=0A)

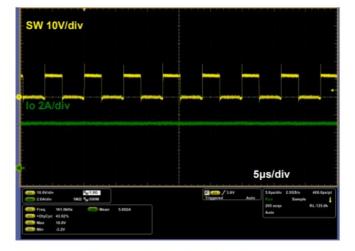


Figure 11-11. Switching Waveform (Vin=12V, Vo=5V, Io=5A)

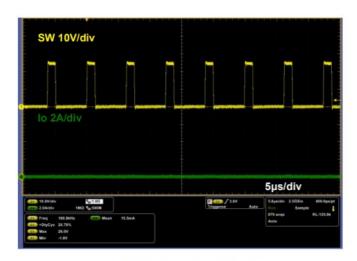


Figure 11-12. Switching Waveform (Vin=24V, Vo=5V, Io=0A)

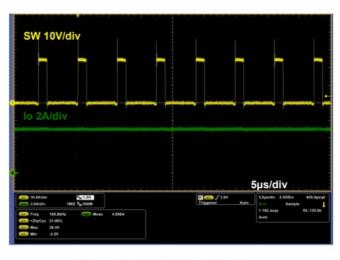


Figure 11-13. Switching Waveform (Vin=24V, Vo=5V, Io=5A)

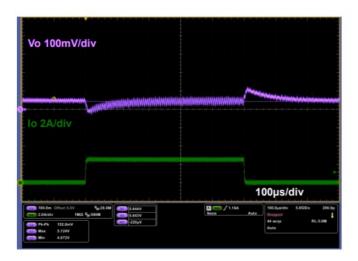


Figure 11-14. Load Transient (Vin=12V, Vo=5V, Io=0A⇔2.5A, 1A/μs)

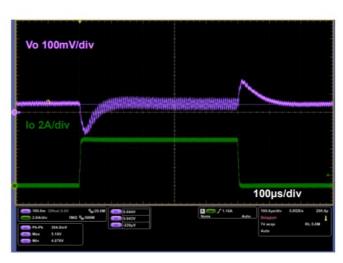


Figure 11-15, Load Transient (Vin=12V, Vo=5V, Io=0A⇔5A, 1A/μs)

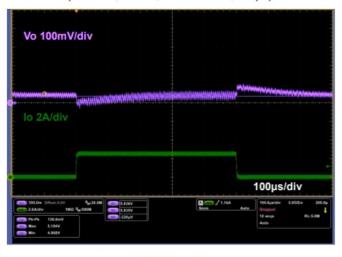


Figure 11-16. Load Transient (Vin=24V, Vo=5V, Io=0A⇔2.5A, 1A/μs)

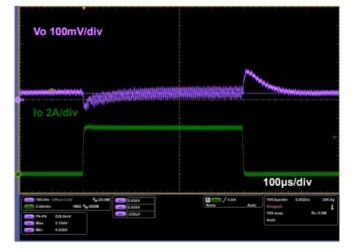


Figure 11-17. Load Transient (Vin=24V, Vo=5V, Io=0A⇔5A, 1A/μs)

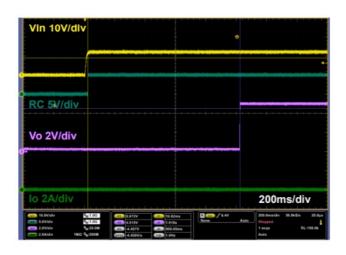


Figure 11-18. Startup Waveform (Vin=0→12V, Vo=5V, Io=0A, RC=open)



Figure 11-19. Startup Waveform (Vin=0→12V, Vo=5V, Io=5A, RC=open)

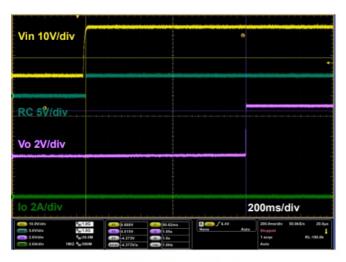


Figure 11-20. Startup Waveform (Vin=0→24V, Vo=5V, Io=0A, RC=open)



Figure 11-21. Startup Waveform (Vin=0→24V, Vo=5V, Io=0A, RC=open)

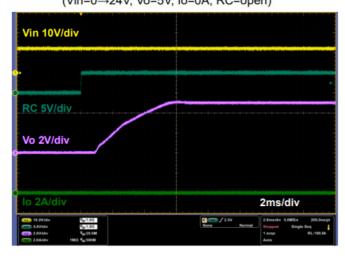


Figure 11-22. Startup Waveform (Vin=12V, Vo=5V, Io=0A, RC=L→H)

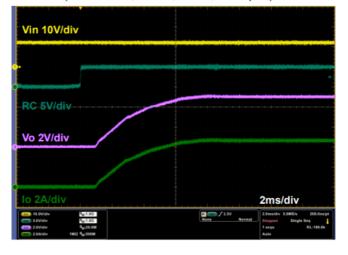


Figure 11-23. Startup Waveform (Vin=12V, Vo=5V, Io=5A, RC=L→H)



Figure 11-24. Startup Waveform (Vin=24V, Vo=5V, Io=0A, RC=L→H)

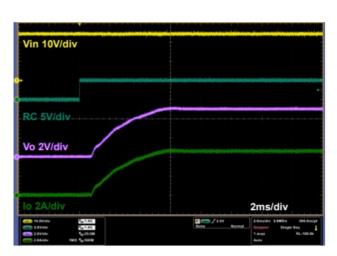


Figure 11-25. Startup Waveform (Vin=24V, Vo=5V, Io=5A, RC=L→H)

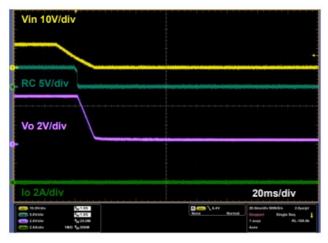


Figure 11-26. Stop Waveform (Vin=12→0V, Vo=5V, Io=0A, RC=open)

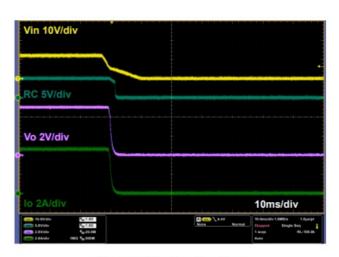


Figure 11-27. Stop Waveform (Vin=12→0V, Vo=5V, Io=5A, RC=open)

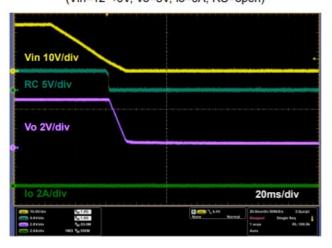


Figure 11-28. Stop Waveform (Vin=24→0V, Vo=5V, Io=0A, RC=open)

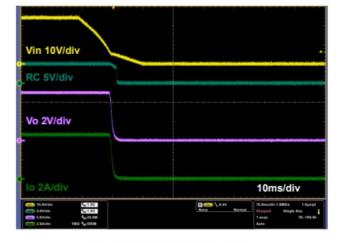


Figure 11-29. Stop Waveform (Vin=24→0V, Vo=5V, Io=5A, RC=open)

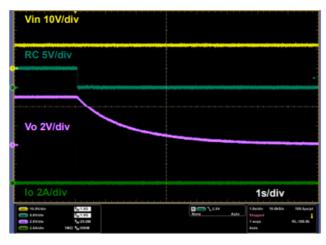


Figure 11-30. Stop Waveform (Vin=12V, Vo=5V, Io=0A, RC=H→L)

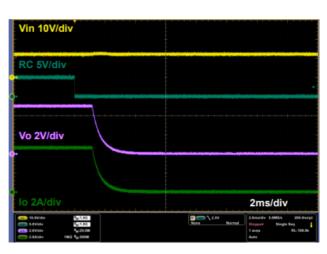


Figure 11-31. Stop Waveform (Vin=12V, Vo=5V, Io=5A, RC=H→L)

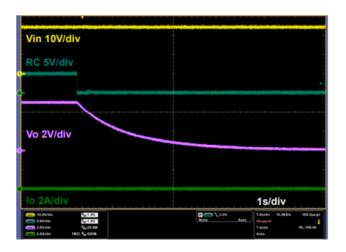


Figure 11-32. Stop Waveform (Vin=24V, Vo=5V, Io=0A, RC=H→L)

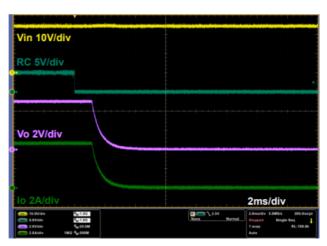


Figure 11-33. Stop Waveform (Vin=24V, Vo=5V, Io=5A, RC=H→L)

#### References

- 1. 66AN145E, Rev001, Analog-Digital hybrid control innovating switching power design
- 2. FEDL62Q2045-01, ML62Q2033/2035/2043/2045 datasheet
- 3. FEUL62Q2045-03, ML62Q2033/2035/2043/2045 User's Manual
- 4. 66AN147E, Rev.001, Operating system for switching power control MCU "RMOS"
- 5. TSZ02201-0BDB0A400100-1-2 Rev.001, For Automotive 45V 150mA Fixed/Adjustable Output Nano CapTM LDO Regulators BD9xxN1-C Series datasheet
- 6. TSZ02201-0RAR0G200370-1-2 Rev.001, High Speed Low Voltage Operation CMOS Operational Amplifiers BU7481G BU7481SG datasheet
- 7. TSZ02201-0Q2Q0A800840-1-2, Rev.002, High Frequency High-Side and Low-Side Driver BD2320EFJ-LA datasheet
- 8. 66AN149E, Rev.001, Serial communication of RMOS and GUI developing manual

## **Revision History**

Date	Revisi on Numb er	Description
10. May.20 24	001	Initial release.
31. Oct. 20 24	002	p.12 Add description of 4.14 LED indicator.  p.17 Add measurement condition and comment in Figure 11-2 and 11-3.

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#### **FAQ**

## Q: Can I use a different input voltage than 12V?

A: The evaluation board is designed for a 12V input voltage. Deviating from this may result in improper functioning or damage to the board.

## Q: How can I update the firmware on the evaluation board?

A: Refer to the user manual or manufacturer's guidelines for detailed instructions on updating the firmware of the evaluation board.

## **Documents / Resources**



ROHM LogiCoA001-EVK-001 Synchronous Buck DCDC Converter Evaluation Board [pdf] User Guide

LogiCoA001-EVK-001, LogiCoA001-EVK-001 Synchronous Buck DCDC Converter Evaluation Board, Synchronous Buck DCDC Converter Evaluation Board, DCDC Converter Evaluation Board, Converter Evaluation Board, Evaluation Board

### References

- User Manual
- ROHM
- ◆ Converter Evaluation Board, DCDC Converter Evaluation Board, Evaluation Board, LogiCoA001-EVK-001, LogiCoA001-EVK-001 Synchronous Buck DCDC Converter Evaluation Board, ROHM, Synchronous Buck DCDC Converter Evaluation Board

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