RENESAS RZ/V Series 2nd Generation Embedded AI MPUs User Manual

User's Manual

RZ/V Series, 2nd Generation
User's Manual: Hardware
arm

Preliminary
Specifications common to RZ/V Series Products
RZ/V2L

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device’s operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

   Semiconductor devices must be stored and transported in an anti-static container, static shielding bag, or conductive material. All test and measurement tools including workbenches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. The input of signal during the power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that

results from the input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during the power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under Handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at the input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example, to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system evaluation test for the given product.

Contents

Overview

1.1 Introduction

The RZ/V2L includes:

RZ/V2L

- 1.2GHz Arm® Cortex®-A55 Dual / Single MPCore cores,
- 200-MHz Arm® Cortex®-M33 core,
- 500-MHz Arm® Mali TM -G31,
- Memory controller for DDR4-1600 / DDR3L-1333 with 16 bits,
- 1 channel MIPI DSI interface or 1channel parallel output interface selectable,
- 1 channel MIPI CSI-2 input interface or 1channel parallel input interface selectable,
- The video processing unit,
- USB2.0 host / function interface,
- Gigabit Ethernet interface,
- SD card host interface,
- CAN interface,
- Sound interface, and
- DRP-AI for accelerating AI processing.

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1.2 List of Specifications
1.2.1 CPU Core
Item
Description
System CPU Cortex-A55
RZ/V2L

- Arm Cortex-A55 Dual / Single MPCore 1.2 GHz
- L1 I-cache 32 KBytes (Parity) / D-cache 32 KBytes (ECC)
- L2 cache 0 KByte
- L3 cache 256 KBytes (ECC)
- NEON™ / FPU supported
- Cryptographic Extension supported
- Arm®v8.2-A architecture

System CPU Cortex-M33
RZ/V2L

- Arm Cortex-M33 Processor 200MHz
- Security Extension supported
- Arm®v8-M architecture

Boot
RZ/V2L

- 6 boot modes
  — Boot Mode 0: Booting from USD
  Boot Mode 1: Booting from eMMC (1.8V)
  Boot Mode 2: Booting from eMMC (3.3V)

Boot Mode 3: Booting from a serial flash memory (Single / Quad / Octal) connected to the SPI Multi I/O bus space (1.8 V)

Boot Mode 4: Booting from a serial flash memory (Single / Quad) connected to the SPI Multi I/O bus space (3.3 V)

Boot Mode 5: Booting from SCIF download

Debug Interface
RZ/V2L

- Arm® CoreSight TM architecture
- JTAG / SWD interface supported
- ETF 16 KBytes for program flow trace (each cluster)
- JTAG Disable supported

1.2.2 CPU Peripheral

Item
Description
Clock Pulse Generator
(CPG)
RZ/V2L

- Generates the clocks from the external clock (EXTAL 24 MHz).
  — Maximum Arm Cortex-A55 clock: 1.2 GHz
  — Maximum Arm Cortex-M33 clock: 200 MHz
  — Maximum DDR clock: 666 MHz (DDR3L-1333), 800 MHz (DDR4-1600)
  — Maximum 3DGE clock: 500 MHz
  — Maximum VCP clock: 200 MHz
  Maximum AXI-bus clock: 200 MHz
  Maximum APB-bus clock: 100 MHz
- SSC (Spread Spectrum Clock) supported

Under Development
RZ/V Series, 2nd Generation RZ/V2L

Item
Description
Direct Memory Access
Controller
RZ/V2L
(DMAC)

- 2 modules, 16 channels per module
- Transfer request: on-chip peripheral request/auto-request (software trigger)
- A specific DMA transfer interval can be specified to adjust the bus occupancy.
- LINK mode (DMA transfer under descriptor control) supported
- Transfer information can be automatically reloaded

Generic Interrupt Controller
(C)
RZ/V2L

- Arm® CoreLink TM Generic Interrupt Controller (GIC-600) for Arm Cortex-A55
- 32 priority levels available
- Nested Vectored Interrupt Controller (NVIC) for Arm Cortex-M33
- External Interrupt pins (NMI, IRQ7 to IRQ0, TINT31-0)
- On-chip peripheral Interrupts: priority level set for each module

Message Handling Unit
(MHU)
RZ/V2L

- Message handling function between Arm Cortex-A55 and Arm Cortex-M33
- Assert interrupt to inform message and response from/to Arm Cortex-A55, CortexM33

General-purpose I/O (GPIO)
RZ/V2L

- General-purpose I/O ports

  Thermal Sensor Unit (TSU)

  RZ/V2L
- 1 channel

  1.2.3Internal Memory

  Item

  Description

  System RAM

  RZ/V2L
- RAM of 128 Kbytes (ECC)**1.2.4 External Memory Interface**

  Item

  Description

  External Bus Controller for DDR3L / DDR4 SDRAM RZ/V2L (DDR)
- Support DDR3L-1333 / DDR4-1600
- Bus Width: 16-bit
- Inline ECC supported (Support error detection interrupt)
- Memory Size: Up to 4 GB
- Auto Refresh / Self Refresh supported
- Memory access protection for secure regions using TZC-400 (Arm® TrustZone® supported)

Under Development
RZ/V Series, 2nd Generation RZ/V2L
Item
Description
SPI Multi I/O Bus Controller
(SPIM)
RZ/V2L,

- 1 channel (8bit Double data rate)
- Up to 2 serial flash memories with multiple I/O bus sizes (single / quad) can be connected
- Connectable with 1 Octal-SPI flash memory
- Connectable with 1 HyperFlash memory
- External address space read mode (built-in read cache)
- SPI operation mode
- Maximum Clock Frequency: 50 MHz (Quad-SPI DDR), 66 MHz (Quad-SPI SDR), 100 MHz (Octal-SPI, HyperFlash)

SD Card Host Interface / Multimedia Card Interface (SD/MMC)
RZ/V2L

- 2 channels
- Channel 0 supports SDHI / e-MMC (boot supported)
- Channel 1 supports SDHI
- SD memory I/O card interface (1-bit / 4-bit SD bus)
- SD, SDHC, and SDXC SD memory card access supported
- Compliant with SD 3.0
- Default, high-speed, UHS-I/SDR50, SDR104 transfer modes supported
- Error check function: CRC7 (Command), CRC16 (Data)
- Card detection function, write-protect supported
- MMC interface (1-bit / 4-bit / 8-bit MMC bus)
- e-MMC device access supported
- Compliant with eMMC 4.51
- High-speed, HS200 transfer modes supported

1.2.5 Graphics Unit
Item
Description
3D Graphics Engine (3DGE)
RZ/V2L

- Arm Mali-G31
- One single-pixel shader core
- 8 Kbytes L2 Cache
- Vulkan 1.1 Supported
- OpenGL ES1.1 / 2.0 / 3.1 / 3.2 Supported• OpenCL 2.0 Full Profile Supported
- Android 10 or later Supported

Under Development
RZ/V Series, 2nd Generation RZ/V2L
1.2.6 Video Processing Unit
Item
Description
Video Codec Processor (VCP)
RZ/V2L,

- H.264 codec module
- Encoding / Decoding support
  H.264 / AVC (High Profile / Main Profile / Baseline Profile)
  H.264 / MVC (Stereo High Profile)
- Maximum pixel rate: 1920 x 1080 x 30 fps
- Color format (input in encoding): YcbCr 4:2:0 semi-planar supported
- Color format (output in decoding): YcbCr 4:2:0 semi-planar supported

Image Scaling Unit ISU)
RZ/V2L

- Scaling down function with bilinear interpolation
- Input image Size (max): 5M (2800×2047)
- Output image Size (max): Full HD (1920×1080)
- Support Color format Conversion
- RGB / ARGB / YcbCr422 / YcbCr420 / RAW(Grayscale)

1.2.7
Camera Interfaces
Item
Description
MIPI CSI-2 Interface RZ/V2L

- 1 channel
- The number of Lane: 1/2/4-lane
- Support 5MP, 30 fps (RAW12)
- Maximum Bandwidth: 1.5 Gbps per lane
- Select 1 VC from 4 VC (virtual channel) supported
- Support Input Image Data Formats:
  YUV420 8-bit / 10-bit
  Legacy YUV420 8-bit
  YUV420 8-bit / 10-bit (Chroma Shifted Pixel Sampling)
  YUV422 8-bit / 10-bit
  RGB444 / RGB555 / RGB565/ RGB666 / RGB888
  RAW6 / RAW7 / RAW8 / RAW10 / RAW12 / RAW14 / RAW16 / RAW20
- Generic short packet code 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8
- Generic long packet data type 1 / 2 / 3 / 4
- User Defined 8-bit data type 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8

Under Development
RZ/V Series, 2nd Generation RZ/V2L
Item
Description
Parallel Input Interface
RZ/V2L ,

- 1 channel
- Support ITU-R BT.656 Interface (Interlace supported, YcbCr422 8-bit / 10-bit)
- Support HD, 30 fps (YCbCr422 Interleave), 60fps (YCbCr422 Y/CbCr separate data, binary data)
  Maximum input pixel frequency: 108MHz
- Support Input Data Format: YcbCr422 8-bit / 10-bit Binary data 16-bit
- VSYNC / HSYNC / FIELD timing signal supported

RZ/V2L ,
MIPI CSI-2 / Parallel to AXI Bridge Module

- 1 channel (MIPI CSI-2 Input or Parallel Input)
- Support Image Processing:
  Clipping
  Frame Sampling
  LUT
  Color format conversion
  Color space conversion
- Support Color Formats for Image Processing:
  YUV422 8/10-bit
  RGB565 / RGB666 / RGB888
  RAW8 / 10 / 12 / 14 / 16 (Clipping and Frame Sampling only)
- Support Output Data Formats:
  YCbCr422 8-bit (Interleave/Semi planar, Interlace/Progressive)
  YCbCr420 8-bit (Interleave, Interlace)
  Y-Only
  RGB888 / ARGB8888
  RAW8/10/12/14/16 (without Image Processing)
  MIPI CSI-2 V2.1 Recommended Memory storage data (without Image Processing)

1.2.8 Display Interface
Item
Description
LCD Controller
RZ/V2L,

- 1 channel (MIPI DSI output or Parallel output)
- 2 planes blending (can blend 2 different size images)
- Support Image Processing:
  Dither processing (RGB666)
  Clipping
  RGB Gamma Correction LUT
- Support Input Data Format:
  RGB565 / RGB666 / RGB888
  ARGB1555 / ARGB4444 / ARGB8888
  YcbCr444 8-bit / YcbCr422 8-bit / YcbCr420 8-bit

Under Development
RZ/V Series, 2nd Generation RZ/V2L
Item
Description
MIPI DSI Interface
RZ/V2L

- 1 channel
- The number of Lane: 4-lane
- Support Full HD (1920 x 1080), 60 fps (RGB888)
- Maximum Bandwidth: 1.5 Gbps per lane (T.B.D.)
- Support Output Data Format:
  RGB666 / RGB888

Parallel Output Interface
RZ/V2L,

- 1 channel
- Support WXGA (1280×800), 60 fps (T.B.D.)
- Support Output Data Format:
  RGB666 / RGB888
- CLK / HD / VD timing signal supported

1.2.9 Sound Interface
Item
Description
Serial Sound Interface (SSI)
RZ/V2L,

- 4 channels bidirectional serial transfer
- 2 external clock sources are available
- Duplex communication (channel 0, 1, and 3)
- Support of I2S / Monaural / TDM audio formats
- Support of master and slave functions
- Generation of programmable word clock and bit clock
- Multi-channel formats
- Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats
- Support of 32-stage FIFO for transmission and reception
- Support of LR-clock continue to function in which the LR-clock signal is not stopped

Sampling Rate Converter (SRC)
RZ/V2L

- 1 channel
- Data format: 16-bit (stereo / monaural)
- Sampling Rate
  Input: Selectable from 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32

kHz, 44.1 kHz, 48 kHz

Output: Selectable from 8 kHz*, 16 kHz*, 32 kHz, 44.1 kHz, 48 kHz (*:can select in 44.1kHz input mode)

- SNR: more than or equal to 80db

Under Development
RZ/V Series, 2nd Generation RZ/V2L
1.2.10 Storage and Network
Item
Description
USB2.0 Host / Function (USB)
RZ/V2L

- 2 channels (ch0: Host-Function ch1: Host-only)
- Compliance with USB2.0
- Supports On-The-Go (OTG) Function
- Supports Isochronous transfer
- Internal dedicated DMA

Gigabit Ethernet Interface (GbE)
RZ/V2L,

- 2 channels
- Supports transfer at 1000 Mbps and 100 Mbps, 10Mbps
- Supports filtering of Ethernet frames
- Supports interface conforming to IEEE802.3 PHY RGMII (Reduced Gigabit Media Independent Interface)
- Supports interface conforming to IEEE802.3 PHYMII (Media Independent Interface)

CANFD Interface (RS-CANFD)
RZ/V2L

- 2 channels
- ISO 11898-1 (2003) compliant
- CAN-FD ISO 11898-1 (CD2014) compliant
- Message buffer

  Up to 64 x, 2-channel receive message buffer: shared among all channels 16 transmit message buffers per channel

Under Development
RZ/V Series, 2nd Generation RZ/V2L
1.2.11 Timer
Item
Description
Multi-function Timer Pulse Unit 3 (MTU3a)
RZ/V2L

- 9 channels (16 bits x 8 channels, 32 bits x 1 channel)
- Module clock frequency (P1φ): 50 MHz

- Maximum 28 lines of pulse inputs/outputs and 3 lines of pulse inputs
- 14 types of count clocks selectable
- Input capture function
- 39 outputs compare and input capture registers
- Counter clear operation (Simultaneous counter clearing by Compare match or Inpucapture is available)
- Simultaneous writing to multiple timer counters (TCNT)
- Synchronous input/output of each register due to the synchronous operation of the counter
- Buffered operation
- Cascade-connected operation
- 43 types of interrupt sources
- Automatic transfer of registered data
- Pulse output modes
  Toggle, PWM, complementary PWM, and reset-synchronized PWM modes
- Phase counting mode
  16-bit mode (channel 1 and 2)
  32-bit mode (channel 1 and 2)
- The counter function of dead time compensation
- Digital filter functions for the input capture and external count clock pin

Port Output Enable 3 (POE3)
RZ/V2L

- Control of the high-impedance state of the MTU3a waveform output pins
- Activation with four input pins
- Activation on detection of short-circuited outputs (detection of simultaneous PWM
  output to the active level)
- Activation by register write
- Additional programming of output control target pins is possible.

Under Development
RZ/V Series, 2nd Generation RZ/V2L
Item
Description
General PWM Timer (GPT)
RZ/V2L,

- 32 bits x 8 channels
- Counting up or down (sawtooth wave), counting up and down (triangular wave) selectable for all channels
- Independent selectable for each channel
- 2 input/output pins per channel
- 2 output compare/input capture registers per channel
- For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers
  when buffering is not in use
- In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally

asymmetrically PWM waveforms
- Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow)
- Generation of dead times in PWM operation
- Synchronous start/stop / clear of counters on arbitrary channels
- Starting, stopping, and clearing up/down counters in response to a maximum of eight events
- Starting, stopping, and clearing up/down counters in response to input level comparison
- Starting, stopping, and clearing up/down counters in response to a maximum of four external triggers
- Output pin invalidation functions due to dead time error or detection of short circuit between output pins
- Digital filter functions for the input capture and external trigger pins

Port Output Enable for GPT (POEM)
RZ/V2L

- Output prohibition control of the GPT waveform output pin
- Activation with up to four input pins
- Activation by dead time error detection or output short detection
- Activation by register write

Watchdog Timer (WDT)
RZ/V2L

- 3 channels
- A counter overflow can reset the LSI
- CPU parity error can reset the LSI

General Timer (GTM)
RZ/V2L

- 32 bits x 3 channels
- Two operating modes
  – Interval timer mode
  – Free-running comparison mode

Under Development
RZ/V Series, 2nd Generation RZ/V2L
1.2.12 Peripheral Module
Item
Description
I2C Bus Interface (I2C)
RZ/V2L,

- 4 channels
- Master mode and slave mode supported
- Support for 7-bit and 10-bit slave address formats
- Support for multi-master operation

- Timeout detection

Serial Communication Interface with FIFO (SCIFA)
RZ/V2L,

- 5 channels
- Clock synchronous mode or asynchronous mode selectable
- Simultaneous transmission and reception (full-duplex communication) supported
- Dedicated baud rate generator
- Separate 16-Byte FIFO registers for transmission and reception
- Modem control function (channel 0, 1, and 2 in asynchronous mode)

Serial Communication
Interface (SCIg)
RZ/V2L

- 2 channels
- Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable
- Simultaneous transmission and reception (full-duplex communication) supported
- Dedicated baud rate generator
- LSB first / MSB first selectable
- Modem control function
- Encoding and decoding of IrDA communications waveforms in accord with version

1.0 of the IrDA standard (on channel 0)
Renesas Serial Peripheral Interface (RSPI)
RZ/V2L

- 3 channels
- SPI operation
- Master mode and slave mode supported
- Programmable bit length, clock polarity, clock phase can be selected
- Consecutive transfers
- LSB first / MSB first selectable
- Maximum transfer rate: 50 Mbps (T.B.D.)

1.2.13 Security
Item
Description
Trusted Secure IP (TSIP) [option]
RZ/V2L

- Security algorism

  Common key encryption: AES

  Non-common key encryption: RSA, ECC
- Other features

TRNG (true random number generator)

Hash value generation: SHA-1, SHA-224, SHA-256, GHASH Support of Unique ID

Under Development
RZ/V Series, 2nd Generation RZ/V2L
Item
Description
Time programmable memory (OTP)
RZ/V2L

- A nonvolatile memory that can be written only once
- Security setting, authentication settings is possible
- Support one time read function (512 Bytes) 1.2.14 Analog

Item
Description
A/D Converter (ADC)
RZ/V2L,

- 8 channels
- Resolution: 12-bit
- Input Range: 0V ~ 1.8V
- Conversion Time: 1us
- Operation Mode: Single Scan / Continuous Scan
- Condition for A/D conversion start

  Software trigger

  Asynchronous trigger: External trigger supported

  Synchronous trigger: MTU and PWM timer

1.2.15 Others
Item
Description
Boundary Scan
RZ/V2L

- Boundary-scan based on IEEE 1149.1 via JTAG interface is supported.

  Note that some module pins are not available on this boundary-scan.

  1.2.16 AI Accelerator

Item
Description
AI Accelerator
RZ/V2L

- DRP-AI

  1.2.17 Power supply voltage

Item

Description
Power supply voltage
RZ/V2L

- T.B.D.

1.2.18 Temperature range

Item
Description
Temperature range
RZ/V2L

- Ta : -40℃ to +85 ℃ (1) *
- Tj : -40℃ to +125 ℃ (T.B.D)

(*1) : If wider temp is required than this range, use case has to be investigated.

Under Development

RZ/V Series, 2nd Generation RZ/V2L

1.2.19 Quality level

Item

Description

Quality level

RZ/V2L

- Industrial usage, etc.

1.2.20 Package

Item

Description

Package

RZ/V2L ,

- 551-pin BGA, 21-mm square, 0.8-mm pitch
- 456-pin BGA, 15-mm square, 0.5-mm pitch

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RZ/V Series, 2nd Generation
RZ/V2L

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Documents / Resources

	**RENESAS RZ/V Series 2nd Generation Embedded AI MPUs** [pdf] User Manual RZ V Series, 2nd Generation Embedded AI MPUs, RZ V Series 2nd Generation Embedded AI MPUs