RENESAS RA family, RX family 32-Bit Arm Cortex-M Microcontrollers Owner's Manual

RENESAS Application Notes

RA family, RX family

Board design guideline for BGA products

Summary

This guideline is intended to help those who are familiar with QFP (Quad Flat Package) and who are planning to use BGA (Ball Grid Array) packages for the first time. This document is a summary of points to note when designing a board that uses a BGA package.

Target Device

RA family, RX family

Contents [hide]

Characteristic of BGA packaging

What is BGA packaging

BGA package refers to a package in which solder balls are mounted on the back of the package (see Figure 1). BGA has the following characteristics compared to QFP.

Features of BGA package compared to QFP:
– A BGA package is typically smaller than an LQFP for the same number of pins.
– A BGA package typically has more pins than an LQFP for the same package size.
– BGA packages are better for heat dissipation as they have lower thermal resistance than QFP packages as there is a better heat dissipation path through the substrate.
– BGA packages are better low impedance and high transmission speeds because the package length can be shortened by miniaturization and the substrate (interposer) can be multilayered.
– BGA packages have an optimal ball arrangement when electrical characteristics are considered. However, if it is not necessary to consider the electrical characteristics, the ball can be placed anywhere.

Note: BGA with a plastic package material is called PBGA (Plastic BGA). In Renesas, BGA generally refers to PBGA.

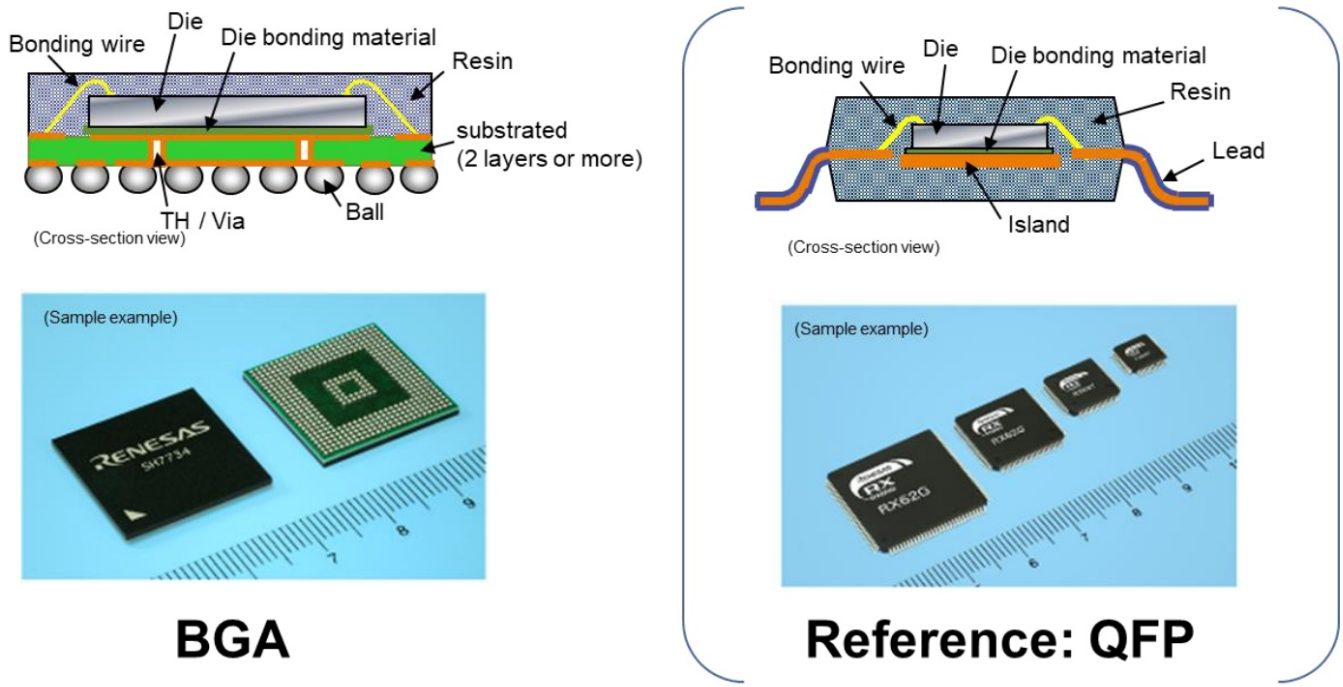


Figure 1, Cross-section view of BGA package and QFP and sample examples

Example of BGA ball arrangement

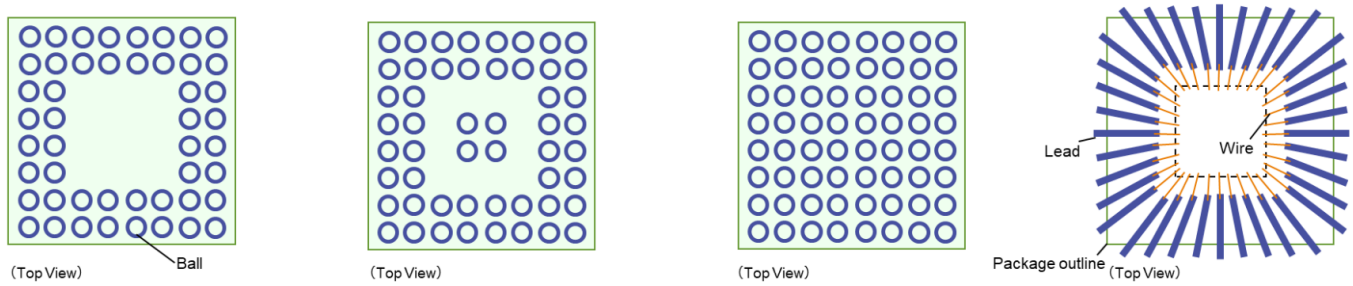
As shown in Figure 2, the number of signals that can be connected to QFP is almost

fixed relative to the package size (See Figure 2, Case QFP), BGA packages can be roughly divided into three ball arrangements.

– The first is when the ball is placed on the outer periphery of the package (See Figure 2, Case BGA①). It is used when the number of signals is relatively small for the package size.

– The second is when a thermal ball is placed directly under the chip in addition to the outer circumference of the package (See Figure 2, Case BGA②). It is adopted when heat dissipation needs to be considered.

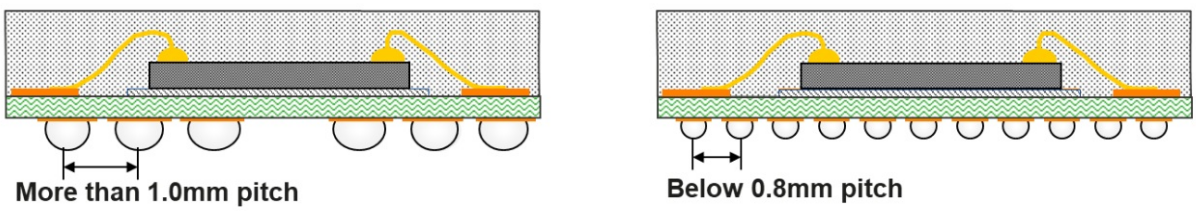
– The third is when the balls are placed across the entire surface of the package without gaps (See Figure 2, Case BGA③). It is used when the number of signals is large. In general, it is more difficult to design packages and boards with such a package, and both the package and the board it can be mounted on can become expensive.



BGA①: Periphery ball **BGA②: With thermal ball** **BGA③:Full grid ball** **QFP**

Definition of BGA, FBGA and LGA

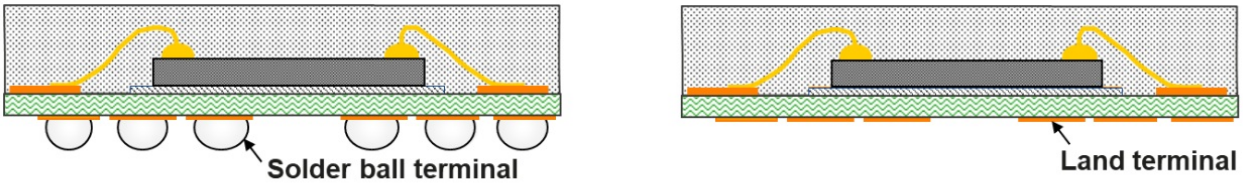
As shown in Figure 3, BGA and FBGA (Fine Pitch Ball Grid Array) have different terminal pitch specifications. A package with a terminal pitch of 1 mm or more is called BGA, and a package with a terminal pitch of 0.8 mm or less is called FBGA.



BGA：1mm ball pitch or more FBGA：Ball pitch less than 0.8 mm

Figure 3, Definition of BGA and FBGA

As shown in Figure 4, BGA and LGA (Land Grid Array) differ in the presence or absence of solder ball terminals. A package with solder ball terminals is called BGA, and a package without solder ball terminals is called LGA.



BGA：With ball　　LGA：Without ball

Figure 4, Definition of BGA and LGA

Package name and code (JEITA code)

The package of our ICs is uniformly assigned a JEITA package code in accordance with the JEITA standard “EIAJ ED-7303C”. The structure of the JEITA package code is introduced below.
The package code consists of the following 6 items and is displayed in a maximum of 30 characters.

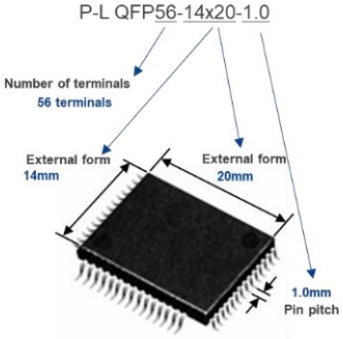
Package body material code 1

1. The package body material code is displayed as a single character according to the classification in Table

Table 1, Package body material code

Symbol	Material	Application
C	Ceramics	Ceramic package with a laminated structure
G	Ceramics	Glass-sealed ceramic package
M	Metal	Packages constructed of metallic materials
P	Plastics	Package formed of resin
S	Silicon	Package made of silicon
T	Tape	Package composed of tape

[Example of package code display]



Package Appearance Feature Codes 2

The package appearance feature code is displayed in up to 3 characters as necessary according to the functional classification in Table 2.

Table 2, Package Appearance Feature Codes

Ranking	Function class	Code	Meaning	Appearance characteristics
1	Addition of external features	H	Heat sink	With heat sink for heat dissipation
2	Package mounting height	L	Low profile	1.20mm<L≦1.70mm
		T	Thin	1.00mm<T≦1.20mm
		V	Very thin	0.80mm<V≦1.00mm
		W	Very-very thin	0.65mm<W≦0.80mm
		U	Ultra thin	0.50mm<U≦0.65mm
		X	Extremely thin	X≦0.50mm
3	Linear spacing of terminals	F	Fine pitch	Terminal-pitch 0.8mm or less (BGA, LGA), 0.5mm or less (QFP)

Basic package name code 3

The basic package name code is displayed in three characters in principle according to the basic package name. The form classification of the package conforms to EIAJ ED-7300. As an exception, only the derived package name codes TSOP (1), TSOP (2), DTP (1), and DTP (2) corresponding to the basic package name code SOP and DTP are treated as basic package name codes, and 7 or 6 characters are allowed. At this time, TSOP (1) and TSOP (2) do not use conventional TSOP (I), TSOP (II), or the like. Further, in the case of TSOP (1), TSOP (2), DTP (1), and DTP (2), when the maximum number of digits of the package code exceeds 30 digits, the number of package terminals is omitted as shown in the example.

Package Terminal Number Codes 4

The number of terminal codes in the package is displayed in a maximum of 5 characters. The terminal is a general term for electrodes with different external connection methods, such as leads, pins, lands, bumps, and balls. Medium nuke indication is allowed for less than 100 pins, and 5 characters are specified. For example, in the case of a 28-pin package with 2 medium nukes, it is written as 28/26.

Package Nominal Dimension Codes 5

As shown in the example, the package nominal dimension code consists of “package body width (mm)” × “package body length (mm)” and is displayed in a maximum of 11 characters. However, if the decimal number is “x0” or “00”, “0” and “00” are not noted.

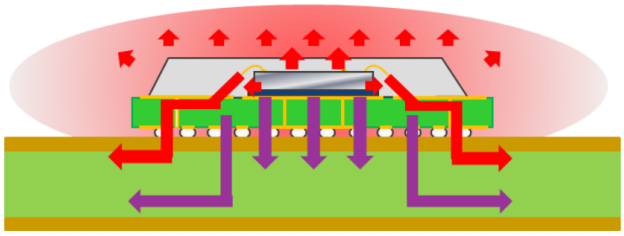
The terminal linear spacing code is displayed in 4 characters. Terminal linear spacing in inches (inches) in millimeters (mm) is rounded according to ISO R370.

Properties of BGA Packaging

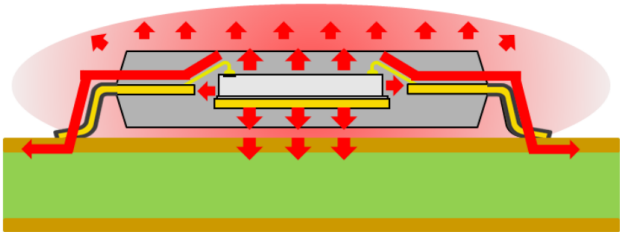
Thermal resistance A value that expresses the difficulty of transmitting temperature)

Compared to QFP, BGA has the advantage of low thermal resistance because it increases the heat dissipation path through the substrate. In other words, BGAs have better heat dissipation characteristics than QFP (See Figure 5).

As shown in Figure 5, compared to QFP, BGA has lower thermal resistance than QFP because in addition to the heat dissipation path from the lead portion and resin indicated by the red arrow, the heat generated by the chip indicated by the purple arrow is dissipated from directly under the chip from the source of heat generation through vias and balls of the package.



BGA



QFP

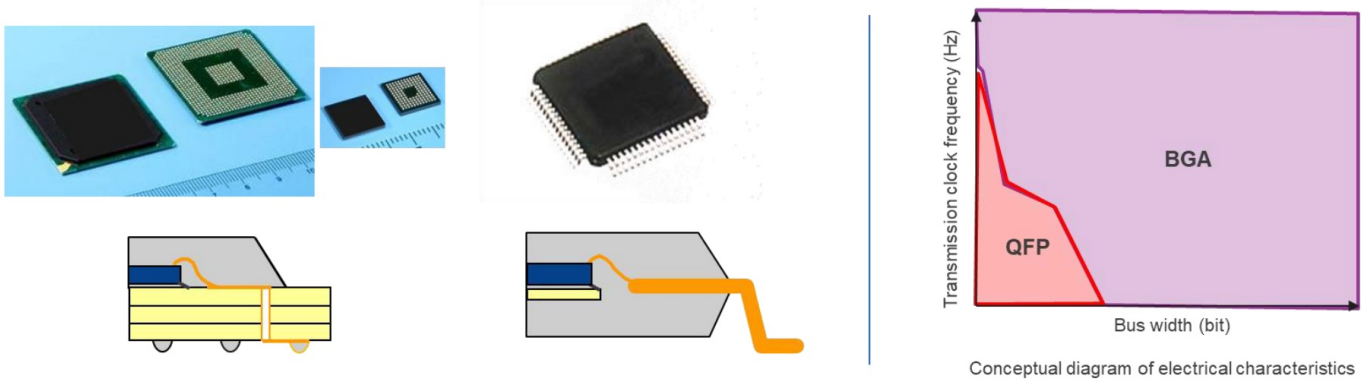
Electrical characteristics

BGA packages can be made smaller than packages with pins such as QFP packages, which is better for low impedance and high transmission speed (See Figure 6).

– Compared to QFP packages, BGA can shorten the total length inside the package, so that the inductance and resistance components can be lowered.

– The bonding-wire length and trace length inside a BGA package can be further shortened, and the inductance and resistance components can be lowered by reducing the package size of BGA.

Example: Since the BGA can reduce the power supply impedance, it is possible to reduce the number of bypass capacitors (hereinafter referred to as CC: Chip Capacitor) in the power supply and contribute to the reduction of BOM cost.



BGA　　QFP　　Relationship between bus width and transmission frequency

Figure 6, Image of BGA package total length (compared with QFP) and electrical characteristics

Implementation of BGA packaging

RA/RX BGA lineup of microcontrollers

RA/RX microcontrollers offer the following packages mainly for small consumer devices (See Figure 7 and Table 3).

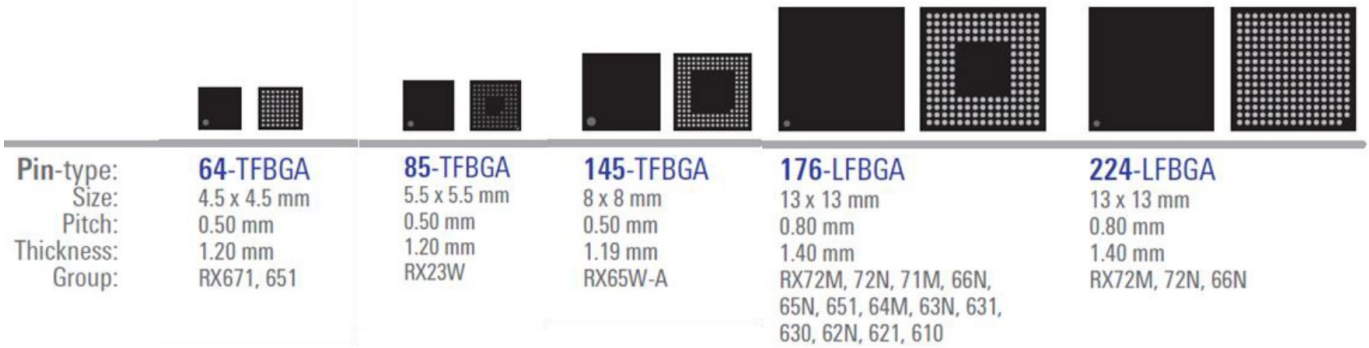


Figure 7, RA/RX BGA lineup of microcontrollers

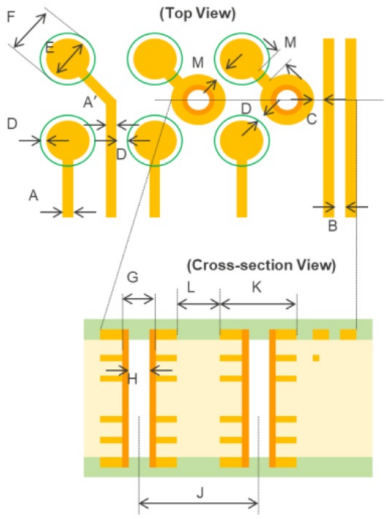
Table 3, List of BGA lineup of RA/RX microcontrollers

Target device	Target package information			
	Package name	Renesas code	Pin pitch	Size
RA4M3, RA6M4	BGA 64-pin	PLBG0064JC-A	0.65mm	6 x 6 mm
	BGA 144-pin	PLBG0144KB-A	0.5mm	7 x 7 mm
RA6M3	BGA 176-pin	PLBG0176GE-A	0.8mm	13 x 13 mm
RA6M5		PLBG0176GF-A	0.8mm	13 x 13 mm
RA4E2, RA6E2	BGA 36-pin	PLBG0036KA-A	0.5mm	4 x 4 mm
	BGA 64-pin	PLBG0064KB-A	0.5mm	5 x 5 mm
RA2A1	BGA 36-pin	PLBG0036GA-A	0.8mm	5 x 5 mm
RA2E1	VFBGA 64-pin	PVBG0064LB-A	0.4mm	4 x 4 mm
RX671, RX651	TFBGA 64-pin	PTBG0064KB-A	0.5mm	4.5 x 4.5 mm
RX72M, RX72N, RX71M, RX66N, RX65N, RX651, RX64M,RX63N, RX631, RX62N, RX621, RX610	LFBGA 176-pin	PLBG0176GA-A	0.8mm	13 x 13 mm
RX72M, RX72N, RX66N	LBBGA 224-pin	PLBG0224GA-A	0.8mm	13 x 13 mm
RX71M, RX671, RX65N, RX651, RX64M, RX63N, RX631,RX21A, RX210, RX113	TFLGA 100-pin	PTLG0100JA-A	0.65mm	7 x 7 mm
RX671, RX62N, RX621	TFLGA 145-pin	PTLG0145KC-A	0.65mm	9 x 9 mm

Recommended board design rules with through hole (TH)

The recommended board design rules for boards using TH are shown below (See Figure 8). In order to maximize the benefits of BGA packages in terms of traces and characteristics, it is recommended to apply board design rules that allow trace to pass between balls. It is recommended that the trace width in the package mounting area be at least 100 um.

Note: The recommended rules may vary depending on the board manufacturer, and it is necessary to contact the board manufacturer for details.



unit : um

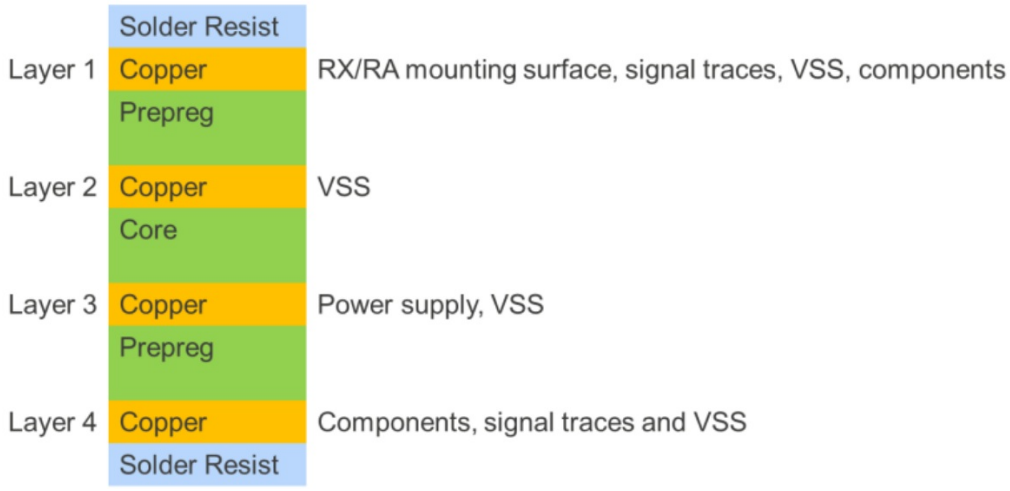
Symbol	Name	Recommended by Ball Pitch (assuming plate thickness 1.2 to 1.6 mm)					
		0.5mm ball pitch		0.65mm ball pitch		0.8mm ball pitch	
		Outer layer	Inner layer	Outer layer	Inner layer	Outer layer	Inner layer
A	Pattern-width (other than BGA)	100	75	100	75	100	100
A'	Pattern-width (BGA section only)	100	60	100	60	100	100
B	Pattern spacing (Min.)	100	75	100	75	100	100
C	Patterned TH Land Spacing (Min.)	100	70	100	70	100	100
D	Patterned-SR opening spacing (Min.)	50		50		50	
E	BGA padding diameter	ϕ200		ϕ250		ϕ400	
F	BGA padded SR opening diameter	ϕ300		ϕ350		ϕ500	
G	Through TH drilling diameter	ϕ200		ϕ200		ϕ250	
H	TH bore diameter	ϕ150		ϕ150		ϕ200	
J	TH Pitch (between centers)	650		650		800	
K	Through TH land diameter	ϕ450	ϕ450	ϕ450	ϕ450	ϕ500	ϕ500
L	Through TH land spacing	200	200	200	200	300	300
M	Through TH Land-BGA Pad Spacing (Min.)	100		100		100	

Figure 8, Recommended board design rules with through hole

Recommended layer configuration

As for the layer configuration of the board, a 4-layer board is recommended (See Figure 9). It is recommended that the RA/RA microcontroller should be placed on Layer 1 along with the with signal trace, VSS, and other components, VSS planes should be routed on layer 2, the minimum necessary power supply plane and VSS plane should be routed on

Layer 3, and with components, signal traces, and VSS on Layer 4. If it is necessary to further improve the electrical characteristics, it is recommended to add an additional two layers between the layer 2 and layer 3.



Basic board design concept

The basic idea of board design can be roughly divided into two steps. The 1st step (①) in which the outer circumference 2 Row is wired with a surface layer (Layer 1) where the RA/RX is mounted , and a 2nd step (②) in which the inner circumference 2 Row is wired on the back side (Layer 4) or an inner layer (2 or 3 layer) that is opposite the layer where the RA/RX through TH.

Figure 10 is an example of the layout of the basic concept of Layer 1 and Layer 4 of a full grid 64 BGA, and Figure 11 is a layout example of the basic concept of Layer 1 and Layer 4 of the outer circumference 4 Row-144 BGA. The red wire indicates the trace of Layer 1, the black circle indicates the ball, and the green wire and the green circle indicate the lead out line from the ball and TH. This example shows a case where one wire passes between the balls. If the trace does not pass between the balls, the trace layer increases by one, and depending on the trace situation of the other layers, the number of substrate layers may be 6 or more. The gray dotted circle indicates the ball passing through Layer 1, and the green circle indicates the TH and the callout line from TH. Although not shown, the capacitor is placed near TH. In addition, the TH position and trace withdrawal direction change depending on the specifications of the microcomputer mounted circuit.

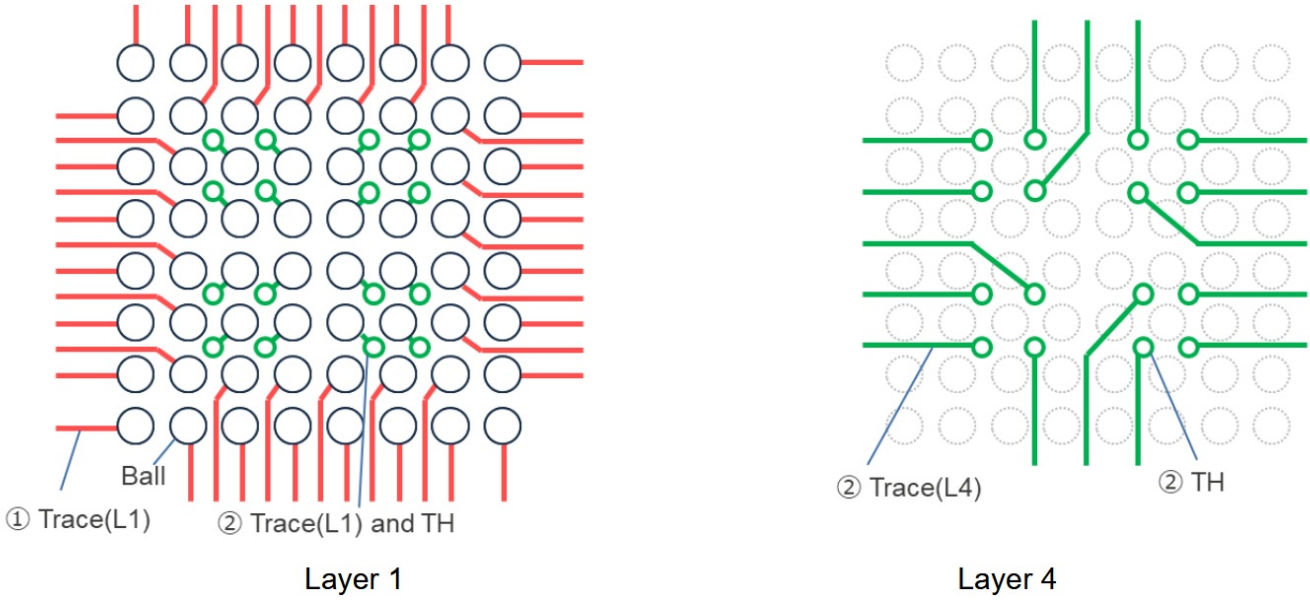


Figure 10, Example of basic layout for Layer 1 and Layer 4 of a 64 (8×8) BGA full grid (Top View)

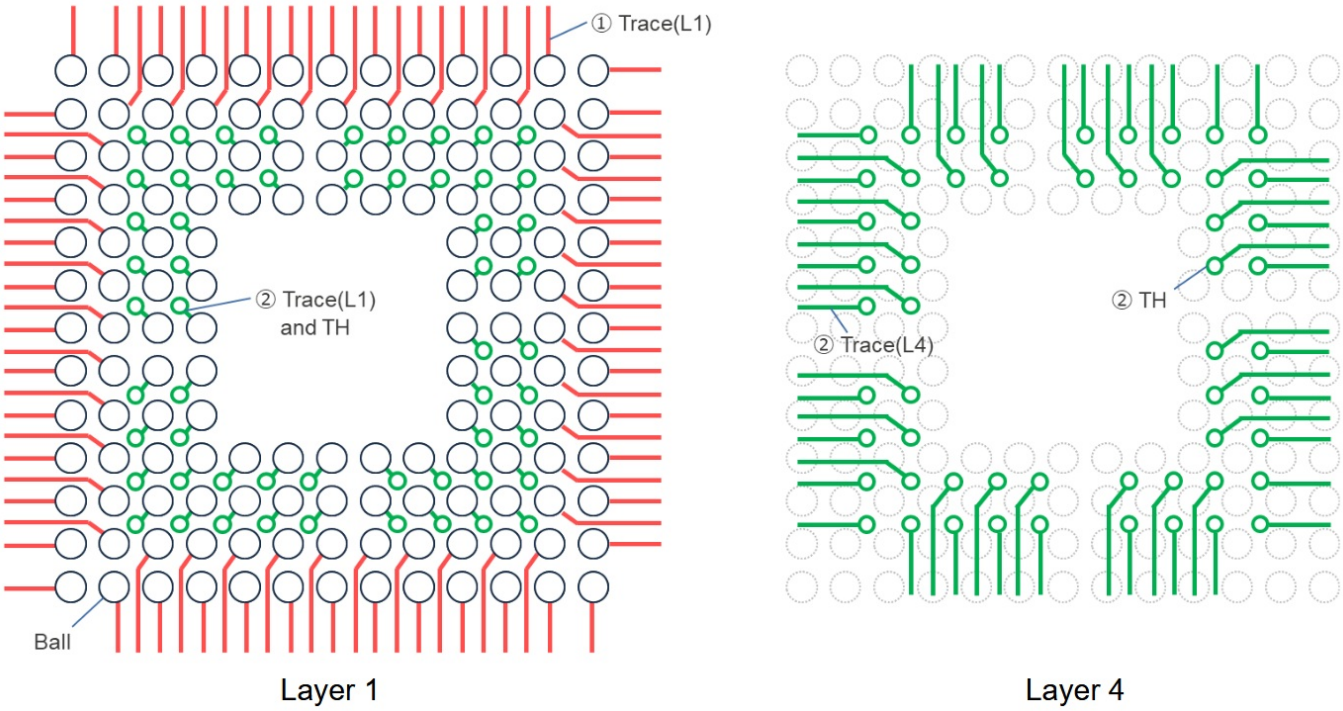


Figure 11, Example of basic layout for L1 and L 4 of 144(13×13)BGA outer perimeter 4 rows (Top View)

Recommended board design rules

Power Supply, VCL

– Connect a capacitor (a ceramic capacitor with good frequency characteristics) to the power supply pin with the shortest possible distance between the paired VSS. A capacitor is placed close to the IC/package and connected to the common plane after

the capacitor (See Figure 12). The current is designed to flow through the IC/package, through the capacitors, and through the common power supply VSS plane in order (See Figure 13).

-,It is recommended that the capacitor is mounted on the same side as the IC/package when the power supply terminals are arranged in the outer circumference 2row, and on the opposite side (back side/Layer 4) from the IC/package when the power supply terminals are arranged in the 3row or later.

– If there are specifications such as the distance from the IC/package to the capacitor (resistance/inductance value of trace and THs), capacitor capacitance and insertion position, ferrite bead insertion position, merge position with other power supplies, etc., follow each specification.

– The trace width and the number of THs after passing through the capacitor should take into account the size of the current that could flow, and design the trace with a width and a TH that exceeds the required number. Separate these traces as much as possible from other power supply balls to reduce the amount of coupling (including adjacent layers).

– Shield with VSS as much as possible. If VSS shielding is not possible, increase the spacing (>2×h (thickness between adjacent layers)).

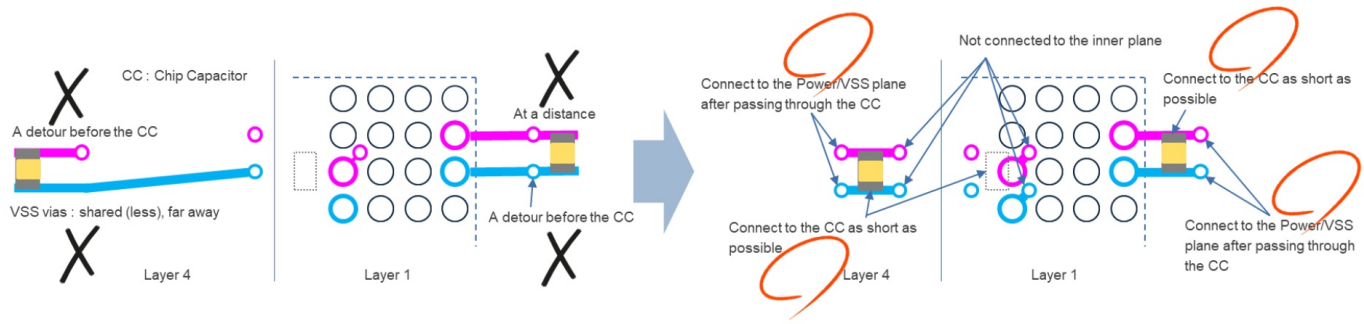


Figure 12, Image of recommended capacitor design for power supply and VCL (Layer 1 and 4, Top View

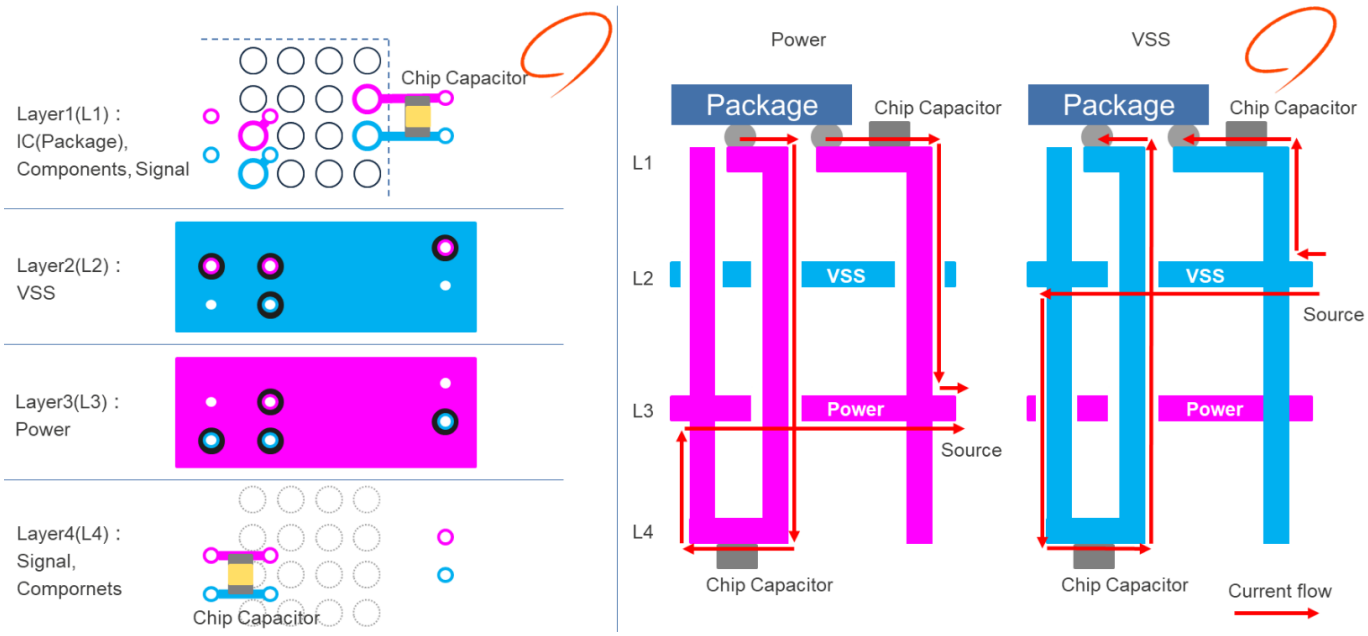


Figure 13, Recommended capacitor design image for Power Supply and VCL

Reset

– When connecting directly to the reset IC, place the reset IC as close to the microcontroller as possible (See Figure 14).

– When suppressing noise, it is recommended to insert a low-pass filter. (VSS shielding is not required when inserting a low-pass filter.) (See Figure 14)

– Keep a distance from other signals (especially traces with large currents and high-speed signal traces), and shield them with a VSS that is wide and has multiple THs (See Figure 14).

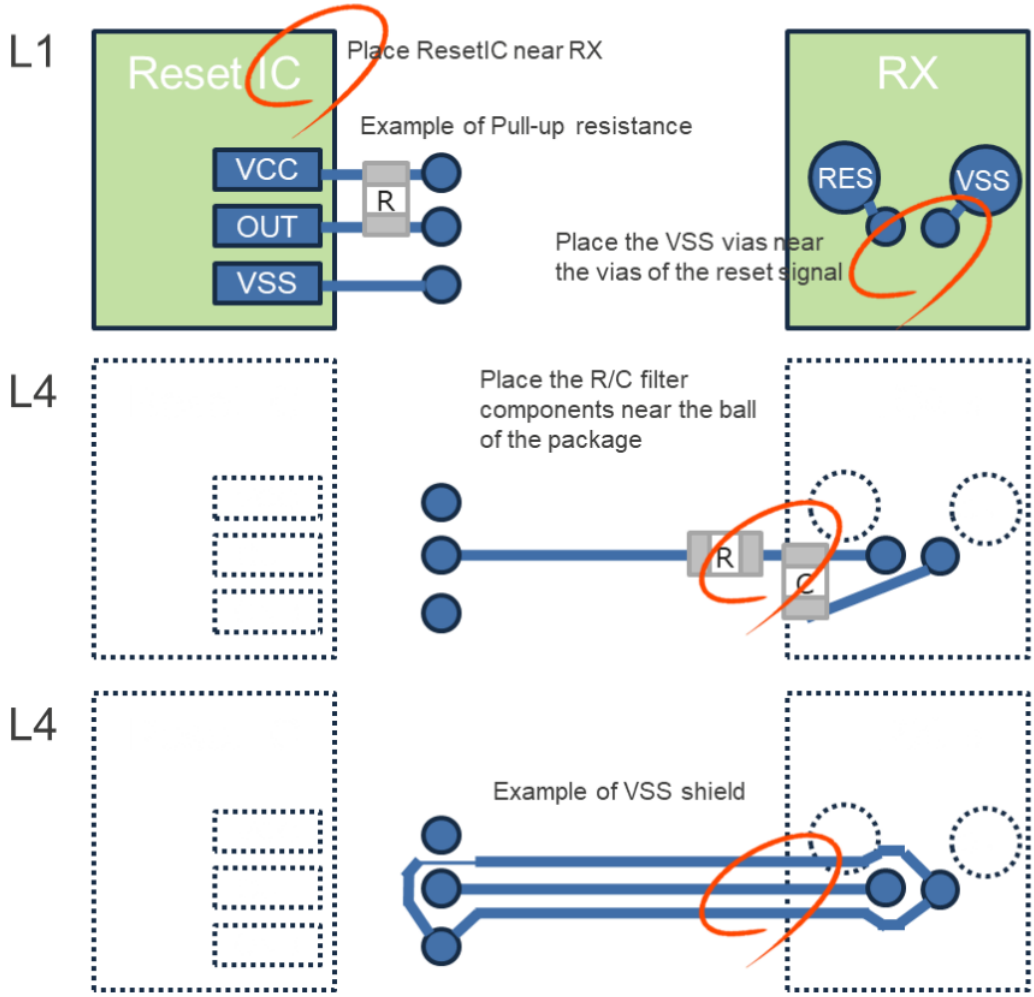


Figure 14, Recommended Design Image for Reset (Top View)

Clock

– The traces for Clock input/output terminals such as EXATL, XTAL, XCIN, XOUT, X1, X2, etc. should be as short as possible, including peripheral circuits.

– Separate these from other traces (especially traces with large currents and high-speed signals) and shield them with VSS.

– The width of the VSS shield traces should be 0.3 mm or more, and the distance between the VSS shield traces and the clock traces should be 0.3~2 mm.

– The layer below the peripheral circuit of the crystal does not allow the trace of signals, power supplies, or VSS patterns (See Figure 15).

OSC

– For external components (capacitors, resistors, etc.) when using a quartz crystal,

select the most suitable components for the crystal to be used.

– The power supply shall comply with the recommended rules for board design in Section 3.5.1.

– OSC signal trace is wired with a trace width of 0.1 mm on the microcontroller mounting surface, and VSS shielding is performed at the same layer and the bottom layer. There is nothing in the middle layer, including other signals. A distance of 0.3 mm should be maintained between OSC signal traces in the same layer and other signal traces (especially traces with large currents and high-speed signal patterns) and VSS shields. (See Figure 15)

– Place the crystal as close as possible to the terminals (within 10 mm). (See Figure 15)

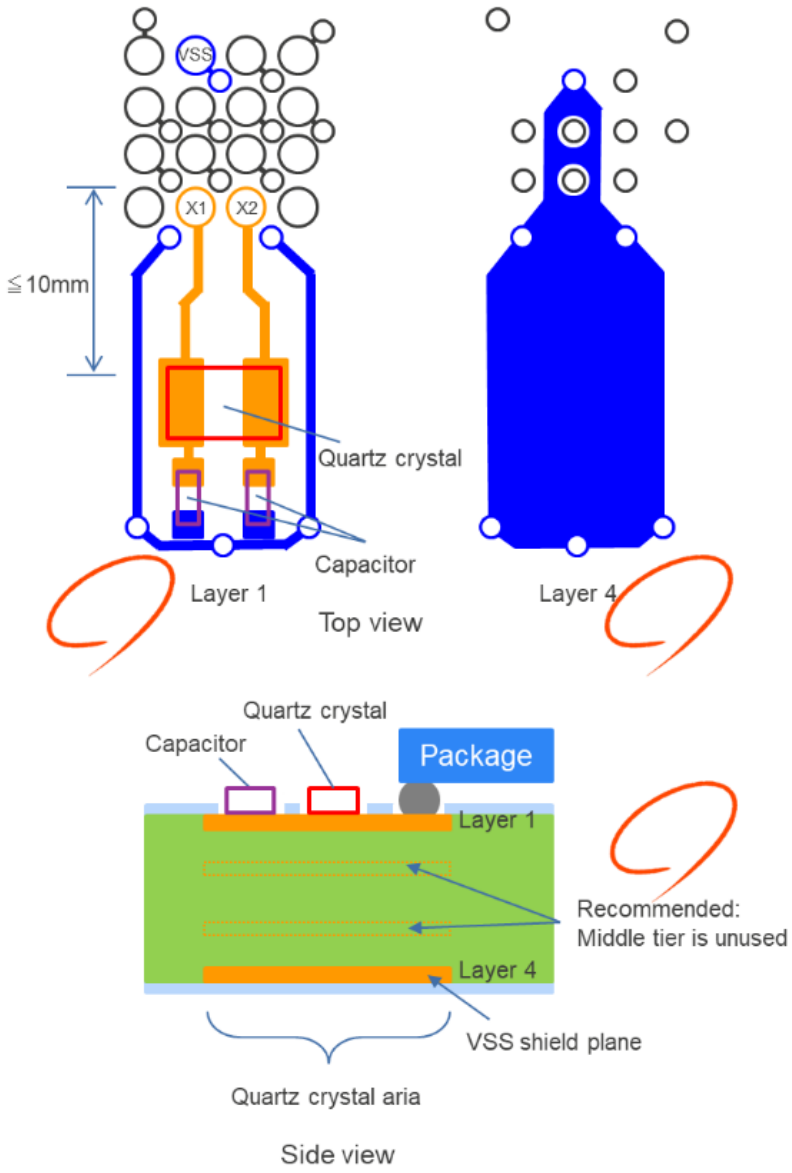


Figure 15, Recommended design image of OSC

USB

– The power supply shall comply with the recommended rules for board design in Section 3.5.1. However, the USB VSS is separated from the others and shorted at one point.

– The RREF resistor is placed in the vicinity of the IC/package, but not in parallel with the capacitor.

– Trace including RREF resistors is shielded with USBAVSS across the same layer and adjacent layers. If it cannot be shielded, it should not be adjacent to other signals or paralleled. Do not cross as much as possible. Space out as much as possible.

– Differential signals (DP, DM) are designed with a differential impedance of 90 Ω ±10% and are wired in pairs (same length, parallel, same width, same number of bends, same number of THs). The approximate trace length difference is within 2 mm (See Figure 16). Shield with USB VSS. If it is not possible to shield, do not space it from other signals (especially traces with large currents or high-speed signal patterns) or parallel them. Do not cross as much as possible. Slots/slits in adjacent layers should also be avoided.

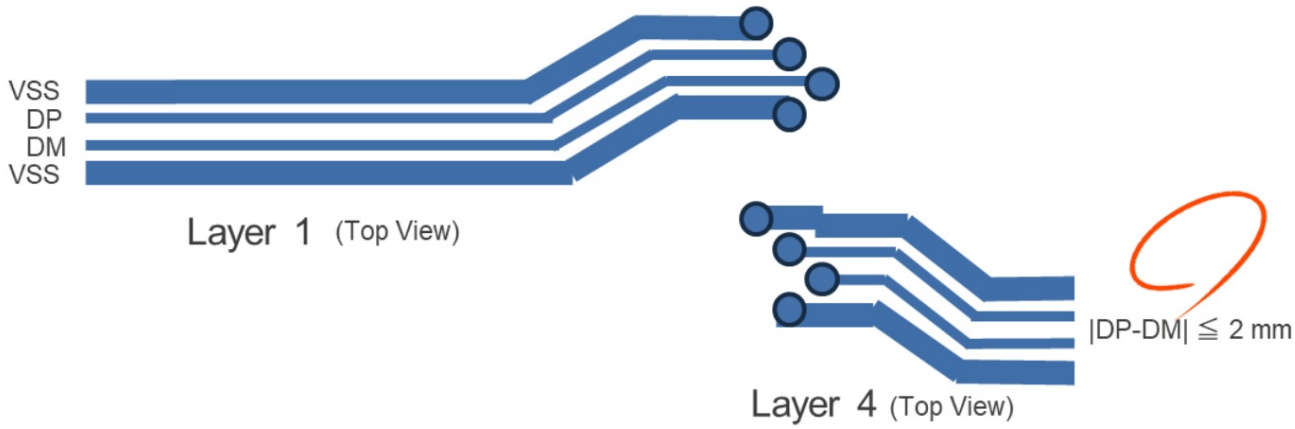


Figure 16, Recommended Design Diagram for Differential Signals

Analog

– The signal trace of the analog terminal is the same layer as the power supply/VSS/other signals (especially traces with large currents and high-speed signal patterns) with a Min trace width and /Space out adjacent layers, stop paralleling, and shield with analog VSS. The width of the analog VSS shield trace should be at least

three times the width of the analog signal trace, and the distance between the analog signal trace and the analog VSS shield should be three times the trace width or three times that of the adjacent layers (See Figure 17).

– When inserting a low-pass filter, follow the specifications of the analog to be implemented.

Figure 17, Recommended design image: Example of shielded trace Top View)

Example of board layout around BGA package

In accordance with the basic board layout concept in Section 3.4 and the recommended rules for board design in Section 3.5, examples of TH position and Layer 1 and Layer 4 layout that also take into account components placement (not shown) are shown in Figure 18 (example of RA6Mx/64BGA) and Figure 19 (example of RA6Mx/144BGA). For the power supply, it is recommended to consider the TH arrangement so that it is adjacent to the VSS so that the required number of capacitors can be mounted on the Layer 4 in the immediate vicinity of the ball. The magenta-colored circle in the figure is an example of a pair of TH of the power supply and VSS.

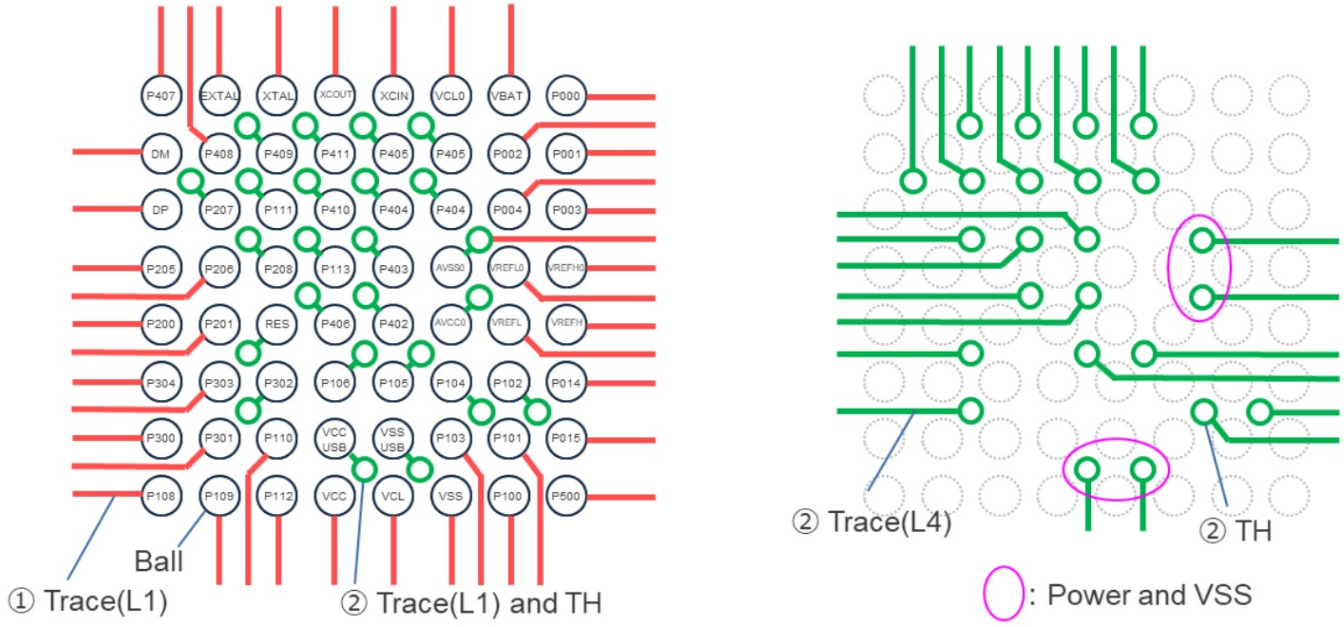


Figure 18, Example of layout for Layer 1 and Layer 4 of a 64 (8×8) BGA full grid (Top View)

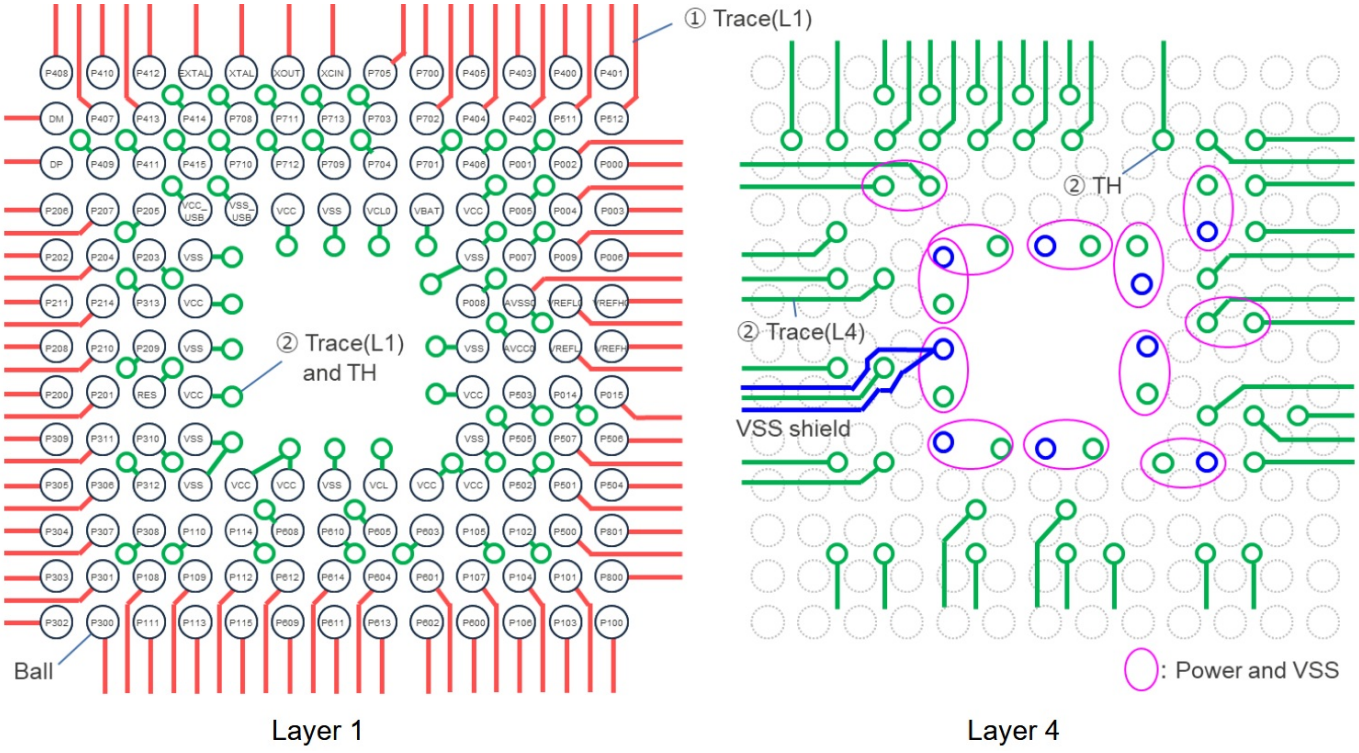


Figure 19, Example of layout for Layer 1 and 4 of a 144(13×13) BGA outer perimeter 4 rows (Top View)

Revision history

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 23, 2024	-	First release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

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