

onsemi UM70096-D FUSB15201P Dual Port USB Type-C-PD Controller One-Tim User Manual

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FUSB15201P Dual Port USB Type-C/PD Controller One-Time Programming Guide UM70096/D



Figure 1. FUSB15201P24LGEVB, FUSB15201P32LGEVB

Contents

- 1 Introduction
- 2 Required Software
- 3 Programming the OTP
- 4 Documents /

Resources

- 4.1 References
- **5 Related Posts**

Introduction

The FUSB15201P Evaluation Board (EVB), together with the firmware binary provided in the release package, permits a customer to program the one–time programmable (OTP) non–volatile memory (NVM) of the FUSB15201P.

Required Hardware and Setup Instructions

The following hardware is required:

- (A) FUSB15201P Evaluation Board (EVB)
- (B) 64KB OTP Chip labeled FUSB15201P24L or FUSB15201P32L
- (C) SEGGER J-Link Pro JTAG/SWD Programming and Debug Probe
- (D) 9-Pin Cortex-M Adapter to connect (A) the EVB to (C) J-Link Pro
- (E) External Power Supply capable of providing 60 W

To set up the hardware, refer to the itemized hardware list above and perform these steps:

- 1. Make sure the EVB is configured for SWD. Install R48 (0 Ω) resistor on the board.
- 2. Use (D) the 9-pin adapter to connect (C) the J-Link Pro to the SWD connector (J5) on the socket EVB as shown in Figure 2.

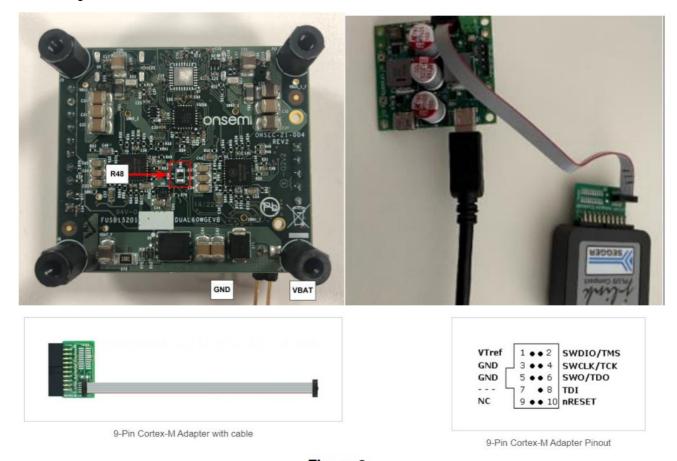


Figure 2.

3. Setup the power supply to 12 V (~200 mA) and connect the positive and negative jumpers on the board.

UM70096/D

Required Software

a. SEGGER J-Link Tools

Download and install the J-Link Software and Documentation Pack Note: Please make sure SEGGER J-Flash is installed.

- b. FUSB15201P SWD Converter Tool Please download and install the FUSB15201P SWD Converter tool Note: Search for keyword FUSB15201P SWD Converter Tool.
- c. FUSB15201P Flash Loader Download the FUSB15201P Flash Loader used by J-Link to flash the EVB. Search for file FUSB15201P_FLASH_LOADER.ELF. Further instructions on where to place this file are indicated in the subsequent paragraph.
- d. FUSB15201P NVR Loader Download the FUSB15201P NVR Loader used by J-Link to load data onto the EVB. Search for file FUSB15201P_NVR_LOADER.ELF. Further instructions on where to place this file are indicated in the subsequent paragraph.
- e. FUSB15201P Device List AddOn Download the FUSB15201P Device AddOn to add the FUSB15201 to the J-Link device list. Search for file FUSB15201P_XML_ADDON.TXT.

Adding FUSB15201P Support to J-Link

To allow FUSB15201P to support J-Link, add the FUSB15201P to the list of J-Link supported devices. J-Link provides a device list in xml format. Add the FUSB15201P to this list, as follows:

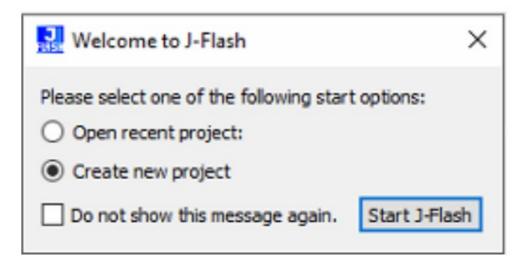
1. Create a directory named onsemi\FUSB15201P here:C:\Users\<USER_NAME>\AppData\Roaming\SE GGER\JLinkDevices\onsemi\FUSB15201P.

- 2. Copy the two files (c.) and (d.) shown in section Required Software, above, into C:\Users\ <USER_NAME>\AppData\Roaming\SE GGER\JLinkDevices\onsemi\FUSB15201P.
- 3. Rename file (e.) to Devices.xml and copy into C:\Users\<USER_NAME>\AppData\Roaming\SE GGER\JLinkDevices\onsemi\FUSB15201P.

Programming the OTP

Complete the following steps to program the EVB:

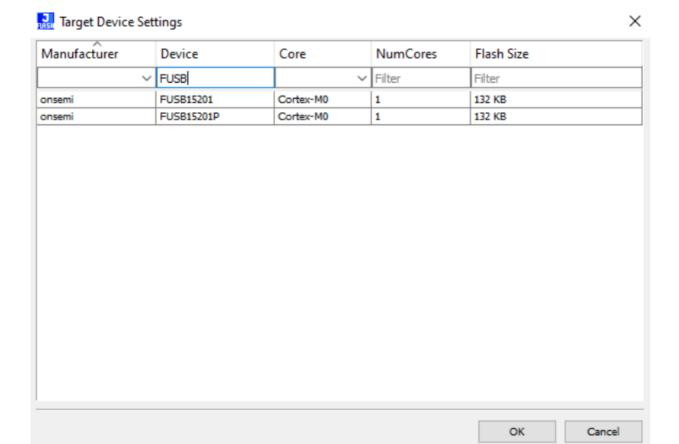
- 1. Connect J-Link to the EVB:
 - Open the SEGGER J-Flash and select Create new project, then select Start J-Flash.



• Click on the selection box (shown with a red outline below).



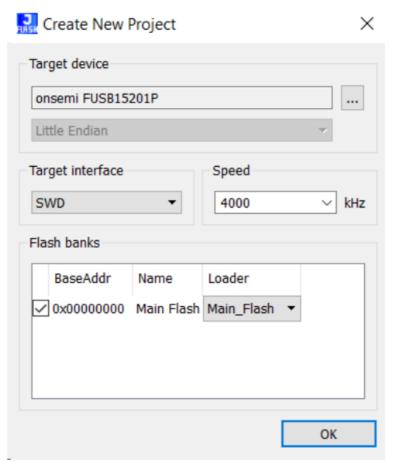
• Select FUSB15201P.



• Select Target interface: SWD.

• Select Speed: 4000 kHz.

• Click OK for the new project to be created.



- From the menu, choose Target.
- From the resulting window, choose Connect.

If the connection is established, the log shows a message indicating a successful connection.

Log

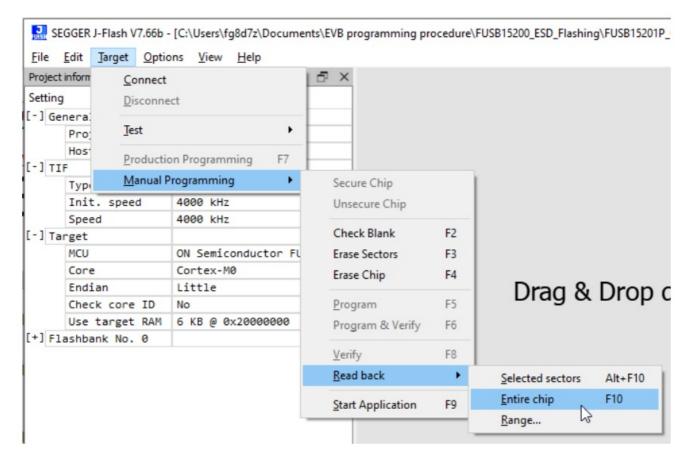
- CoreSight SoC-400 or earlier - Scanning AP map to find all available APs - AP[1]: Stopped AP scan as end of AP map has been reached - AP[0]: AHB-AP (IDR: 0x04770031) - Iterating through AP map to find AHB-AP to use - AP[0]: Core found - AP[0]: AHB-AP ROM base: 0xE00FF000 - CPUID register: 0x410CC601. Implementer code: 0x41 (ARM) - Found Cortex-M0 r0p1, Little endian. - FPUnit: 4 code (BP) slots and 0 literal slots CoreSight components: - ROMTb1[0] @ E00FF000 - [0][0]: E000E000 CID B105E00D PID 000BB008 SCS - [0][1]: E0001000 CID B105E00D PID 000BB00A DWT - [0][2]: E0002000 CID B105E00D PID 000BB00B FPB - Executing init sequence ... Initialized successfully - Target interface speed: 4000 kHz (Fixed) - Found 1 JTAG device. Core ID: 0x0BC11477 (None)

Ready

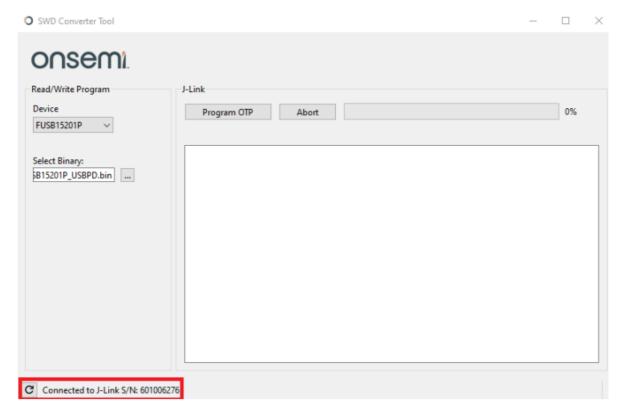
- 2. Verify that the chip is blank:
 - From the menu, choose Target.
 - From the resulting window, choose Manual Programming.
 - Select Check Read back → Entire chip.

Connected successfully

J-Flash will report the the Target memory is all 0x00's.



- 3. Prepare SWD Converter to program OTP:
 - Open the SWD Converter Tool.
 - Select FUSB15201P from the Device drop down menu.
 - Select the FW .bin file to convert in the Select Binary field.
 - Click on the Refresh Connection Icon in the bottom left corner.

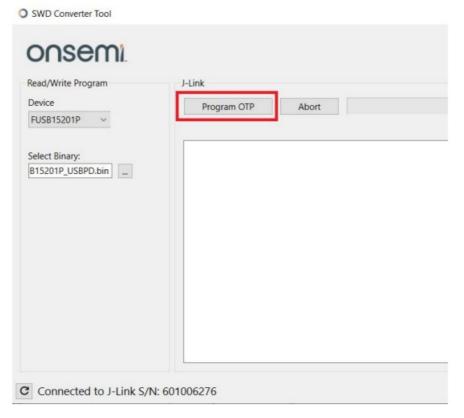


4. Program OTP:

• You can program the OTP by clicking the Program OTP button.

A Message on the Log section shall confirm that the script processing is completed and the OTP programmed

successfully.



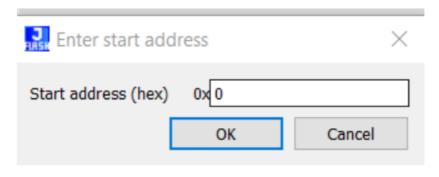
- 5. Validate OTP programmed successfully on the chip:
 - From the menu, choose Target.
 - From the resulting menu, click Connect.

If the connection is established, you should see a message on the Log indicating a successful connection.

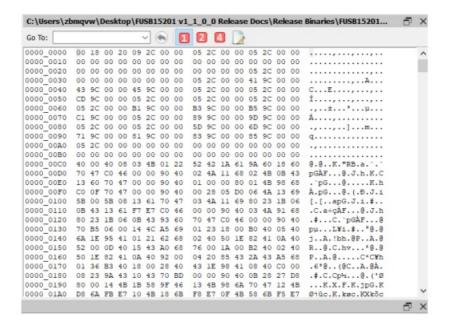
```
Log

- AP[0]: AHB-AP (IDR: 0x04770031)
- Iterating through AP map to find AHB-AP to use
- AP[0]: Core found
- AP[0]: AHB-AP ROM base: 0xE00FF000
- CPUID register: 0x410CC601. Implementer code: 0x41 (ARM)
- Found Cortex-M0 r0p1, Little endian.
- FPUnit: 4 code (BP) slots and 0 literal slots
- Coresight components:
- ROMTbl[0] @ E00FF000
- ROMTbl[0][0]: E000E000, CID: B105E000, PID: 000BB008 SCS
- ROMTbl[0][1]: E0001000, CID: B105E000, PID: 000BB00A DWT
- ROMTbl[0][2]: E0002000, CID: B105E00D, PID: 000BB00B FPB
- Executing init sequence ...
- Initialized successfully
- Target interface speed: 4000 kHz (Fixed)
- Found 1 JTAG device. Core ID: 0x0BC11477 (None)
- Connected successfully
```

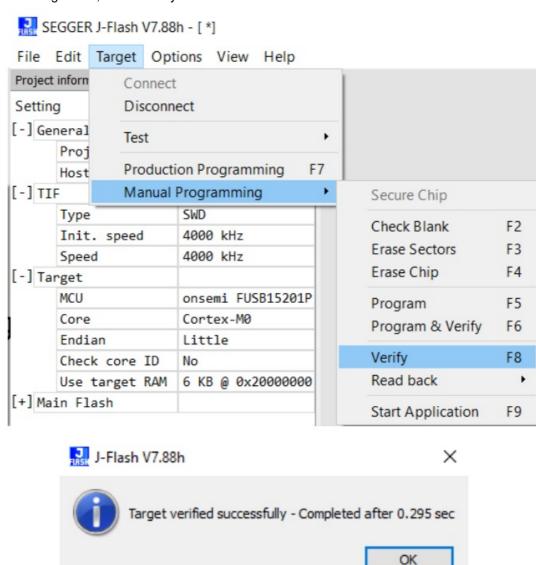
- Drag the .bin file into the J-Flash Window.
- J-Flash will ask for a start address. Enter 0 and click OK.



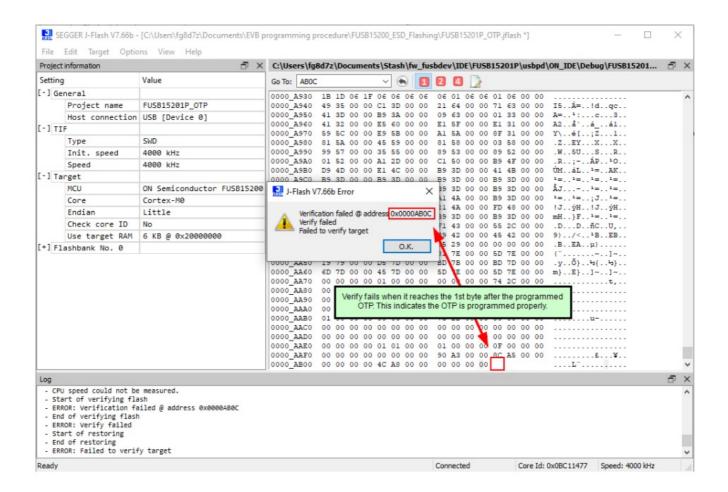
• J-Flash will show the file in Hexadecimal format.



- From the J-Flash Menu, go to Target.
- From the resulting menu, go to Manual Programming.
- From the resulting Menu, select Verify.



the OTP has actually been successfully programmed up to the end of the .bin:



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UM70096-D FUSB15201P Dual Port USB Type-C-PD Controller One-Tim, UM70096-D, FUSB1 5201P Dual Port USB Type-C-PD Controller One-Tim

References

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- O Sales Offices & Distributor Network
- 9-Pin Cortex-M Adapter (8.06.02) SEGGER U.S. Web Shop
- O Intelligent Power and Sensing Technologies | onsemi
- O Technical Documentation
- O Support
- O Sales Offices & Distributor Network
- SEGGER The Embedded Experts Downloads J-Link / J-Trace

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