onsemi NC7SZ32M5X 2 Input OR Logic Gate Instructions

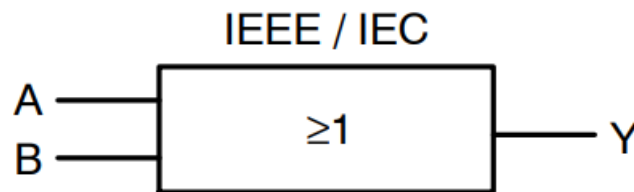**TinyLogic UHS Two-Input
OR Gate
NC7SZ32**

Contents

Description

The NC7SZ32 is a single two−input OR gate from onsemi's Ultra−High Speed (UHS) series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra−high speed with high output drive while maintaining low static power dissipation over a broad VCC operating range. The device is specified to operate over the 1.65 V to 5.5 V VCC operating range. The inputs and output are high impedance when VCC is 0 V. Inputs tolerate voltages up to 5.5 V, independent of VCC operating voltage.
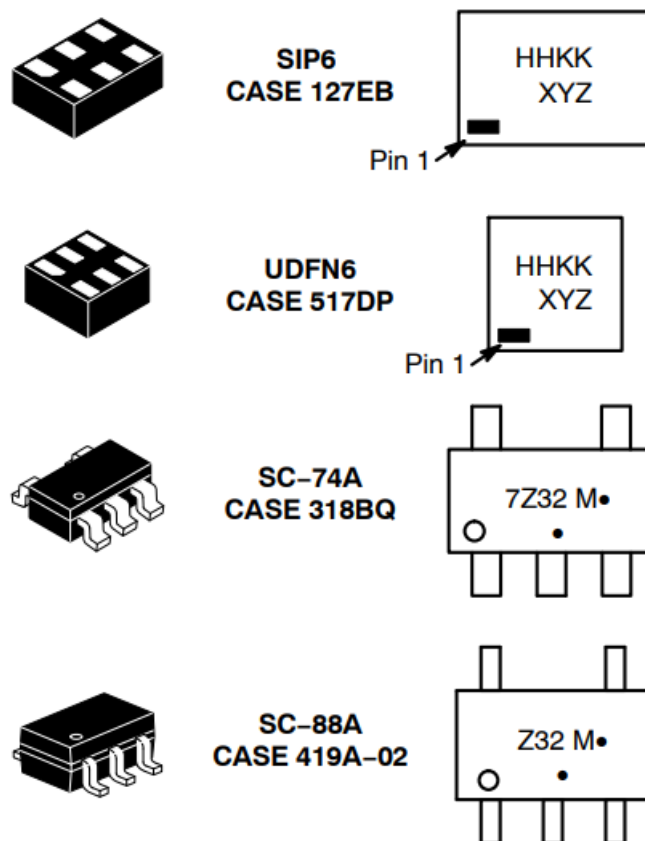
Features

- Ultra−High Speed: tPD = 2.4 ns (Typical) into 50 pF at 5 V VCC

- High Output Drive: ±24 mA at 3 V VCC

- Broad VCC Operating Range: 1.65 V to 5.5 V

- Matches Performance of LCX Operated at 3.3 V VCC

- Power Down High−Impedance Inputs / Outputs

- Over−Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation

- Proprietary Noise / EMI Reduction Circuitry

- Ultra−Small MicroPak™ Packages

- Space−Saving SC−74A and SC−88A Packages

- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

IEEE / IEC

≥1

A
B
Y

Figure 1. Logic Symbol

MARKING DIAGRAMS

SIP6
CASE 127EB

HHKK
XYZ

Pin 1

UDFN6
CASE 517DP

HHKK
XYZ

Pin 1

SC−74A
CASE 318BQ

7Z32 M•

SC−88A
CASE 419A−02

Z32 M•

HH, 7Z32, Z32 = Specific Device Code
KK = 2−Digit Lot Run Traceability Code
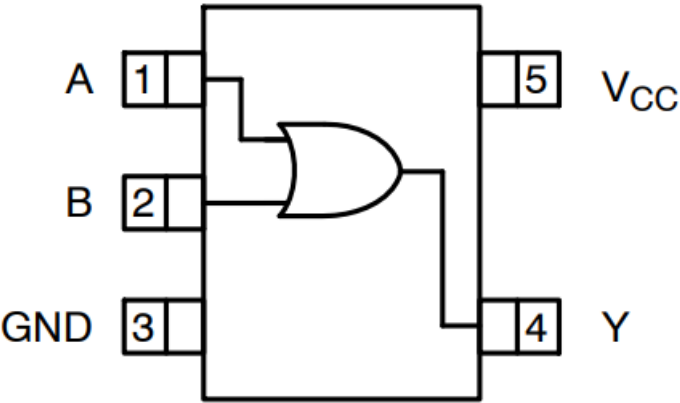XY = 2−Digit Date Code Format
Z = Assembly Plant Code
M = Date Code

• = Pb−Free Package
(Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.
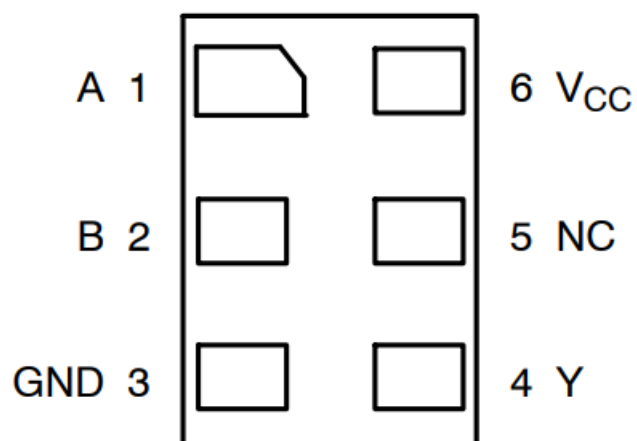
NC7SZ32

Pin Configurations

Figure 2. SC−88A and SC−74A (Top View)

PIN DEFINITIONS

Pin # SC−88A / SC74A	Pin # MicroPak	Name	Description
1	1	A	Input
2	2	B	Input
3	3	GND	Ground
4	4	Y	Output
5	6	VCC	Supply Voltage
	5	NC	No Connect

Figure 3. MicroPak (Top Through View)

A 1 □ □ 6 V$_{CC}$
B 2 □ □ 5 NC
GND 3 □ □ 4 Y

FUNCTION TABLE ($Y = A + B$ **)**

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
Vcc	Supply Voltage		-1.	7.	V
VIN	DC Input Voltage		-1.	7.	V
VOUT	DC Output Voltage		-1.	7.	V
11K	DC Input Diode Current	VIN < 0 V		-50	mA
10K	DC Output Diode Current	VOUT < 0 V		-50	mA
lour	DC Output Current			±50	mA
Icy or IGND	DC Vcc or Ground Current			±50	mA
TSTG	Storage Temperature Range		-65	+150	
T j	Junction Temperature Under Bias			+150	
TL	Junction Lead Temperature (Soldering, 10 Seconds)			+260	
PD	Power Dissipation in Still Air	SC-74A		390	mW
		SC-88A		332	
		MicroPak-6		812	
		MicroPak2TM-6		812	
ESD	Human Body Model, JEDEC: JESD22-A114			4000	V
	Charge Device Model, JEDEC: JESD22-C101			2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage Operating		2.	5.50	V
	Supply Voltage Data Retention		1.50	5.50	
VIN	Input Voltage		0	6.	V
VouT	Output Voltage		0	Vcc	V
TA	Operating Temperature		-40	+85	
tr, tf	Input Rise and Fall Times	Vcc = 1.8 V, 2.5 V ±0.2 V	0	20	nsN
		Vcc = 3.3 V ±0.3 V	0	10	
		Vcc = 5.0 V ±0.5 V	0	5	
OJA	Thermal Resistance	SC-74A	–	320	C/W
		SC-88A	–	377	
		MicroPak-6	–	154	
		MicroPak2-6	–	154	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTICAL CHARACTERISTICS

Symbol	Parameter	VCC (V)	Conditions	TA = +25 C			TA = -40 to +85° C		Unit
				Min	Typ	Max	Min	Max	
VIH	HIGH Level Input Voltage	1.65 to 1.95		0.65 VCC	–	–	0.65 VCC	–	V
		2.30 to 5.50		0.70 VCC	–	–	0.70 VCC	–	
VI	LOW Level Input Voltage	1.65 to 1.95		–	–	0.35 Vcc	–	0.35 VCC	V
		2.30 to 5.50		–	–	0.30 Vcc	–	0.30 VCC	
		2.	VIN = Vol Or VI , IOH = -100 N A	2.	2.	–	2.	–	
		1.80		1.70	1.80	–	1.70	–	
		2.30		2.20	2.30	–	2.20	–	
		3.00		2.90	3.00	–	2.90	–	
		4.50		4.40	4.50	–	4.40	–	

VOH	HIGH Level Output Voltage	2.	10H = -4 mA	1.	2.	–	1.	–	V
		2.30	10H = -8 mA	1.90	2.	–	1.90	–	
		3.00	101.1= -16 mA	2.40	2.80	–	2.40	–	
		3.00	101.1= -24 mA	2.30	3.	–	2.30	–	
		4.50	10H = -32 mA	3.80	4.20	–	3.80	–	
VOL	LOW Level Output Voltage	2.	VIN = Vol Or VI, 10L = 100 IA A	–	0.00	0.10	–	0.10	V
		1.80		–	0.00	0.10	–	0.10	
		2.30		–	0.00	0.10	–	0.10	
		3.00		–	0.00	0.10	–	0.10	
		4.50		–	0.00	0.10	–	0.10	
		2.	loi = 4 mA	–	0.80	0.24	–	0.24	
		2.30	la = 8 mA	–	0.10	0.30	–	0.30	
		3.00	10L = 16 mA	–	0.15	0.40	–	0.40	
		3.00	10L = 24 mA	–	0.22	0.55	–	0.55	
		4.50	10L = 32 mA	–	0.22	0.55	–	0.55	
liN	Input Leakage Current	1.65 to 5.50	VIN = 5.5 V, GND	–	–	+1	–	±10	µA
IOFF	Power Off Leakage Current	0	VIN or Vou-r = 5.5 V	–	–	1	–	10	µA
IOC	Quiescent Supply Current	1.65 to 5.50	VIN = 5.5 V, GND	–	–	2.0	–	20	µA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Vcc (V)	Conditions	TA = +25 C			TA = -40 to +85 C		Unit
				Min	Typ	Max	Min	Max	
tPLH, tpHL	Propagation Delay (Figure 4, 5)	2.	CL = 15 pF, FiL = 1 MQ		6.	12.0		13.	ns
		1.80			5.	10.0		11.	
		2.50 ±0.30			3.0	7.0		8.	
		3.30 ±0.30			2.	5.		5.0	
		5.00 ±0.50			2.	4.		4.	
		3.30 ±0.30	CI_ = 50 pF, IRL = 500 Q		3.0	5.		6.	
		5.00 ±0.50			2.	5.		5.	
CIN	Input Capacitance	0.00			4				pF
Opp	Power Dissipation Capacitance (Note 2) (Figure 6)	3.30			20				pF
		5.00			26				

2. CPD is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (ICCD) at no output loading and operating at 50% duty cycle. CPD is related to ICCD dynamic operating current by the expression: ICCD = (CPD) (VCC) (fIN) + (ICCstatic).
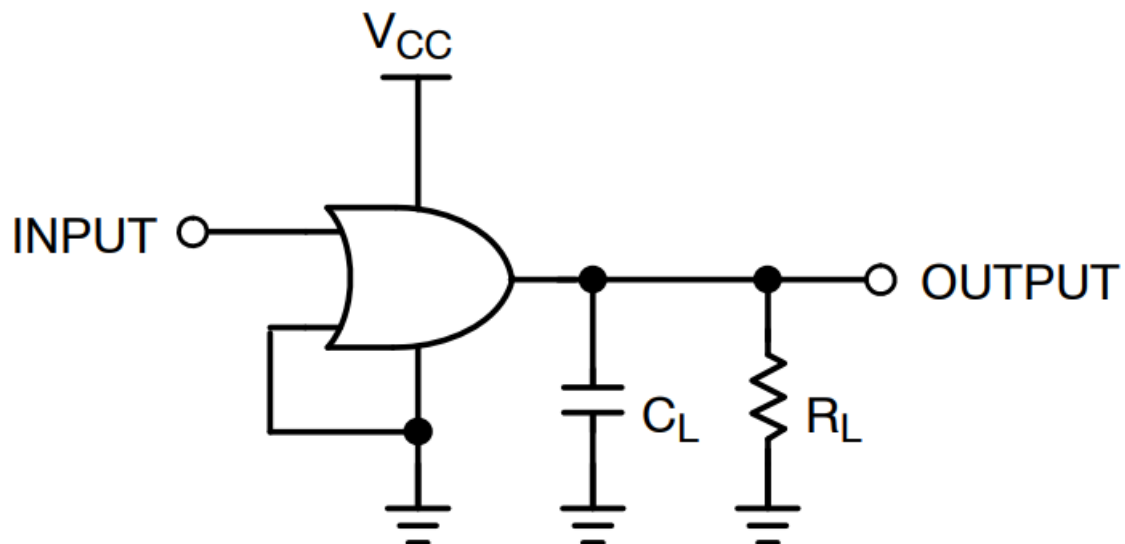
NOTE:
3. CL includes load and stray capacitance.
Input PRR = 10 MHz, tw = 500 ns
Figure 4. AC Test Circuit
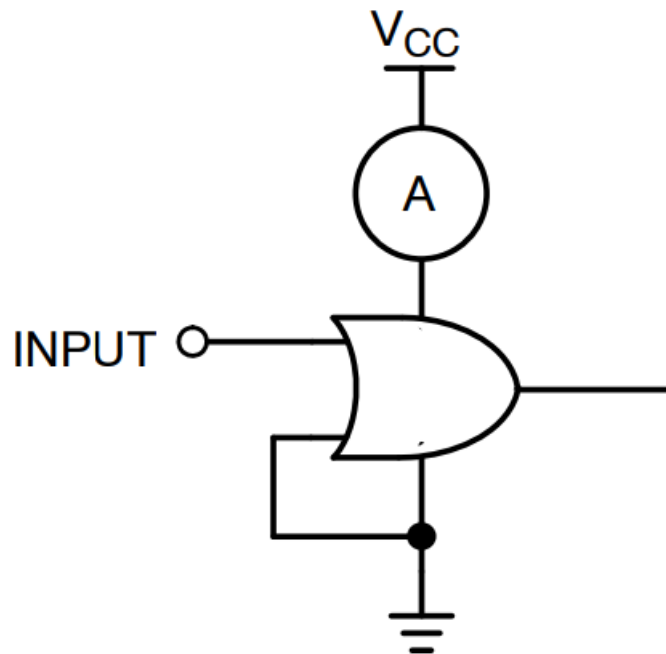
NOTE:
4. Input = AC Waveform; tr = tf = 1.8 ns; PRR = 10 MHz; Duty Cycle = 50%.
Figure 6. ICCD Test Circuit
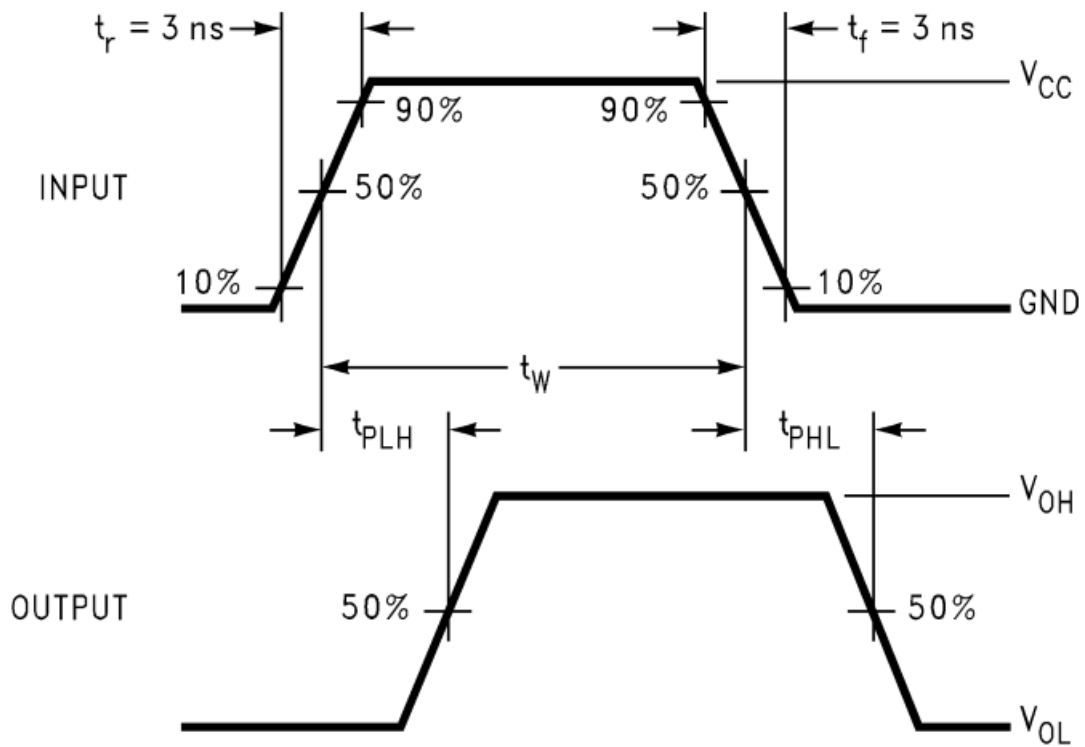
Figure 5. AC Waveforms

ORDERING INFORMATION

Part Number	Top Mark	Packages	Shippingt
NC7SZ32M5X	7232	SC-74A	3000 / Tape & Reel
NC7SZ32P5X	Z32	SC-88A	3000 / Tape & Reel
NC7SZ32P5X-F22057	Z32	SC-88A	3000 / Tape & Reel
NC7SZ32L6X	HH	SIP6, MicroPak	5000 /Tape & Reel
NC7SZ32L6X-L22175	HH	SIP6, MicroPak	5000 /Tape & Reel
NC7SZ32FHX	HH	UDFN6, MicroPak2	5000 /Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016
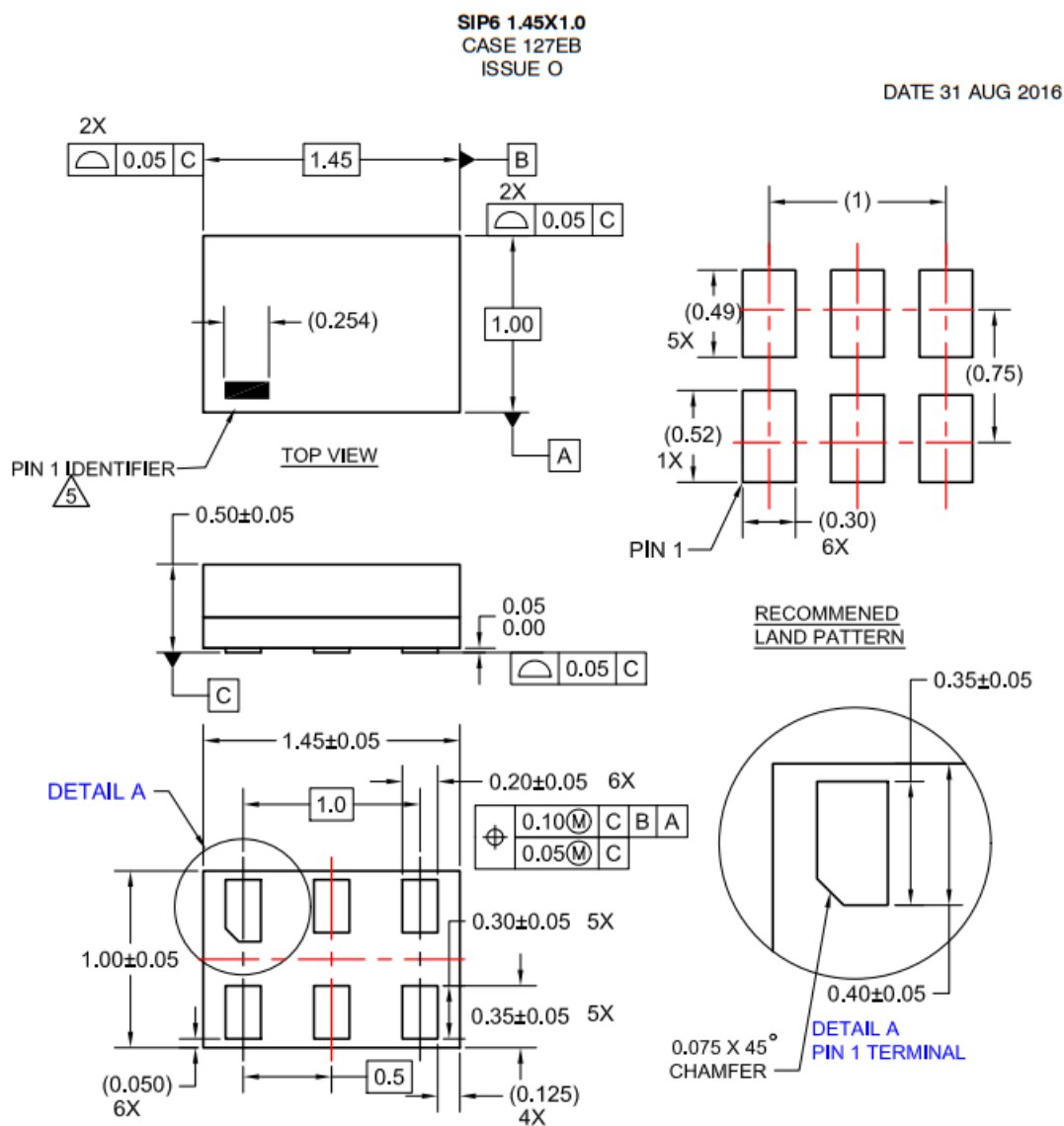
BOTTOM VIEW
NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD

2. DIMENSIONS ARE IN MILLIMETERS

3. DRAWING CONFORMS TO ASME Y14.5M-2009

4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

SC−74A
CASE 318BQ
ISSUE B

5
1
SCALE 2:1

5X **b**

⊕ | 0.20 | C | A | B

E1
B
A
5
4
○1
2
3
E
D
e
TOP VIEW

△ | 0.05
A1
L
M
DETAIL A

A
C | SEATING PLANE
SIDE VIEW
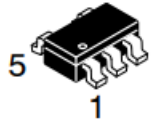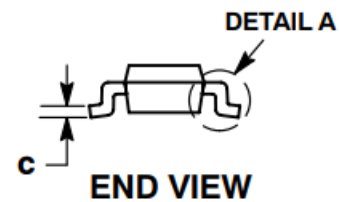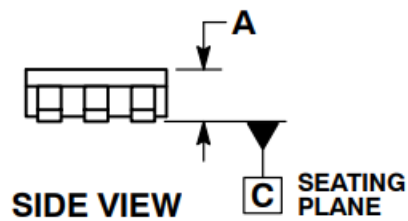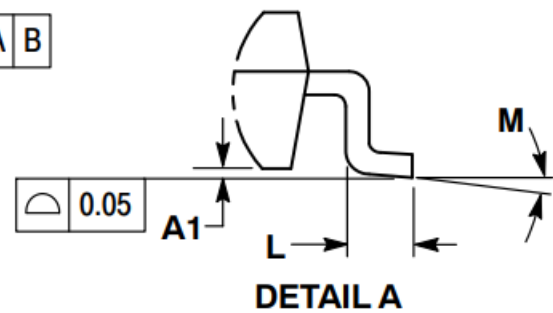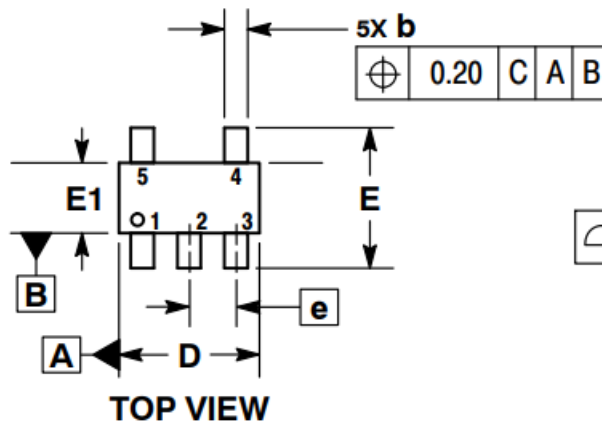
DETAIL A
c
END VIEW

RECOMMENDED SOLDERING FOOTPRINT*

0.95
PITCH

2.40

5X
1.00

5X
0.70

DIMENSIONS: MILLIMETERS
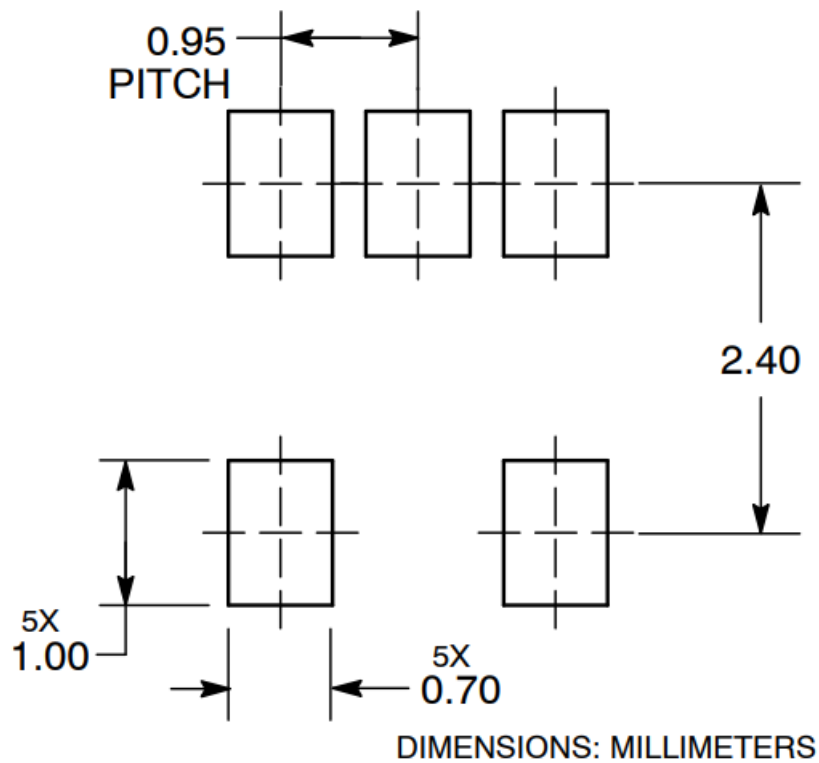
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
DATE 18 JAN 2018

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
Al	0.01	0.10
b	0.25	0.50
C	0.10	0.26
D	3.	3.
E	2.50	3.00
El	1.	2.
e	0.95 BSC	
L	0.20	0.60
M	0°	10°

GENERIC MARKING DIAGRAM*
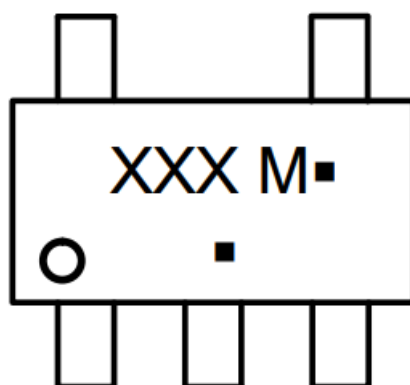
XXX = Specific Device Code
M = Date Code
■ = Pb−Free Package
(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.
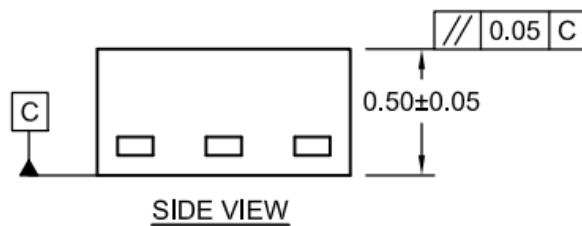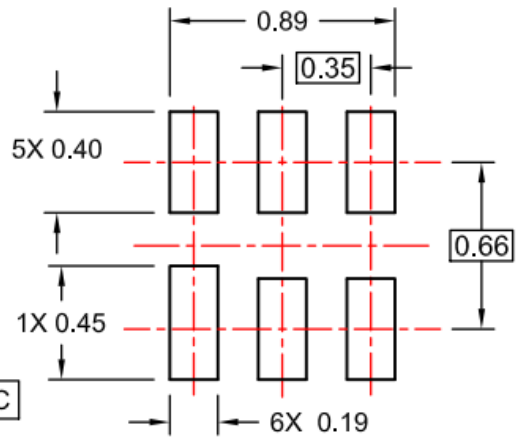**SC−88A (SC−70−5/SOT−353)**
CASE 419A−02
ISSUE L

SCALE 2:1

A

G

S

5   4

1   2   3

–B–

D 5 PL | ⊕ | 0.2 (0.008) Ⓜ | B Ⓜ |

N

C

H

J

K

SOLDER FOOTPRINT

SCALE 20:1 $\left(\dfrac{\text{mm}}{\text{inches}}\right)$
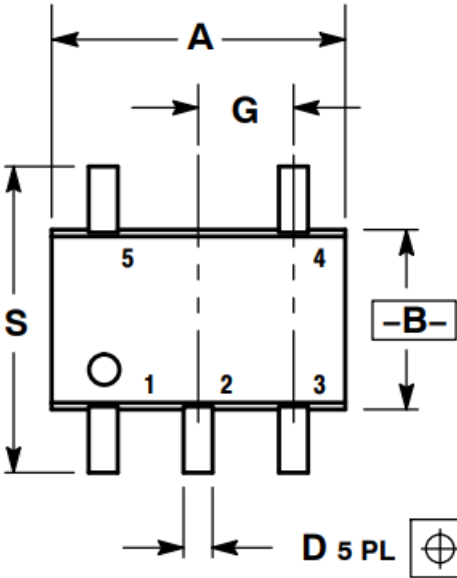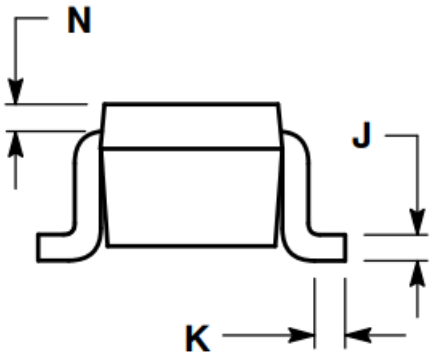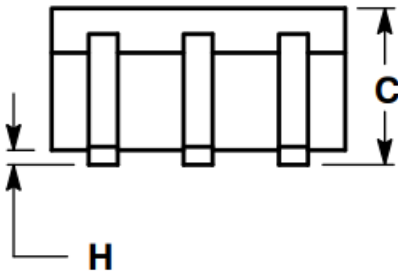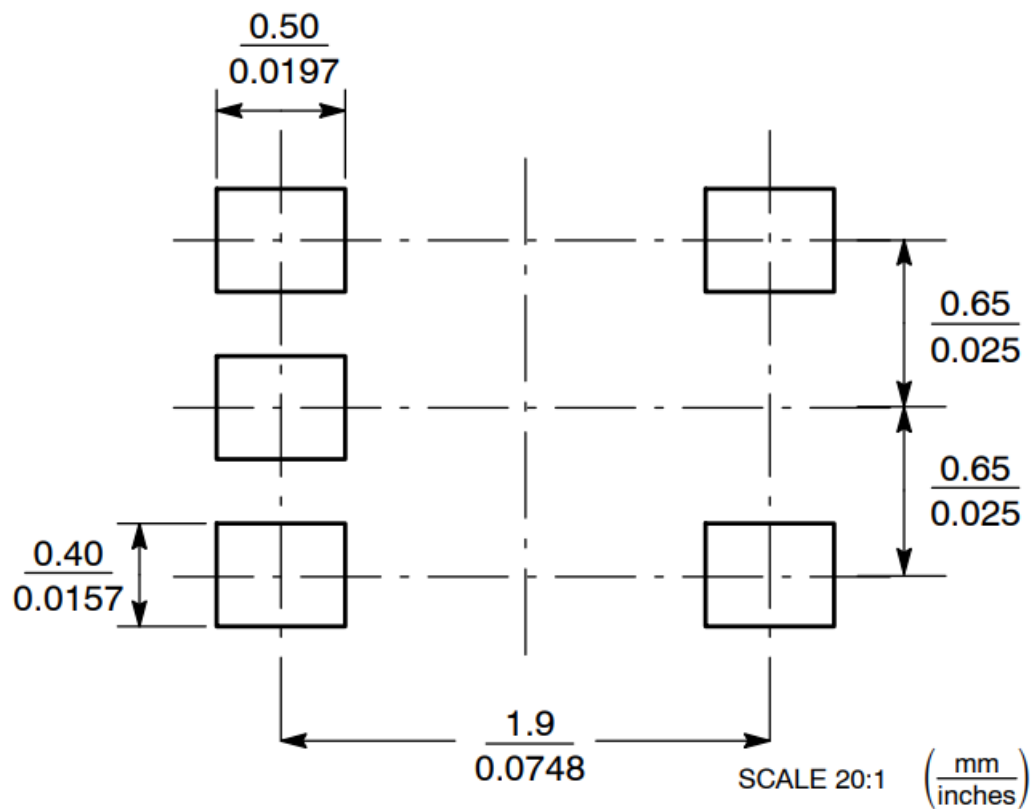
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A–01 OBSOLETE. NEW STANDARD 419A–02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.	1.
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	—	0.004	—	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	I 2.20

GENERIC MARKING DIAGRAM*

XXXM■

XXX = Specific Device Code
M = Date Code
■ = Pb–Free Package
(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 2: PIN 1. ANODE 2. EMITTER 3. BASE 4. COLLECTOR 5. CATHODE	STYLE 3: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. CATHODE 1	STYLE 4: PIN 1. SOURCE 1 2. DRAIN 1/2 3. SOURCE 1 4. GATE 1 5. GATE 2	STYLE 5: PIN 1. CATHODE 2. COMMON ANODE 3. CATHODE 2 4. CATHODE 3 5. CATHODE 4
STYLE 6: PIN 1. EMITTER 2 2. BASE 2 3. EMITTER 1 4. COLLECTOR 5. COLLECTOR 2/BASE 1	STYLE 7: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 8: PIN 1. CATHODE 2. COLLECTOR 3. N/C 4. BASE 5. EMITTER	STYLE 9: PIN 1. ANODE 2. CATHODE 3. ANODE 4. ANODE 5. ANODE	

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

UDFN6 1.0X1.0, 0.35P
CASE 517DP
ISSUE O

DATE 31 AUG 2016

TOP VIEW

PIN 1
MIN 250uM

SIDE VIEW

DETAIL A

BOTTOM VIEW

RECOMMENDED LAND PATTERN
FOR SPACE CONSTRAINED PCB

ALTERNATIVE LAND PATTERN
FOR UNIVERSAL APPLICATION

0.075X45°
CHAMFER

DETAIL A
PIN 1 LEAD SCALE: 2X
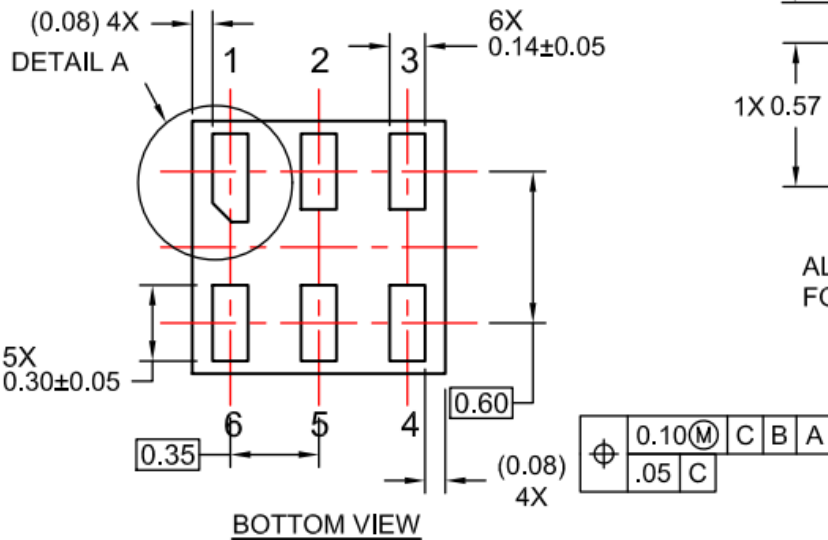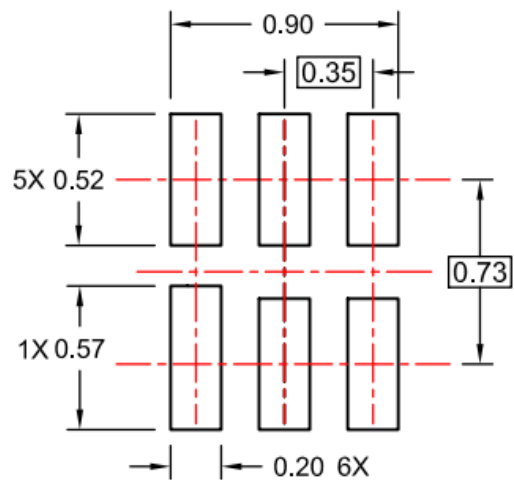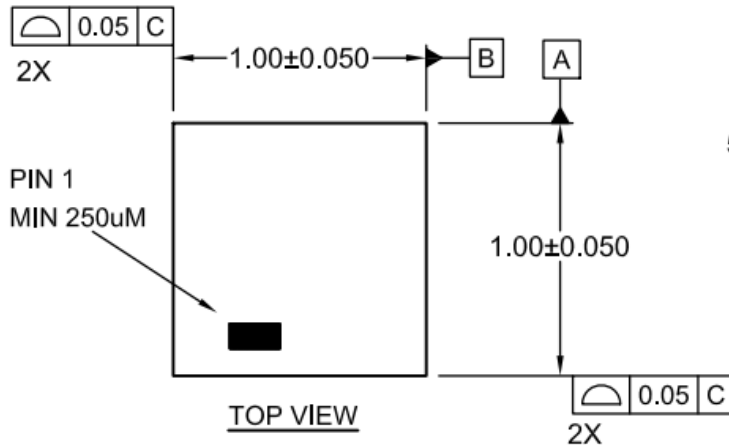
NOTES:
A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009
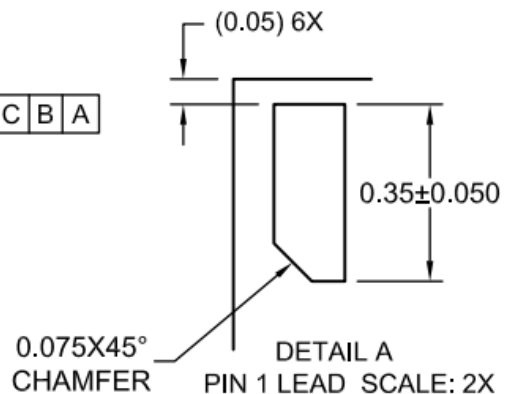
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DESCRIPTION:	UDFN6 1.0X1.0, 0.35P	PAGE 1 OF 1

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Documents / Resources

onsemi NC7SZ32M5X 2 Input OR Logic Gate [pdf] Instructions
NC7SZ32M5X 2 Input OR Logic Gate, NC7SZ32M5X, 2 Input OR Logic Gate, OR Logic Gate, Logic Gate

References

- ⃝ [Intelligent Power and Sensing Technologies | onsemi](#)