onsemi FUSB15201 Dual-Port Source USB Type-C PD Controller Evaluation Board User Manual

FUSB15201 Dual-Port Source USB Type-C PD Controller Evaluation Board User's Manual

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FUSB15201EVBUM

Introduction

The FUSB15201 evaluation board, in conjunction with firmware and software, provides a platform to evaluate a full dual−port Type−C/PD system. The FUSB15201 integrates an ARM ® Cortex−M0+ processor with customized peripherals and supports a fully standalone application with only a power supply.

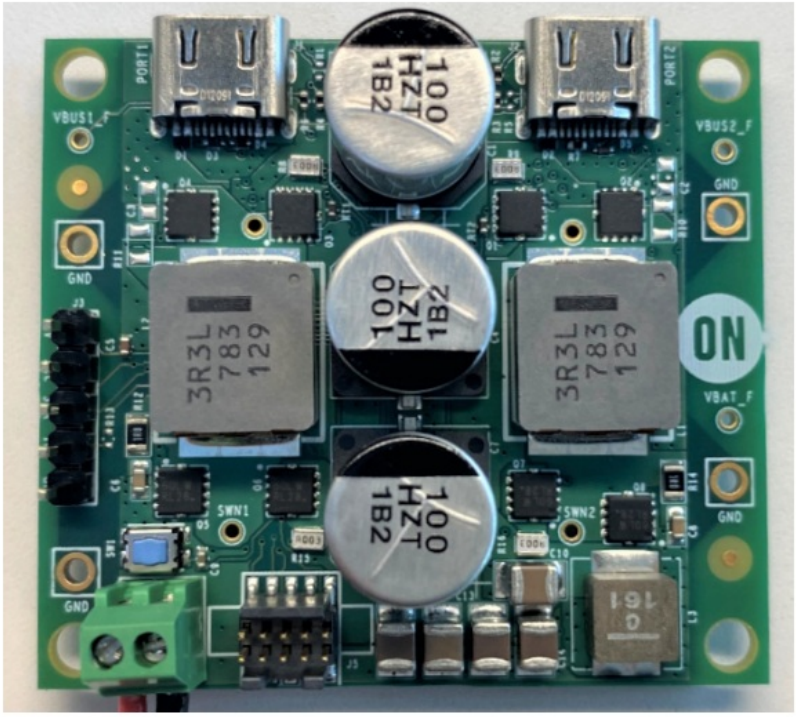


Figure 1. FUSB15201 Evaluation Board

Description

The FUSB15201 Evaluation kit is designed to support the full features of dual−port Type−C/PD Source applications for FUSB15201 with a single battery (typ 13.5 V) or power supply, primarily targeting automotive charger applications.

The Evaluation kit is designed to control two individual VBUS outputs from the NCV81599, a buck/boost DC−DC power converter.

All components are AEC-qualified.

This manual provides information about the evaluation board's interconnection, hardware setting, communication to PC, and detailed information on the board design data.

Key EVB Features

- 20 W, Configurable up to 200 W
- > 94% Efficiency
- Solution Size: 1.7" x 1.9" (20.8cm²) / 1.7" x 1.5" (16.5 cm²) ActiveArea
- Power Density: 5.77 W/cm² or 7.27 W/cm
- Highest Board Temperature: 98.061°C at 22°C Ambient at Full Load
- VBUS Output Current Sense
- VBAT Reverse Current Protection

15201 Features

- ARM Cortex−M0+ Processor
- 132 KB / 6 KB Flash Memory/SRAM
- Integrated VCONN Switch for E−Marked Cables
- Supports Low Power Mode (Idle/ Sleep)
- BC1.2 (SDP, DCP, CDP)/ Apple Divider Mode
- 10-bit ADC for Voltage and General Purpose
- Over Voltage / Over Temperature Protection

- I2C Master/Slave
- SWD Interface for Debugging
- Temperature Sensing using NTC

FUSB15201EVBUM

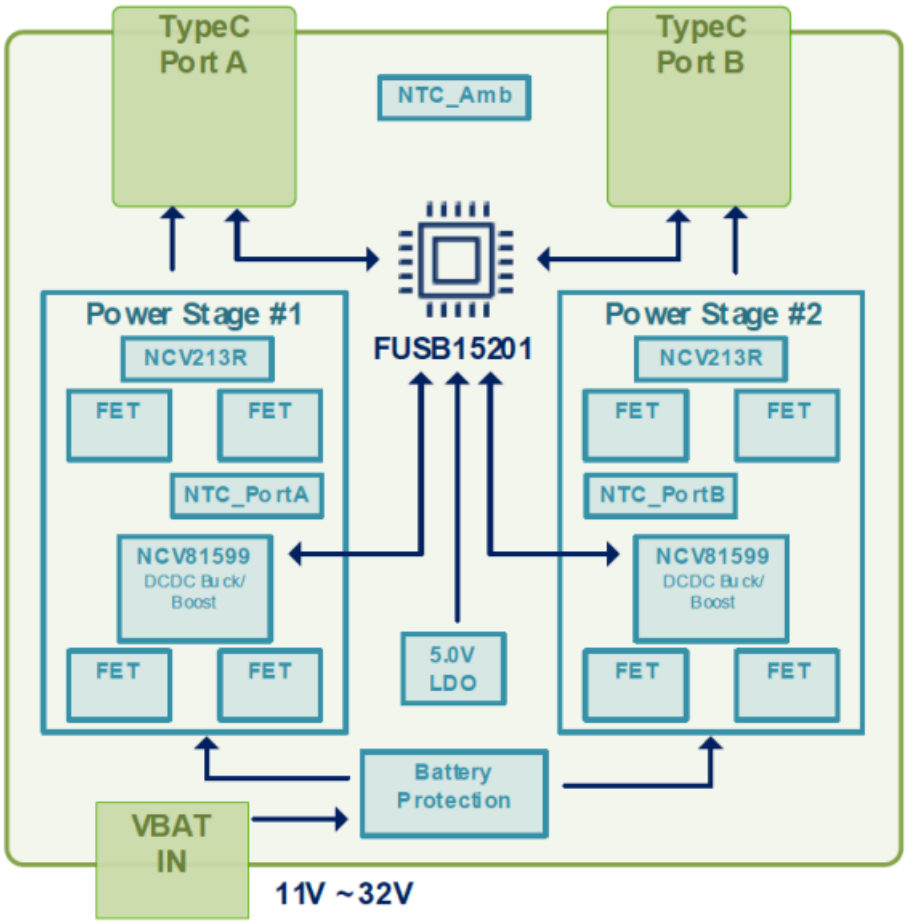


Figure 2. Concept

This Evaluation board is designed to provide a ready−to−use solution for a dual−port Type−C/PD Charging port application. All components are appropriately selected from automotive-qualified devices and capable of operating up to 125°C.

DETAILED DESCRIPTION OF EACH BLOCK

Power Stage

All power components are selected to drive output power up to 100 W per port (20 V / 5 A) if thermal performance is under control. Due to the limited PCB size and the space between each heat-dissipating component, the initial firmware will provide support for up to 60 W per port (120 W = 2 x 60 W) under control of the hottest board spot to lower than 100°C. In case higher output power is desired, it is recommended to perform re−sizing of the PCB design with thicker copper planes (>2 oz) for the top and bottom layers and to maintain enough space between heat-dissipating components (FET switches). This board is designed to fit into an application that has limited space, reflecting customer demand for charging ports in automotive cabin areas.

DC−DC Converter

NCV81599 is used as DC to DC converter controller with NVTFS5C460NL and NVTFS5C471NL for FET switches for Buck and Boost mode respectively. Power Inductor
(3.3 H, ETQP6M3R3YLC) is selected for driving output current up to 5.0 A.
In the Unattached state, FUSB15201 controls
EN_1/EN_2 to logic Low which maintains the NCV81599 power−off state for minimizing power consumption. In this state, NCV81599 has no I2C register accessibility. All
register values in NCV81599 will reset upon EN_x returning to logic High.
Each NCV81599 ADDR pin is set to a different I2C slave address.

Temperature Sensing

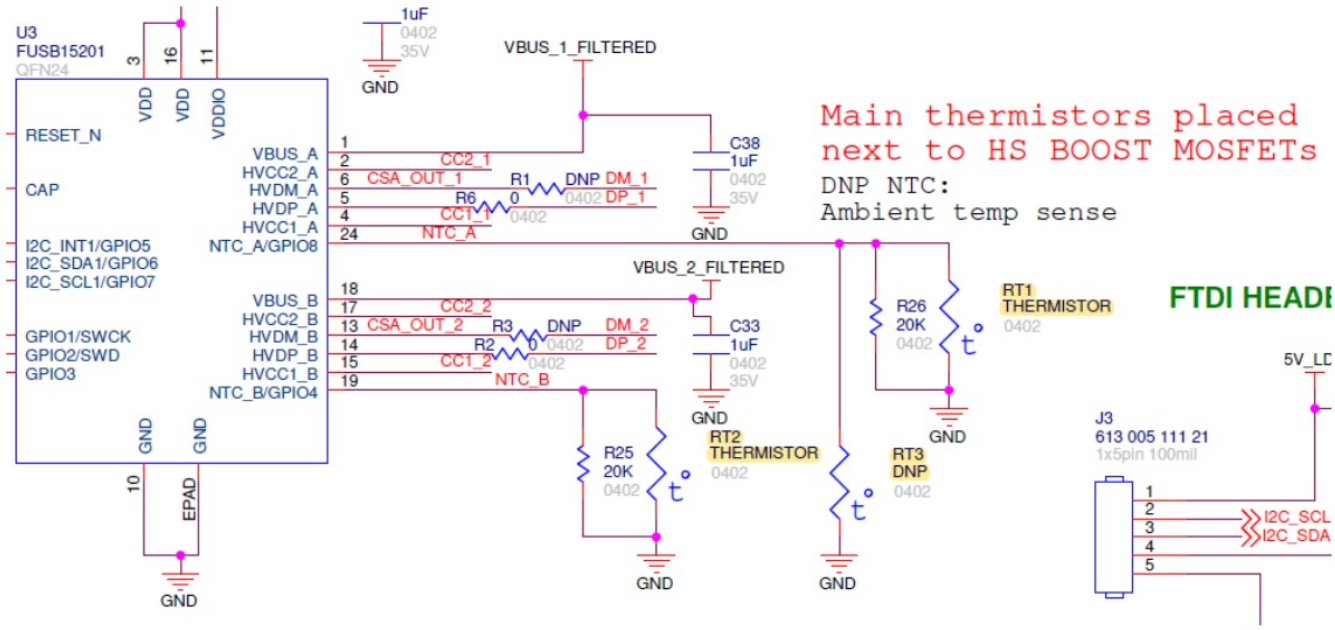


Figure 3.

Figure 3.
NTCs (RT1/ RT2) are initially populated nearby the area where the hi−side boost mode FETs (Q1 and Q3) are located.
Temperature read data from these spots indicate the hottest temperatures on the entire board area. If the ambient temperature is a higher concern than the FET switch, depopulate RT1 and RT2 and populate RT3 (not populated by default). RT3 is placed at the center between the two Type−C ports, and the temperature reading value will indicate the ambient board temperature between these two Type−C ports.

Output VBUS Current Sense

Current sense amplifiers (NCV213R) with 3 sense resistors are in the circuit for filtered VBUS current measurement. The amplified voltage (x50) goes to CSA_OUT_1/2 for ADC reading. (3m x 5.0 A x 50 = 750 mV @ 5.0 A loading)

J−Link Interconnect

GPIO2/SWD is being shared between EN_2, which enables NCV81599, and SWD for J−Link debug or download. A 3−pad 0 option (R48) sets the connection to EN_2 by default, so FUSB15201 can enable or disable NCV81599. When it is desired to connect to the SWD interface using J−Link, move the 0 connection to SWD, then return the connection to EN_2 when the firmware download is complete.
The firmware enables the use of SWD for connection to a J−Link debugger if R48 is configured to SWD. Note that if a sink is attached to Port 2, the firmware will disable SWD. Input/Output Voltage Measurement VBAT_F, VBUS_1_F, and VBUS_2_F are routed at the point of source/load as sensing input/output voltage. These can be used for accurate voltage measurement with minimum impact of voltage change by trace impedance, which can be used for efficiency measurements.

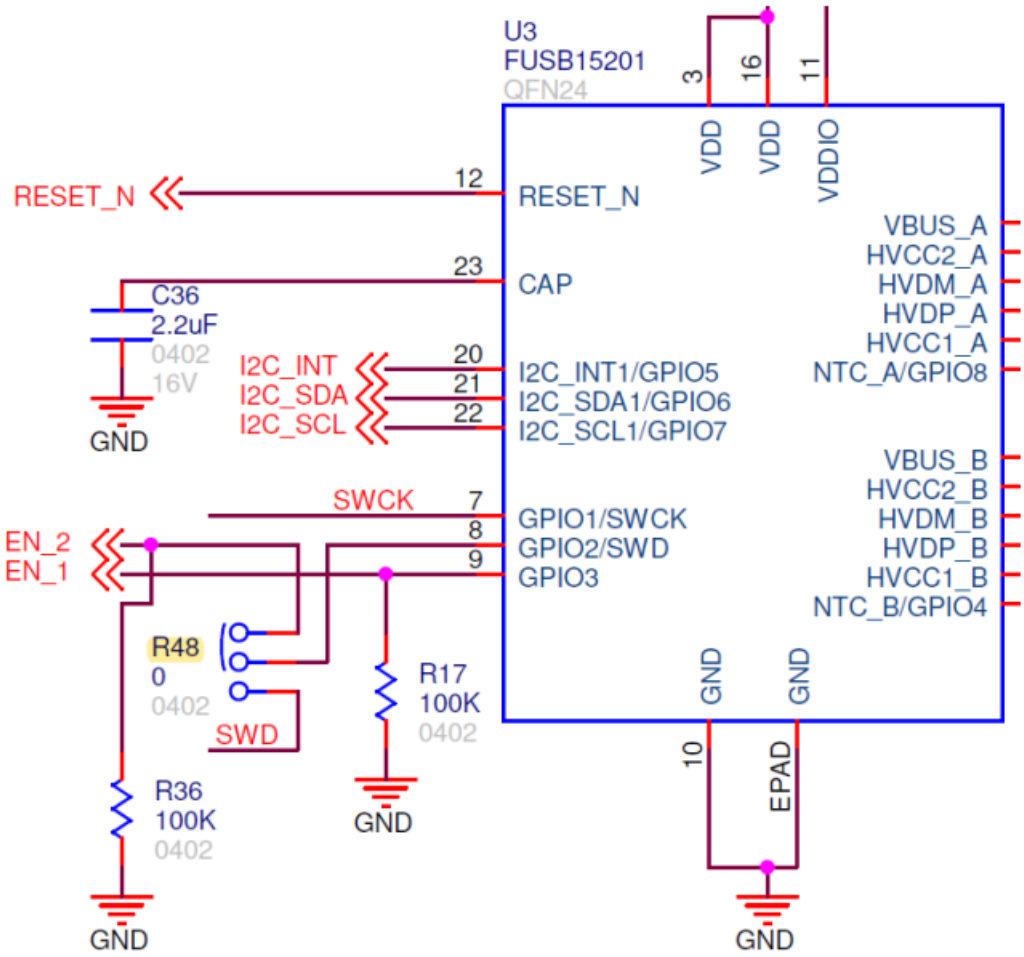


Figure 4.

Legacy BC1.2 Charging Port Support

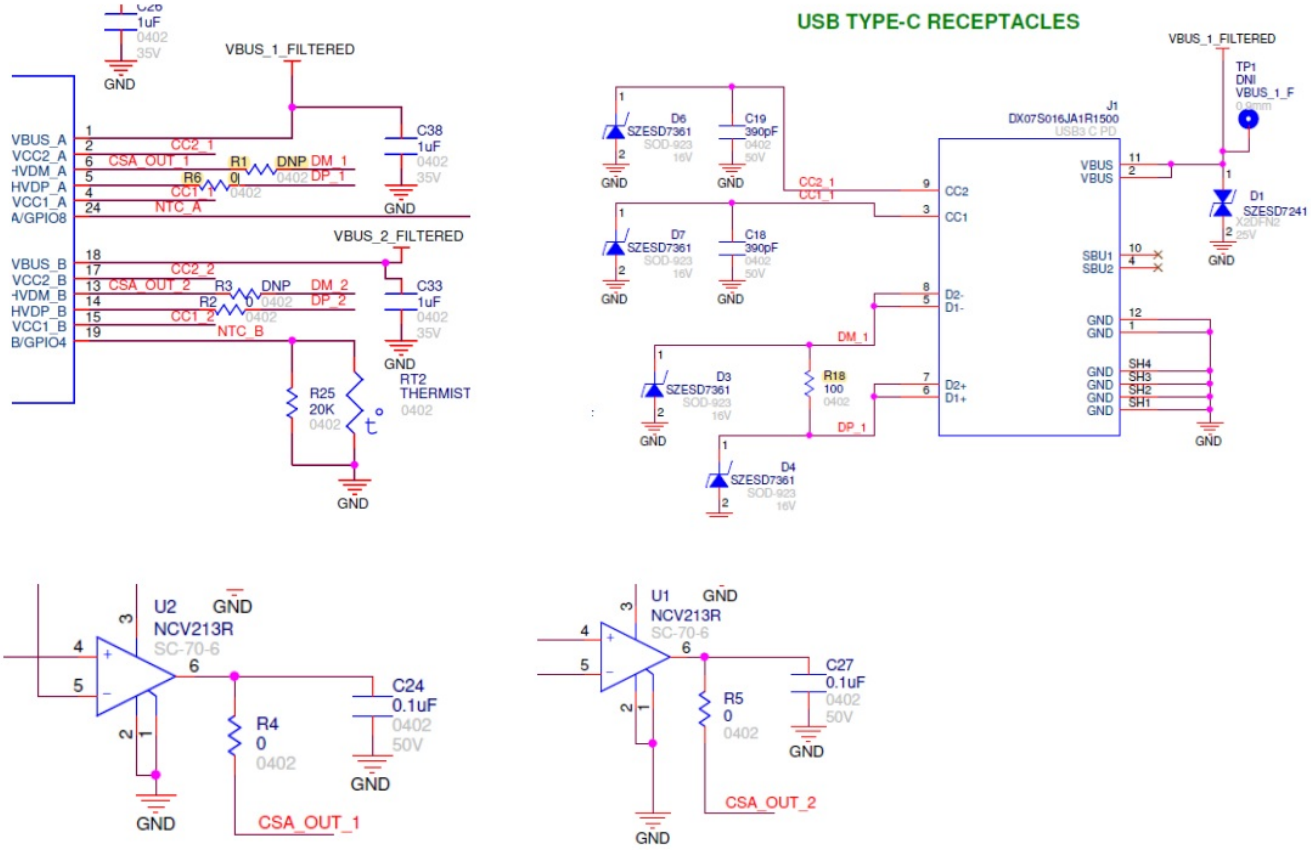


Figure 5.

FUSB15201 is capable of supporting a legacy charging port (Battery Charging 1.2 and voltage divider mode) through a built−in voltage/resistor divider. The built−in circuit uses HVDP/DM pins for mimicking a legacy charging port. This evaluation board uses the HVDP pin for moisture sensing and the HVDM pin for CSA (Current Sense Amplifier) monitoring by default. An external 0 resistor is placed between HVDP and HVDM for DCP (Dedicated Charging Port) configuration.

- Configuration for DCP with Moisture sensing on HVDP and CSA monitor on HVDM (Default):
  - ♦ R1 (PortA) & R3 (PortB): Not Populated
  - ♦ R18 (PortA) & R7 (PortB): 100Ω (~200Ω
  - ♦ R4 (PortA) & R5 (PortB): 0Ω
- Configuration for BC1.2 charging port (CDP/DCP) or voltage divider mode:
  - ♦ R1 (PortA) & R3 (PortB): 0Ω
  - ♦ R18 (PortA) & R7 (PortB): Not populated.
  - ♦ R4 (PortA) & R5 (PortB): Not populated.

CC/ VBUS Plot upon Accessory Plug−in

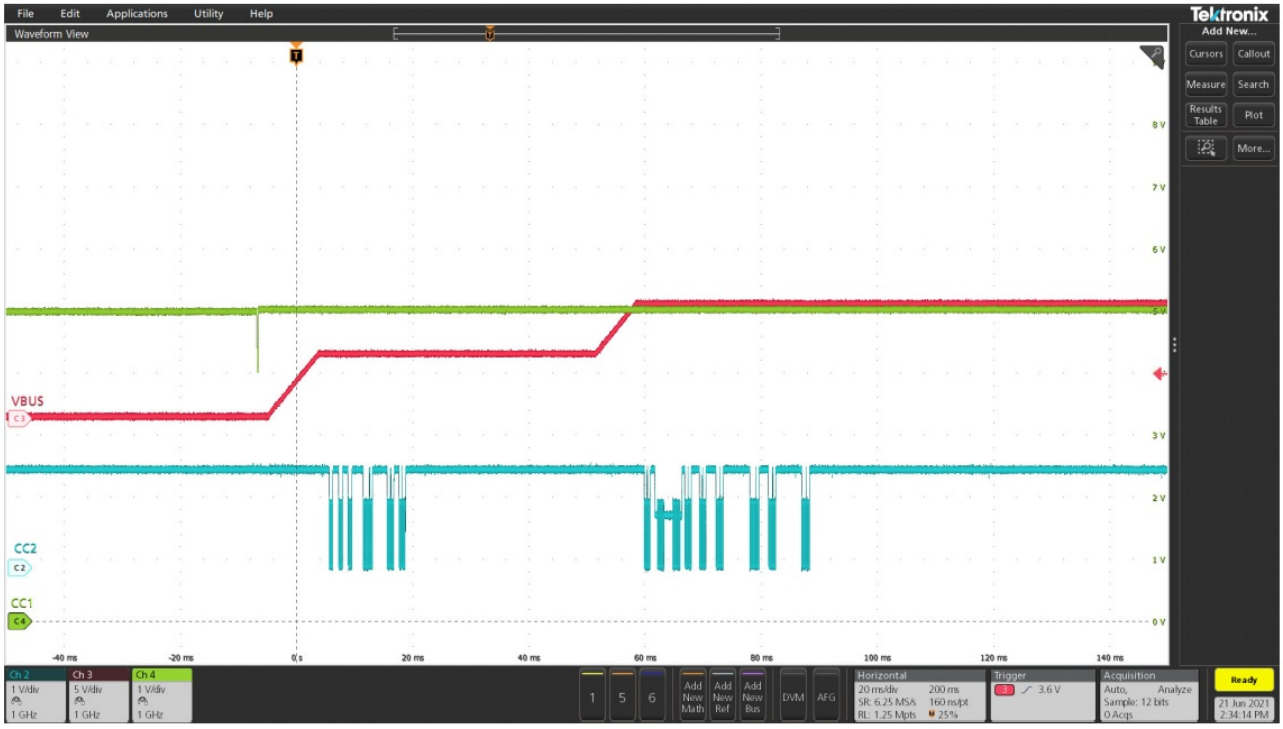


Figure 6. Sink Request 9 V PDO, CC = CC2, VCONN = CC1

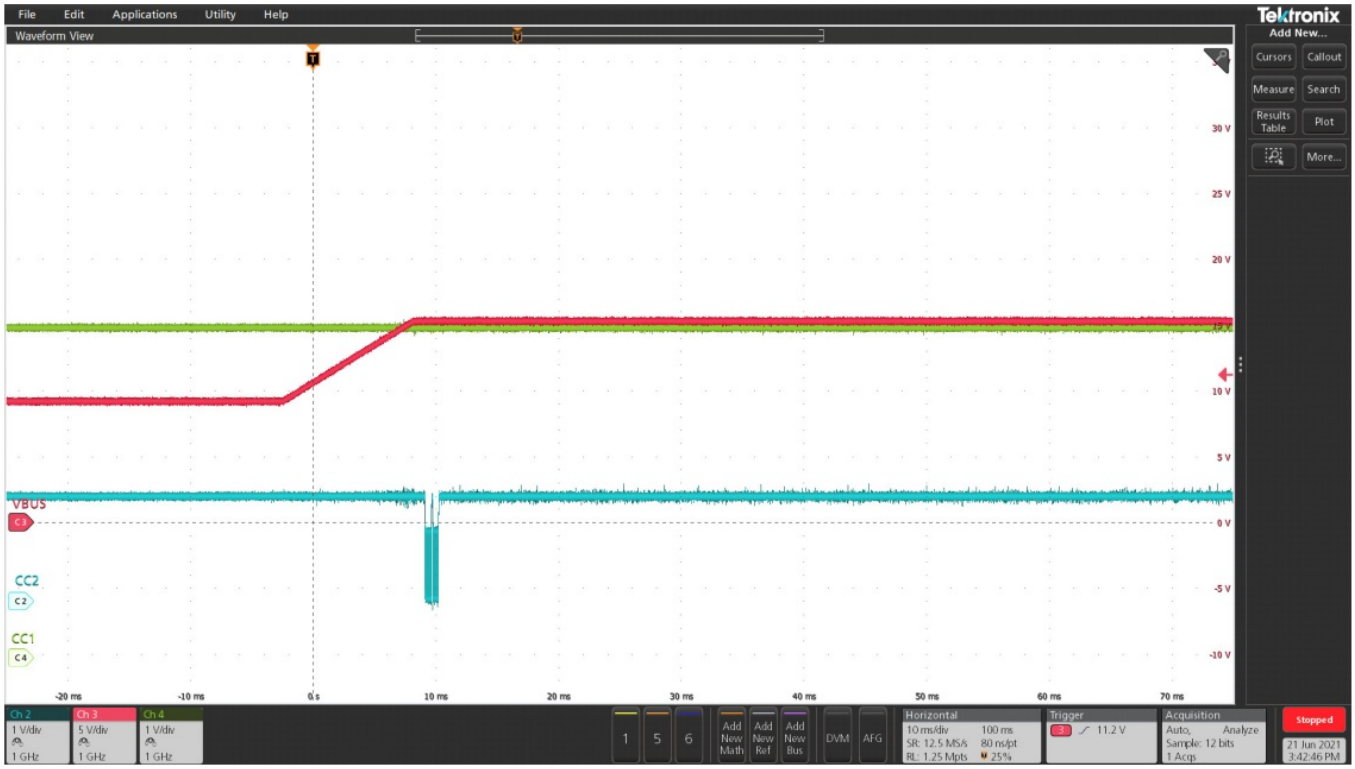


Figure 7. Sink Request 15 V PDO, CC = CC2, VCONN = CC1

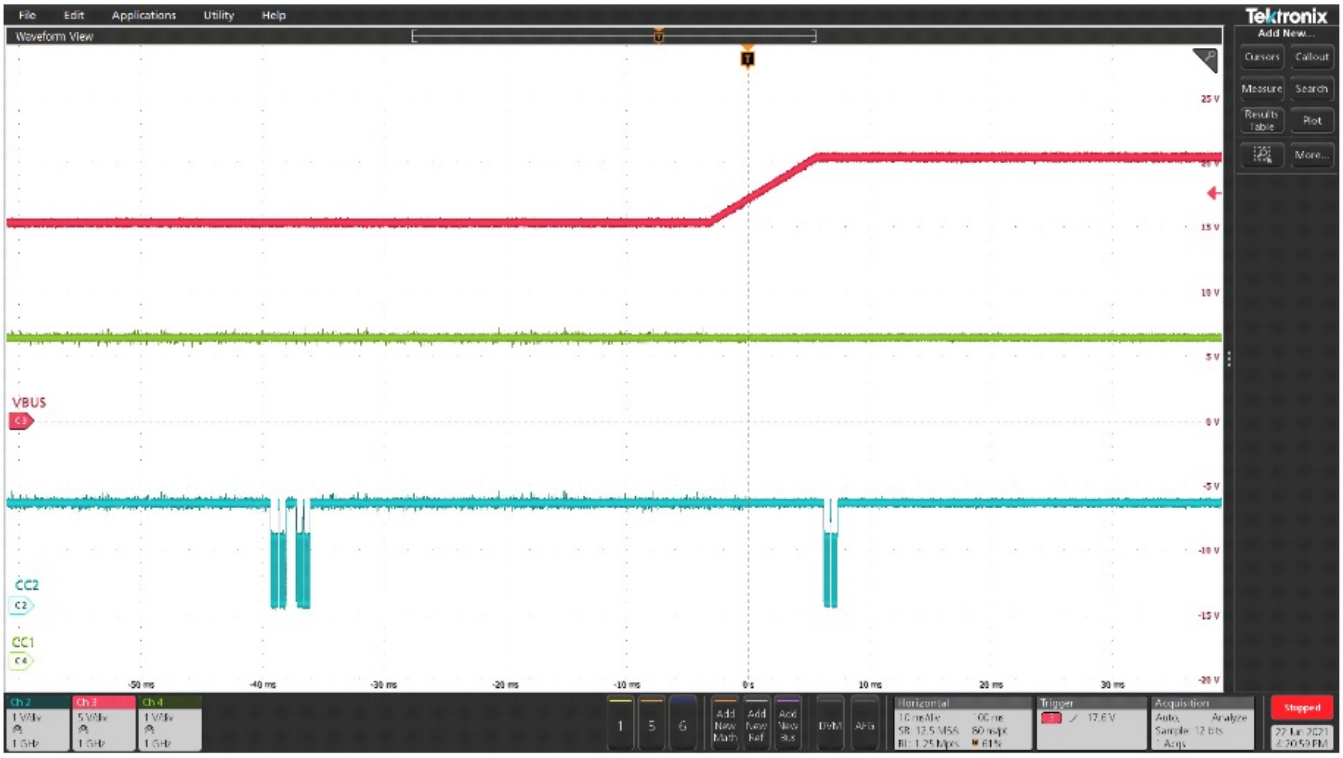


Figure 8. Sink Request 20 V PDO, CC = CC2, VCONN = CC1

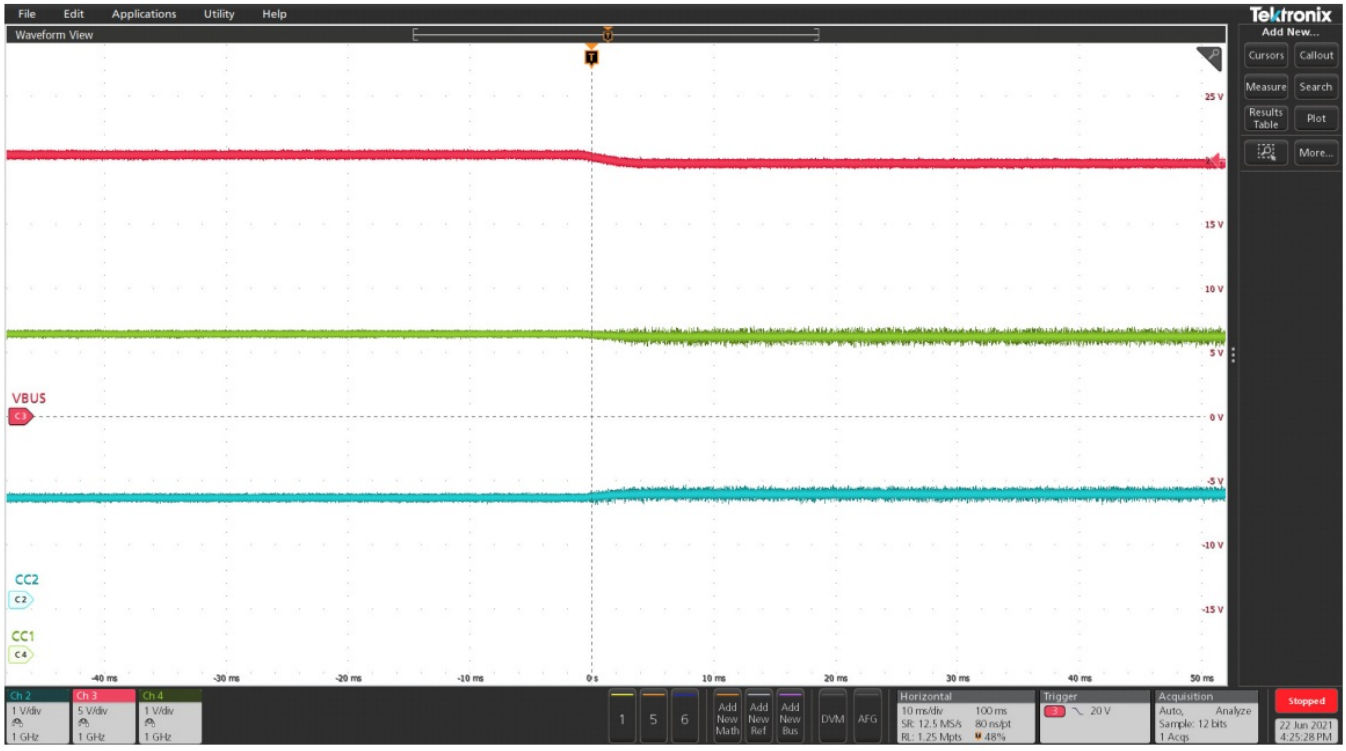


Figure 9. Loading 0 A to 3.0 A @ VBUS = 20 V

Thermal Performance 120 W (60 W + 60 W)

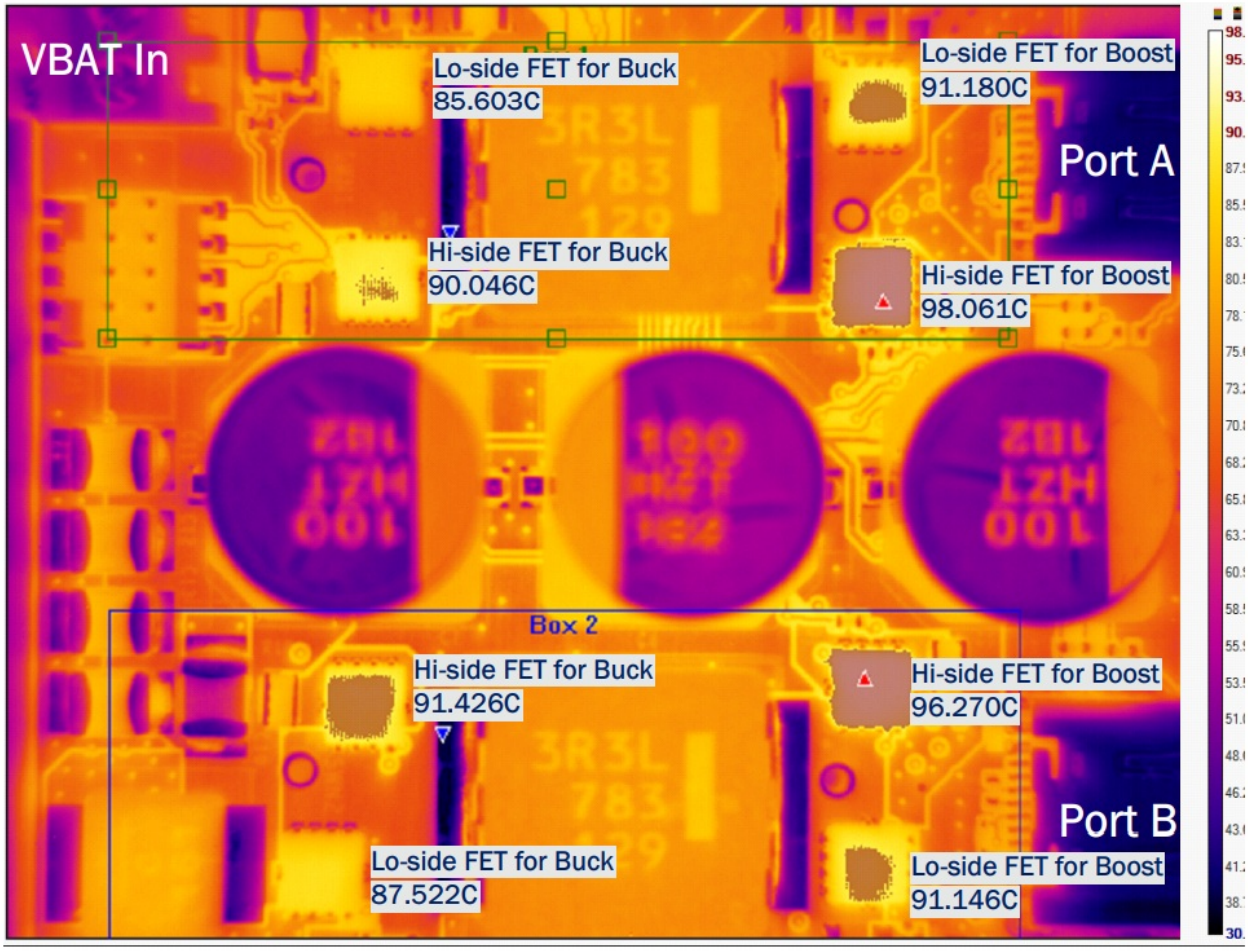


Figure 10.

Conditions

- Thermal Camera: FLIR SC7000
- Room temperature: 22°C
- VBAT power supply: 14 V / 15 A(limited) from BK9202
  ♦ Voltage drop across cable is compensated at the point of VBAT_IN
- VBUS contract: 20 V / 3.0 A
- Sink loader
  ♦ Sink Accessories: 2 x FUSB307B Evaluation Board
  ♦ Electronic loader: 2 x PLZ164WA (Constant Current mode)
  ♦ power out is measured at VBUS1_F and VBUS2_F on FUSB15201 EVB after 5 mins
- Aging time: > 1 hour after full loading

Result

- Highest temperature: 98.061°C (high side FET switch for boost mode)
- Efficiency measurement: 94.55%
  (Pout/Pin = 117.58 W / 124.36 W)
  ♦ PVBATin: 124.36 W = 12.969 V x 9.5888 A
  ♦ PVBUS_A: 58.47 W = 19.46 V x 3.005 A
  ♦ PVBUS_B: 59.11 W = 19.68 V x 3.004 A

♦ PVBUStotal: 117.58 W = 58.47 W + 59.11 W

onsemi DEVICE LINKS

Device	Description
SZESD7241	ESD Protection Diode Ultra Low Capacitance
SZESD7361	ESD Protection Diode
SZMM3Z18VT1G	Generic SOD−323 Zener Diode
NVTFS5C471NL	Generic u8FL DFN−5 N−Channel Power MOSFET
NVTFS5C460NL	Generic u8FL DFN−5 N−Channel Power MOSFET
NVMFS5A140PLZ	Generic SO8−FL DFN−5 P−Channel Power MOSFET
NCV213R	Current−Shunt Monitor, Voltage Output, Bi−Directional Zero−Drift, Gain = 5(
FUSB15201	Dual Port USB Type−C & PD Controller
NCV81599	4 Switch Buck−Boost
NCV8730BMTW500	LDO Regulator, 150 mA, 38 V max input, 1 A IQ, with PG Automotive

Other References
FUSB15201 Flash Programming Guide UM70056/D.

FUSB15201 + NCV81599
USB−PD DUAL PORT
(AUTOMOTIVE)

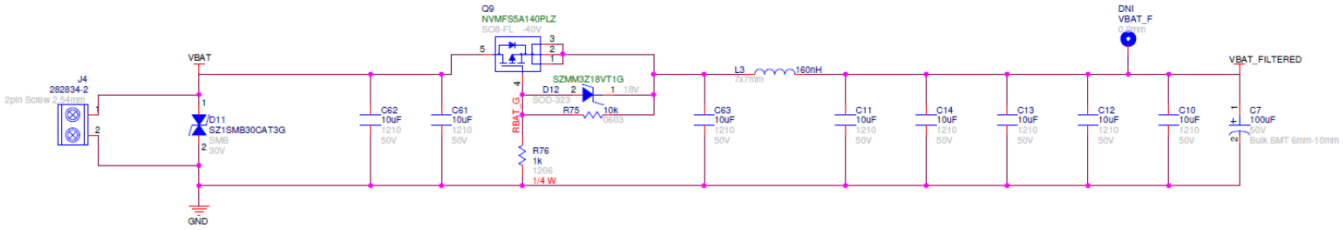
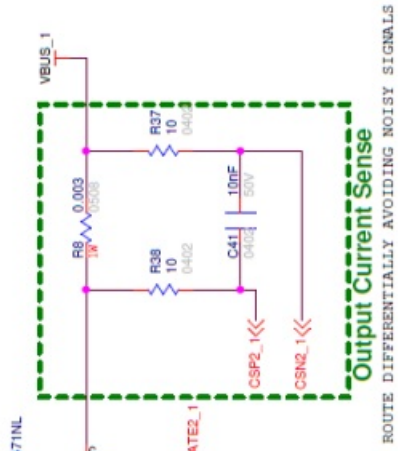


Figure 11. Input Filters and Battery Protection



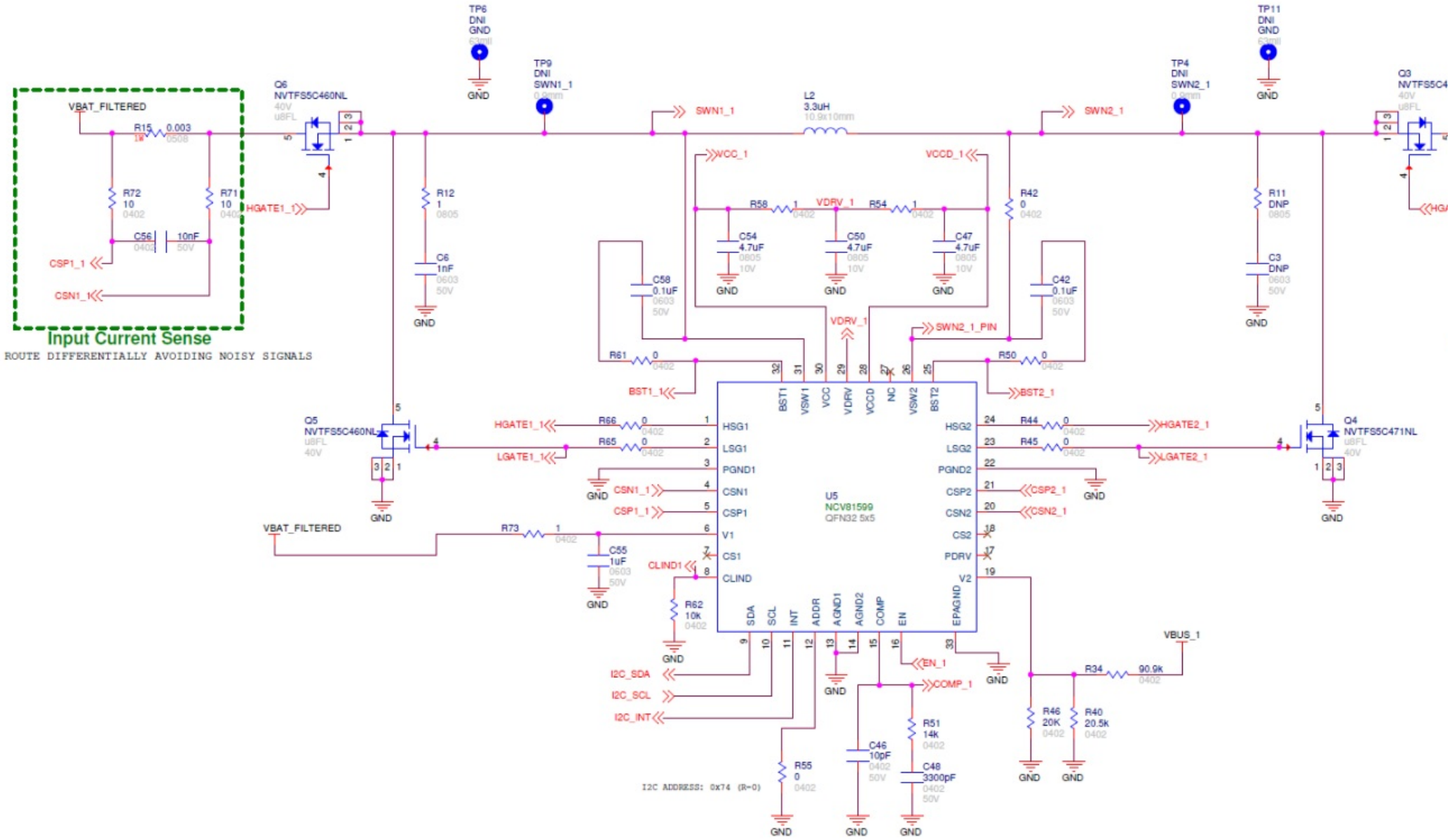
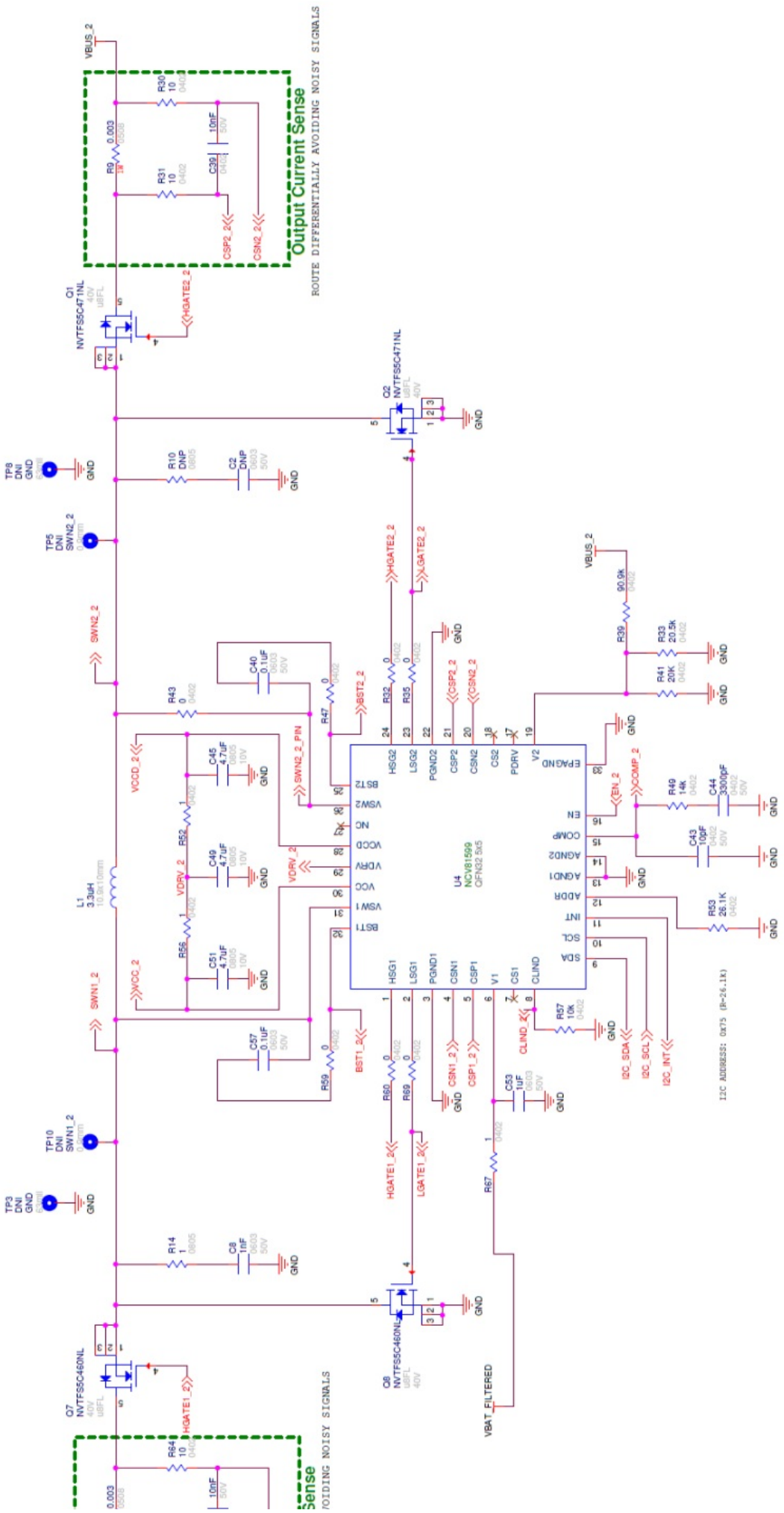

Input Current Sense
ROUTE DIFFERENTIALLY AVOIDING NOISY SIGNALS
VBAT_FILTERED
R15 0.003 1W 0508
R72 10 0402
R71 10 0402
C56 0402
10nF 50V
CSP1_1
CSN1_1
Q6 NVTFS5C460NL 40V u8FL
HGATE1_1
TP6 DNI GND 60mil
TP9 DNI SWN1_1 0.8mm
SWN1_1
L2 3.3uH 10.9x10mm
SWN2_1
TP4 DNI SWN2_1 0.8mm
TP11 DNI GND 60mil
Q3 NVTFS5C4 40V u8FL
R12 1 0805
C6 1nF 0603 50V
VCC_1
VCCD_1
R58 1 0402
VDRV_1
R54 1 0402
C54 4.7uF 0805 10V
C50 4.7uF 0805 10V
C47 4.7uF 0805 10V
R42 0 0402
R11 DNP 0805
C3 DNP 0603 50V
C58 0.1uF 0603 50V
C42 0.1uF 0603 50V
SWN2_1_PIN
R61 0 0402
R50 0 0402
BST1_1
BST2_1
Q5 NVTFS5C460NL u8FL 40V
Q4 NVTFS5C471NL u8FL 40V
HGATE1_1
R66 0 0402
R65 0 0402
LGATE1_1
R44 0 0402
R45 0 0402
HGATE2_1
LGATE2_1
U5
NCV81599
QFN32 5x5
BST1
VSW1
VCC
VDRV
VCCD
NC
VSW2
BST2
HSG1
LSG1
PGND1
CSN1
CSP1
V1
CS1
CLIND
HSG2
LSG2
PGND2
CSP2
CSN2
CS2
PDRV
V2
EPAGND
SDA
SCL
INT
ADDR
AGND1
AGND2
COMP
EN
CSP2_1
CSN2_1
VBAT_FILTERED
R73 1 0402
C55 1uF 0603 50V
CLIND1
R62 10k 0402
I2C_SDA
I2C_SCL
I2C_INT
EN_1
COMP_1
VBUS_1
R34 90.9k 0402
R46 20K 0402
R40 20.5k 0402
R51 14k 0402
C46 10pF 0402 50V
C48 3300pF 0402 50V
R55 0 0402
I2C ADDRESS: 0x74 (R=0)
GND

Figure 12. NCV81599 − Power Stage 1



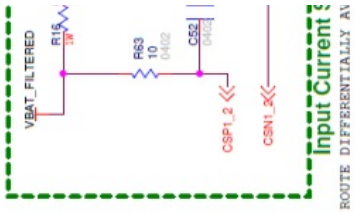


Figure 13. NCV81599 − Power Stage 2

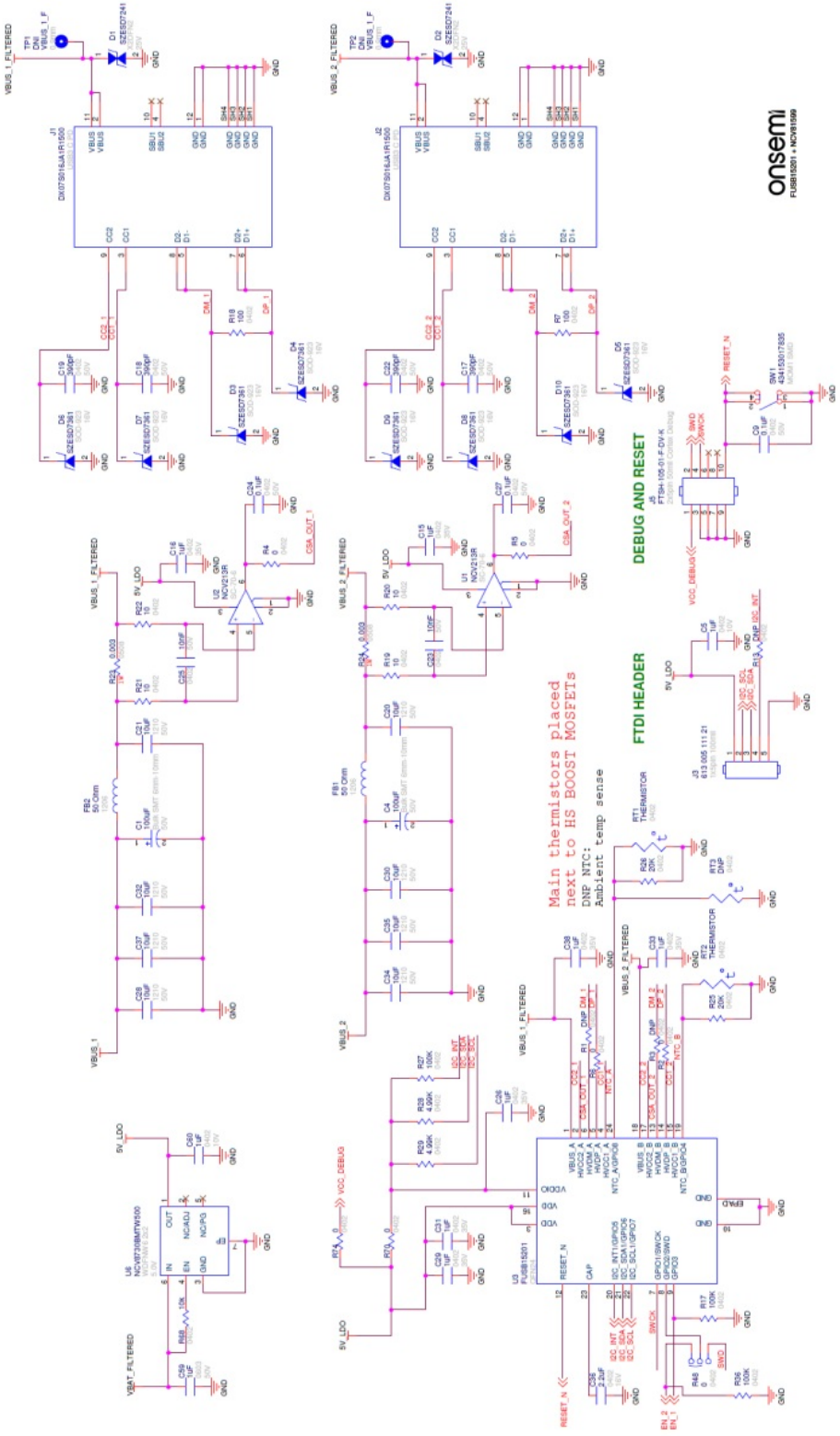


Figure 14. FUSB15201 & Connectors

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References

- Intelligent Power and Sensing Technologies | onsemi