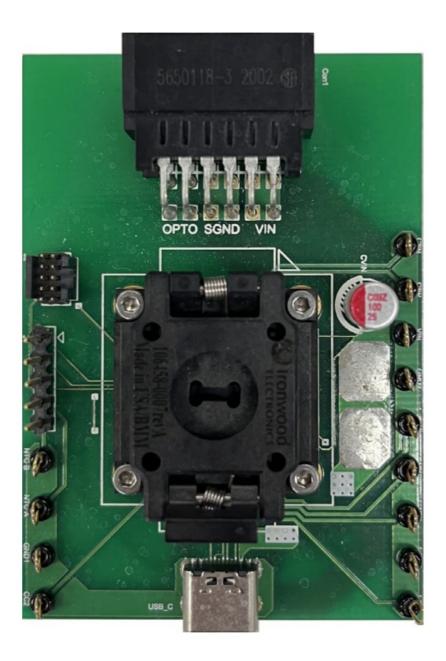


# ON Semiconductor FUSB15101 Single Port USB Type-C-PD Controller User Manual

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ON Semiconductor FUSB15101 Single Port USB Type-C-PD Controller User Manual



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## Introduction

The FUSB15101 Evaluation Board (EVB) together with the firmware binary provided in the release package permits a customer to program the one–time programmable (OTP) non–volatile memory (NVM) of the FUSB15101.

# **Required Hardware and Setup Instructions**

- A. FUSB15101 Evaluation Board (EVB)
- B. 32 kB OTP Chip labeled FUSB15101 MIN
- C. SEGGER J-Link Pro JTAG/SWD programming and debug probe

- D. 9-Pin Cortex-M Adapter to connect (A) the EVB to (C) J-Link Pro
- E. External Power Supply
- Use (D) the 9-Pin Adapter to connect (C) the J-Link Pro to the SWD connector (J2) on the socket EVB
- · Place the OTP chip in socket
- Connect (E) the Power Supply GND to the SGND pin of (A) the EVB
- Setup (E) the Power Supply to 8.4 V (~200 mA) and connect to VIN pin (Con1) of (A) the EVB

## **Required Software**

#### A. SEGGER J-Link Tools

Please download and install the SEGGER J-Link utility **Note:** Please make sure SEGGER J-Flash is installed.

#### B. Serial Wire Debug (SWD) Converter Tool

Please download and install the FUSB15101 SWD Converter tool **Note:** Search for keyword FUSB15101 SWD Converter Tool.

#### C. FUSB15101 Flash Loader

Please download the FUSB15101 Flash Loader used by J-Link to flash the EVB. Search for file FUSB15101 FLASH LOADER.ELF

Further instructions on where to place this file will be indicated in the subsequent paragraph.

#### D. FUSB15101 NVR Loader

Please download the FUSB15101 NVR Loader used by J–Link to load data onto the EVB. Search for file FUSB15101\_NVR\_LOADER.ELF Further instructions on where to place this file will be indicated in the subsequent paragraph.

#### E. FUSB15101 Device List AddOn

Please download the FUSB15101 Device AddOn to add the FUSB15101 to the device list xml. Search for file FUSB15101 XML ADDON.TXT

## Adding FUSB15101 Support to J-Link

There is a need to add the FUSB15101 to the list of J-Link supported devices. J-Link provides a device list in xml format to which the FUSB15101 shall be added as follow:

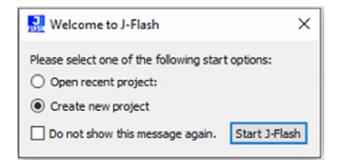
- Create a directory named FUSB15101 under:
  - C:\Program Files (x86)\SEGGER\JLink\Devices\ONSemiconductor\
- Copy the 2 files (C) and (D) from section "Required Software" into
  - C:\Program Files (x86)\SEGGER\JLink\Devices\ONSemiconductor\FUSB15101
- Open the file C:\Program Files (x86)\SEGGER\JLink\JLinkDevices.xml in a text editor.

Add the content of (E) FUSB15101\_XML\_ADDON.TXT to the end of the JLinkDevices.xml file.

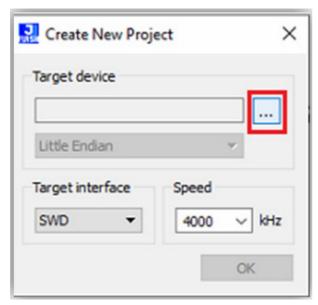
#### **Programming the OTP**

Complete the following 5 steps:

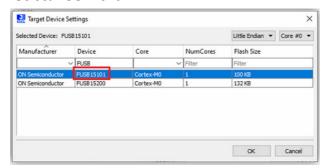
- a. Connect J-Link to the EVB
- **b.** Validate OTP chip is blank
- c. Convert the FW Image with the SWD Converter tool
- d. Flash the converted FW image into OTP
- e. Validate OTP Content
- a. Connect J-Link to the EVB
- Open the SEGGER J-Flash and select "Create new project" then "Start J-Flash"



· Click on the selection box



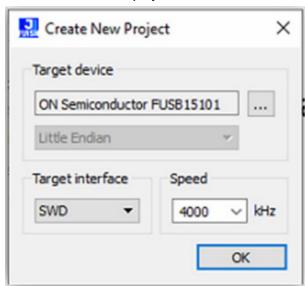
• Select FUSB15101



• Select Target interface: SWD

• Select Speed: 4000 KHz

· Click OK for the new project to be created



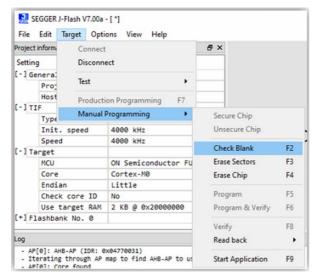
- From the menu go to Target
- Then go to Connect If the connection is established, you should see a message on the Log indicating a successful connection.

```
Log

- AP[0]: AHB-AP (IDR: 0x04770031)
- Iterating through AP map to find AHB-AP to use
- AP[0]: Core found
- AP[0]: Core found
- AP[0]: AHB-AP ROM base: 0xE00FF000
- CPUID register: 0x410CC601. Implementer code: 0x41 (ARM)
- Found Cortex-M0 r0p1, Little endian.
- FPUnit: 4 code (BP) slots and 0 literal slots
- Coresight components:
- ROMTDL[0] @ E00FF000
- ROMTDL[0][0]: E000E000, CID: B105E000, PID: 000BB008 SCS
- ROMTDL[0][1]: E0001000, CID: B105E000, PID: 000BB00B DWT
- ROMTDL[0][2]: E0002000, CID: B105E000, PID: 000BB00B FPB
- Executing init sequence...
- Initialized successfully
- Target interface speed: 4000 kHz (Fixed)
- Found 1 JTAG device. Core ID: 0x0BC11477 (None)
- Connected successfully
```

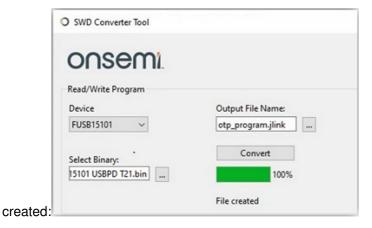
#### b. Validate OTP Chip is Blank

- · Go to Target
- · Go to Manual Programming
- Select Check Blank. J–Flash should confirm the OTP is blank



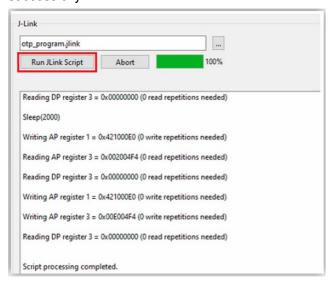
## c. Convert the FW Image with the SWD Converter Tool

- Open the SWD Converter Tool
- Select FUSB15101 from the Device list
- Select the FW Binary to convert in the Select Binary field
- Click on Convert When the image conversion is completed, you should see the following indicating File



d. Flash the Converted FW Image into OTP

Once the FW Image converted successfully, you can program the OTP by clicking on Run JLink Script.
 A Message on the Log section shall confirm that the script processing is completed and the OTP programmed successfully



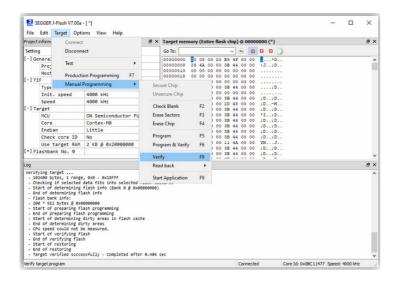
e. Validate the OTP Content

At the end of the process, users shall take the extra step to validate that programming the OTP went as expected.

- · Go to Target
- Go to Manual Programming
- · Select Verify

A message in the Log section shall state Target verified successfully.

The FW can start either by power cycling the EVB or by selecting Start Application (F9) shown also in the below screenshot.



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#### **Documents / Resources**



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#### References

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- SEGGER The Embedded Experts Downloads
- SEGGER J-Link PRO

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