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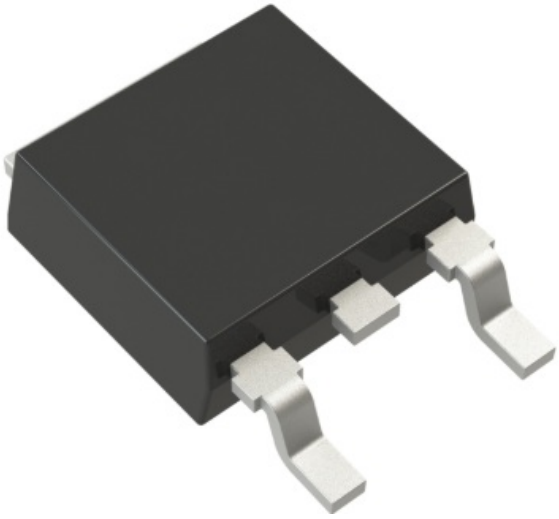
ON Semiconductor FDD9409L-F085 Channel Logic Level Power Trench



Specifications

- **Model:** FDD9409L-F085
- **Voltage:** 40V
- **Current:** 90A
- **Size:** 2.6 m
- **Features:**
  - IG Typical RDS(on) = 2.1 m at VGS = 10V, ID = 80 A
  - ES Typical Qg(tot) = 52 nC at VGS = 10V, ID = 80 A
  - UIS Capability
  - RoHS Compliant
  - Qualified to AEC Q101
- **Applications:**
  - Automotive Engine Control
  - PowerTrain Management
  - Solenoid and Motor Drivers
  - Electronic Steering
  - Integrated Starter/Alternator
  - Distributed Power Architectures and VRM
  - Primary Switch for 12V Systems

Safety Precautions

Before using the product, please read the safety precautions in the user manual to ensure safe operation.

Installation

1. Ensure the power is turned off before installation.
2. Connect the product according to the provided wiring diagram.
3. Securely mount the product in a suitable location.

Features

- Typical RDS(on) = 2.1 at VGS = 10V, ID = 80 A
- Typical Qg(tot) = 52 nC at VGS = 10V, ID = 80 A
- UIS Capability
- RoHS Compliant
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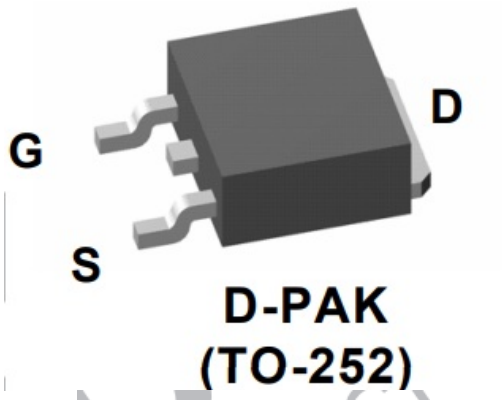
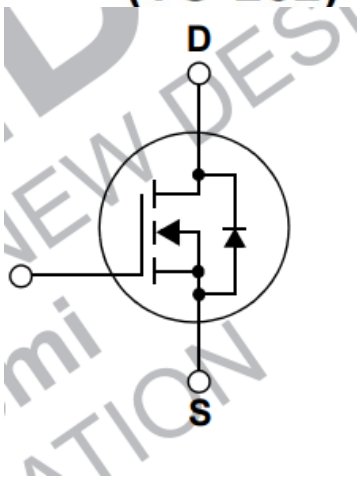




Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electronic Steering

- Integrated Starter/Alternator
- Distributed Power Architectures and VRN
- Primary Switch for 12V Systems

MOSFET Maximum Ratings

T, = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
VDSS	Drain-to-Source Voltage			40	V
VGS	Gate-to-Source Voltage			±20	V
ID	Drain Current – Continuous (VGS=10) (Note 1)	TC = 25°C		90	A
	Pulsed Drain Current	TC = 25°C		See Figure 4	
EAS	Single Pulse Avalanche Energy		(Note 2)	33.7	mJ
PD	Power Dissipation			150	W
	Derate Above 25°C			1	W/°C
TJ, TSTG	Operating and Storage Temperature			-55 to + 175	oC

RqJC	Thermal Resistance, Junction to Case			1	°C/W
RqJA	Maximum Thermal Resistance, Junction to Ambient		(Note 3)	52	°C/W

Notes:

1. Current is limited by the bondwire configuration.
2. Starting TJ = 25°C, L = 15uH, IAS = 67A, VDD = 40V during inductor charging ,and VDD = 0V during time in avalanche.
3. ROJA is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. RJC is guaranteed by design, while ROJA is determined by the board design. The maximum rating presented here is based on mounting on a 1 in2 pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD9409L	FDD9409L-F085	D-PAK(TO-252)	13”	16mm	2500units

Electrical Characteristics TJ = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units

Off Characteristics

BVDSS	Drain-to-Source Breakdown Voltage	ID = 250mA, VGS = 0 V	40	–	–	V

IDSS	Drain-to-Source Leakage Current	VDS=40V, VGS = 0V	TJ = 25°C	–	–	1	mA
			TJ = 175°C (Note 4)	–	–	1	mA
IGSS	Gate-to-Source Leakage Current	VGS = ±20V		–	–	±100	nA

On Characteristics

VGS(th)	Gate to Source Threshold Voltage	VGS = VDS, ID = 250 mA		1.0	1.8	3.0	V
RDS(on)	Drain to Source On Resistance	ID = 80A, VGS= 4.5V		–	3.0	4.4	mW
		ID = 80 A, VGS = 10V	TJ = 25°C	–	2.1	2.6	mW
			TJ = 175 °C (Note 4)	–	3.7	4.6	mW

Dynamic Characteristics

Ciss	Input Capacitance	VDS = 20V, VGS = 0V , f = 1MHz		–	3360	–	pF
Coss	Output Capacitance			–	1080	–	pF
Crss	Reverse Transfer Capacitance			–	42	–	pF
Rg	Gate Resistance	f = 1MHz		–	2.2	–	W
Qg(ToT)	Total Gate Charge	VGS = 0 to 10V	VDD =	–	52	68	nC

Qg(th)	Threshold Gate Charge	VGS = 0 to 2V	32V ID = 80A	–	7	–	nC
Qgs	Gate-to-Source Gate Charge			–	11	–	nC
Qgd	Gate-to-Drain “Miller“ Charge			–	8	–	nC

Switching Characteristics

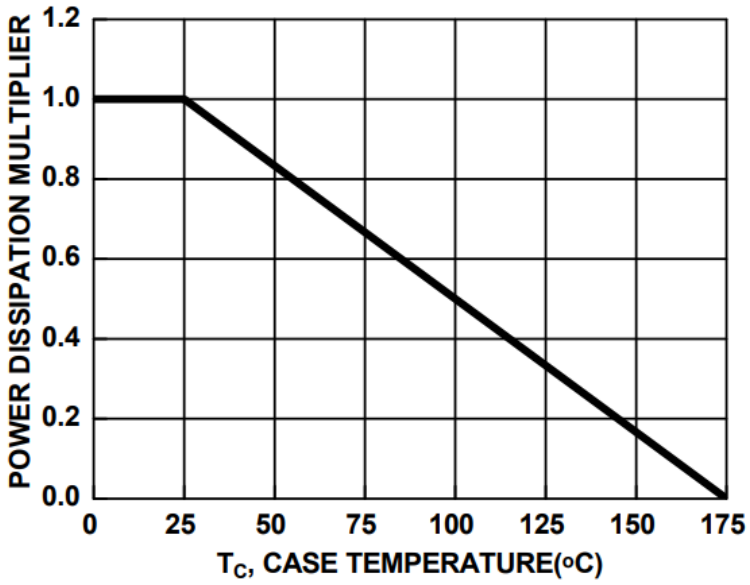
ton	Turn-On Time	VDD = 20V, ID = 80A, VGS = 10V, RGEN = 6W	–	–	47	ns
td(on)	Turn-On Delay		–	10	–	ns
tr	Rise Time		–	13	–	ns
td(off)	Turn-Off Delay		–	36	–	ns
tf	Fall Time		–	10	–	ns
toff	Turn-Off Time		–	–	70	ns

Drain-Source Diode Characteristics

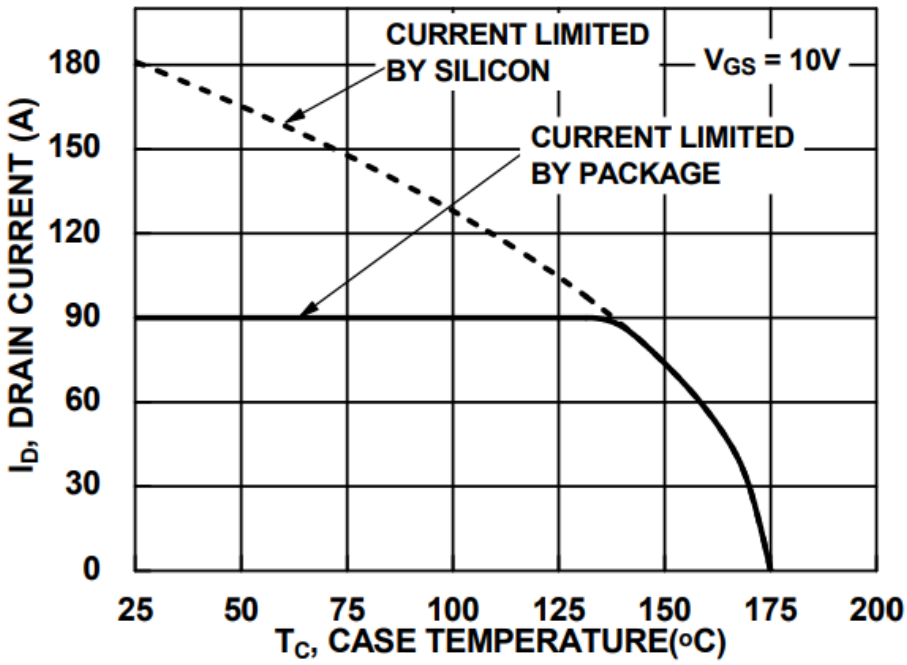
VSD	Source-to-Drain Diode Voltage	ISD =80A, VGS = 0V	–	–	1.25	V
		ISD = 40A, VGS = 0V	–	–	1.2	V
trr	Reverse-Recovery Time	IF = 80A, dISD/dt = 100A/ms VDD = 32V	–	59	77	ns
Qrr	Reverse-Recovery Charge		–	57	74	nC

Note: The maximum value is specified by design at TJ = 175°C.The product is not tested under these conditions in production.

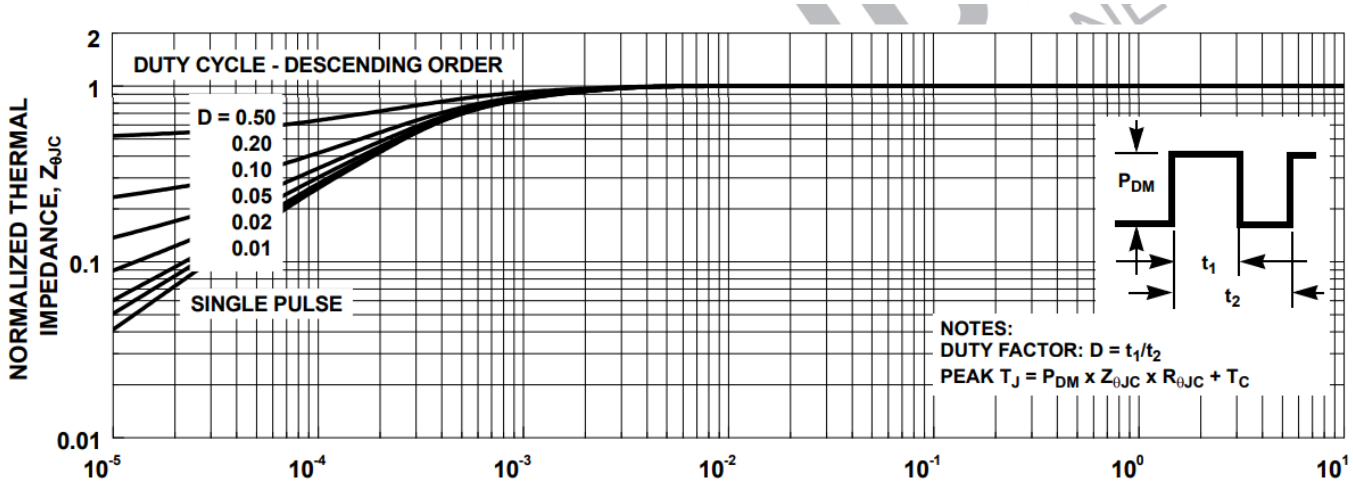
Typical Characteristics



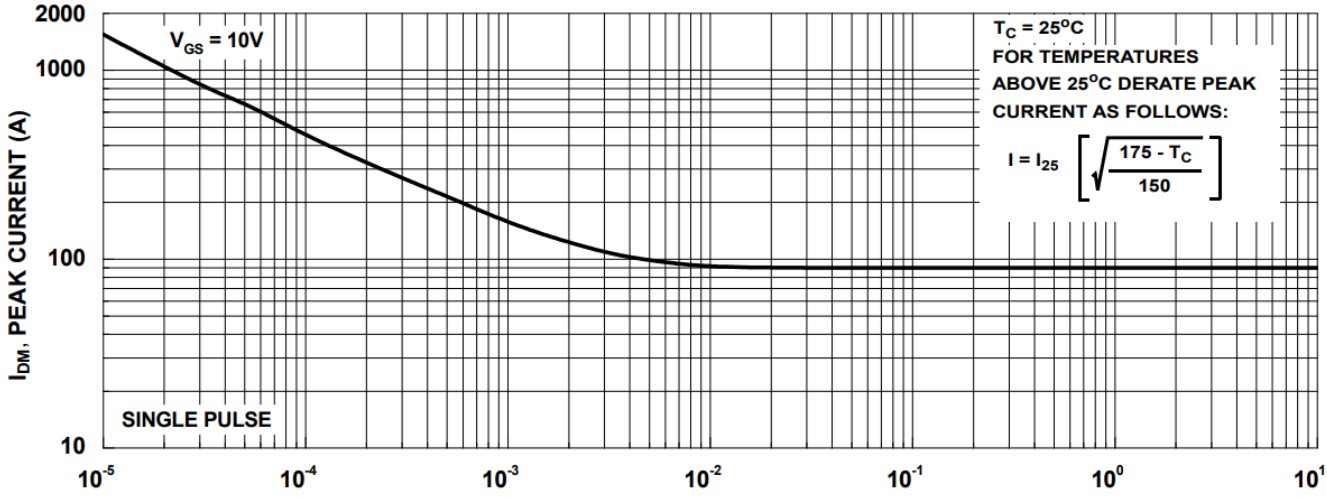
- Normalized Power Dissipation vs. Case Temperature



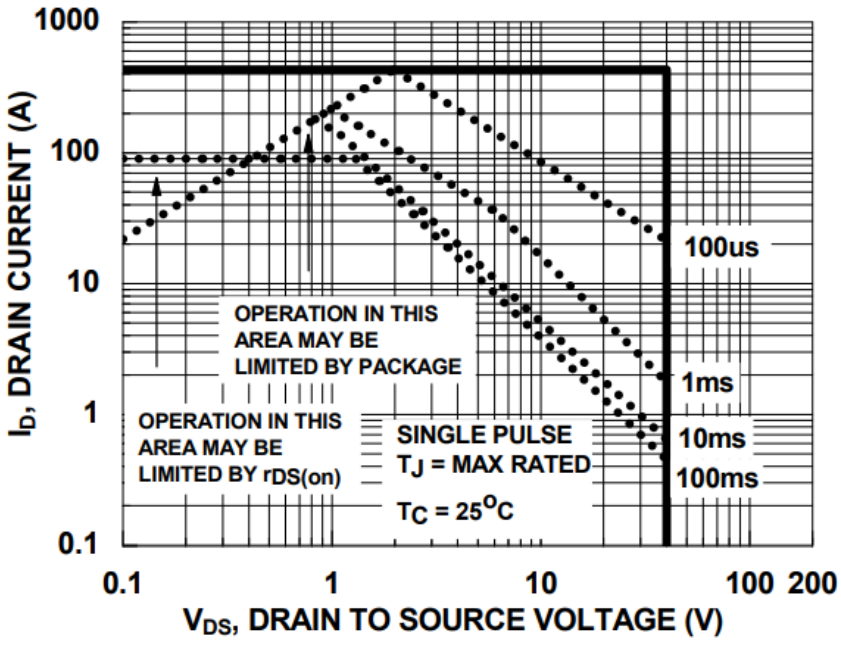
- Maximum Continuous Drain Current vs. Case Temperature



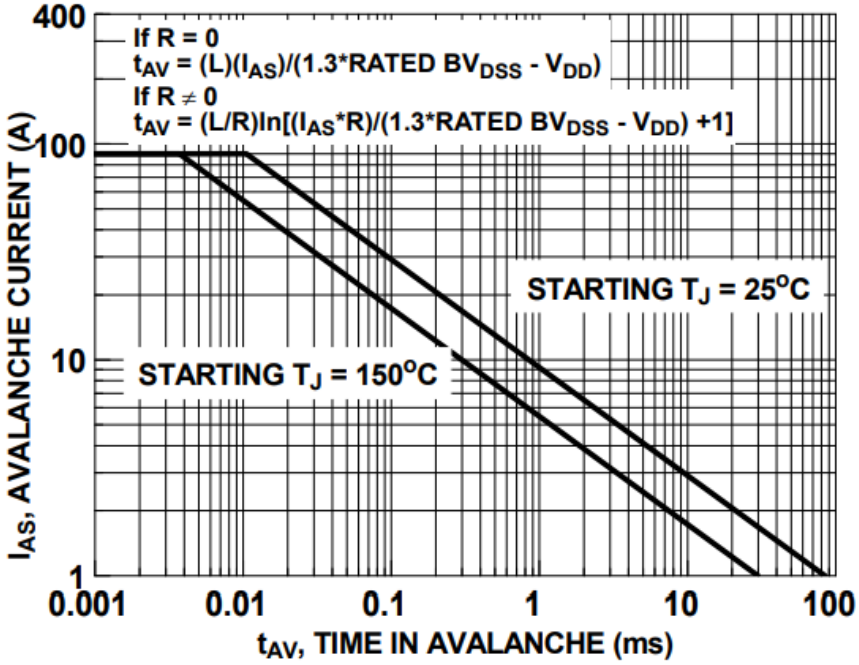
- Normalized Maximum Transient Thermal Impedance



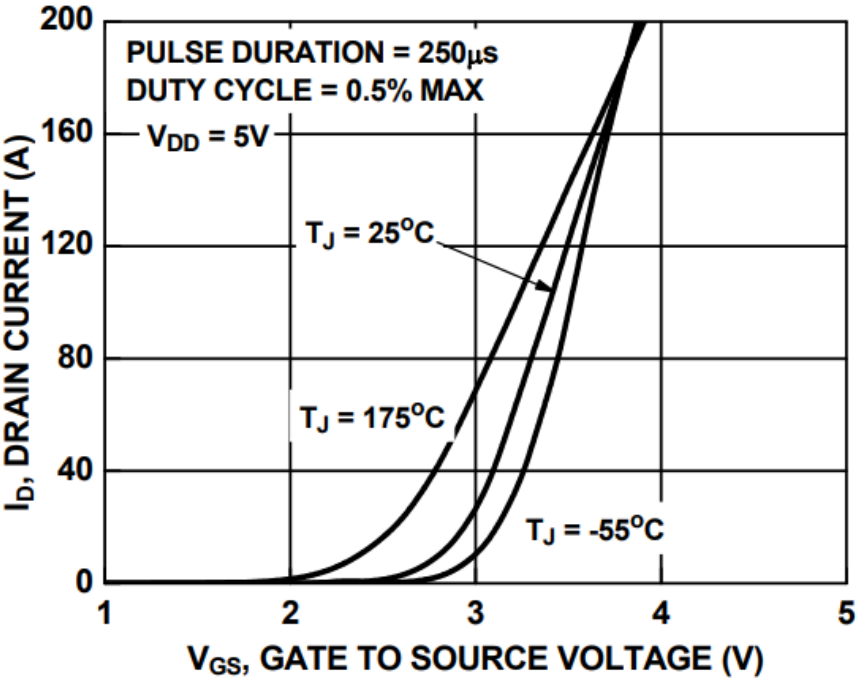
- Peak Current Capability



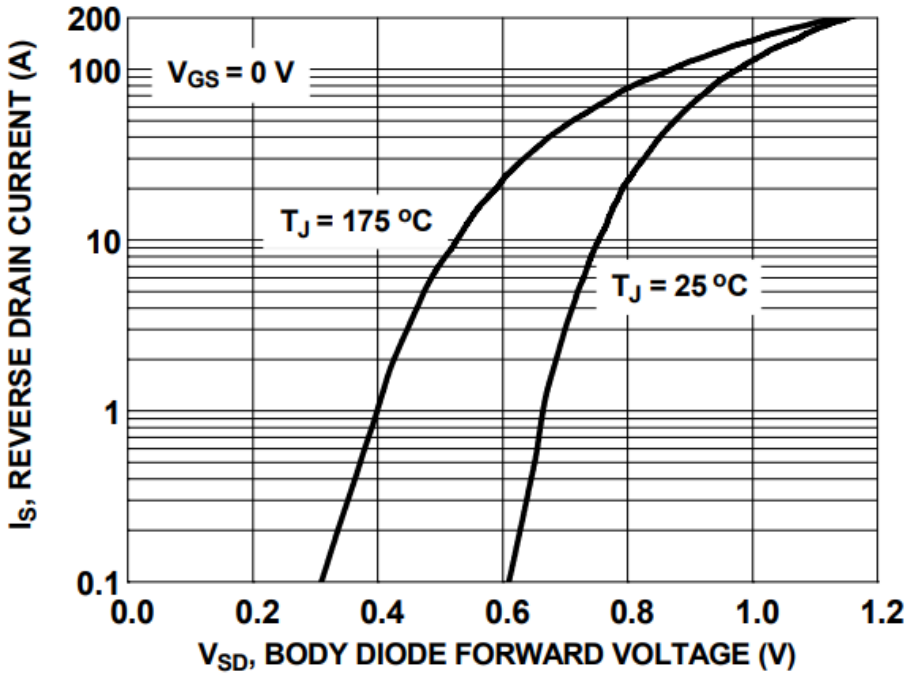
- Forward Bias Safe Operating Area



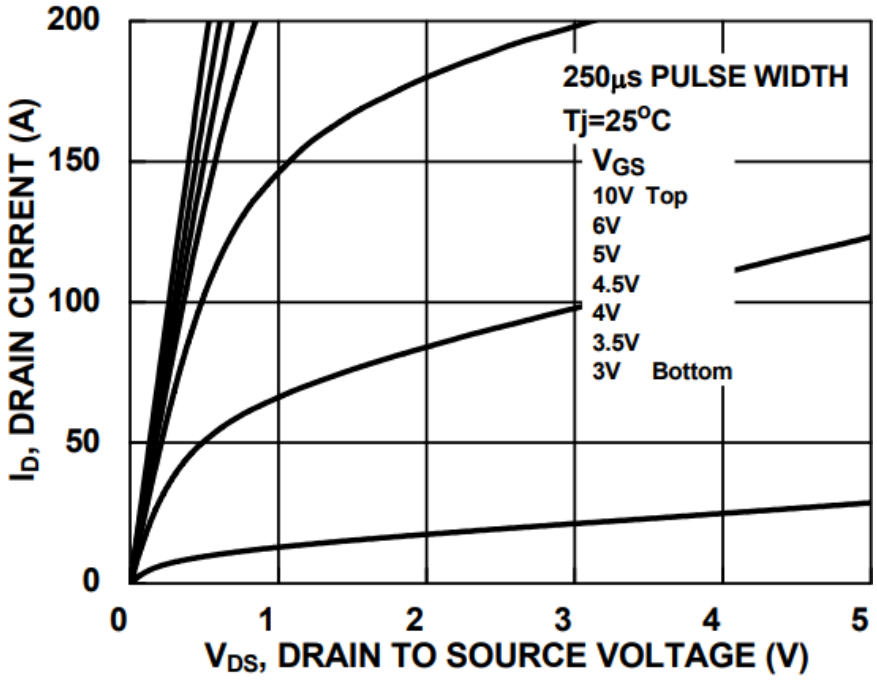
- Unclamped Inductive Switching Capability



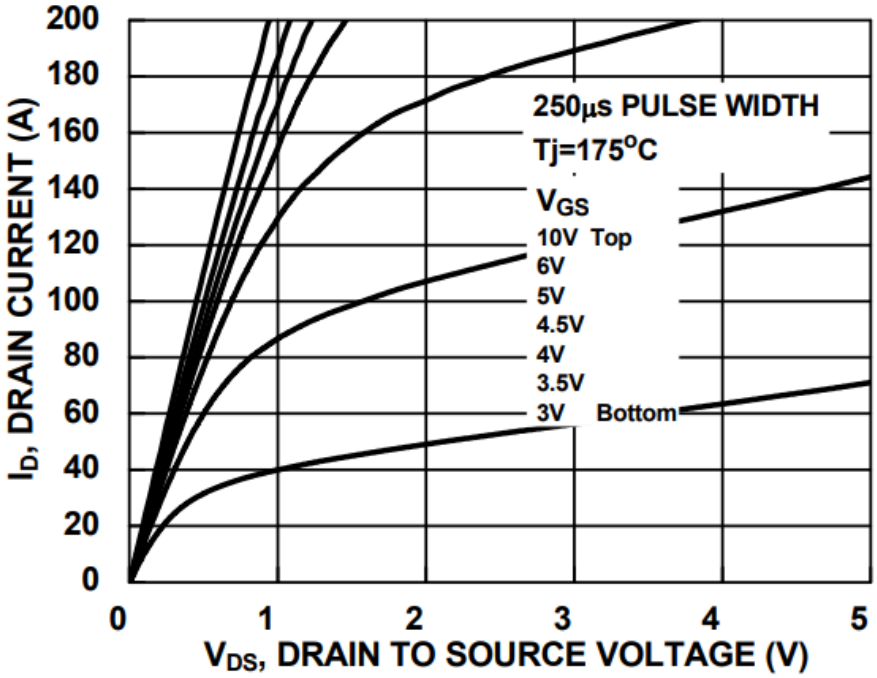
- Transfer Characteristics



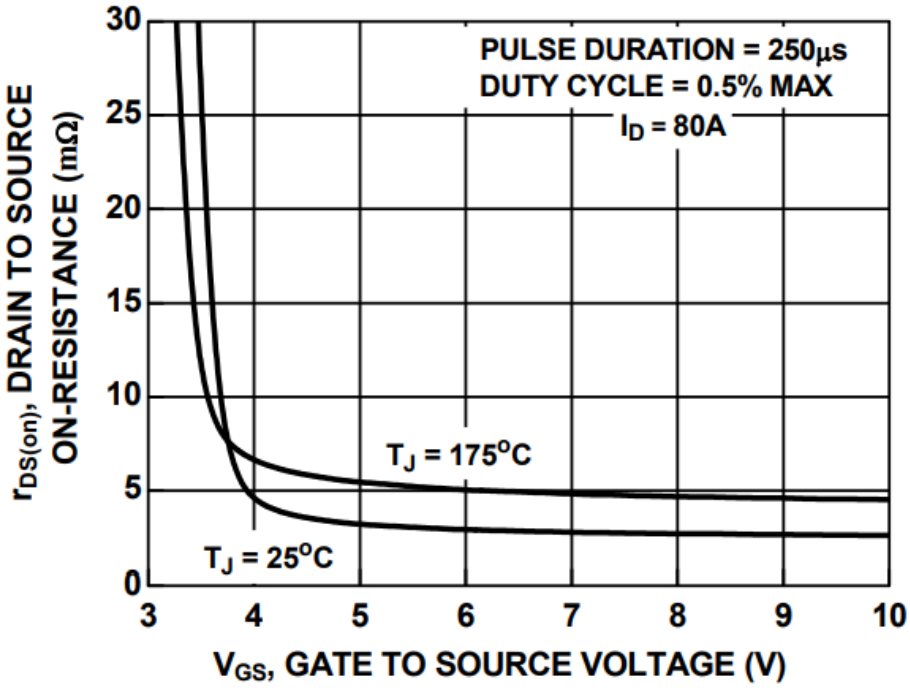
- Forward Diode Characteristics



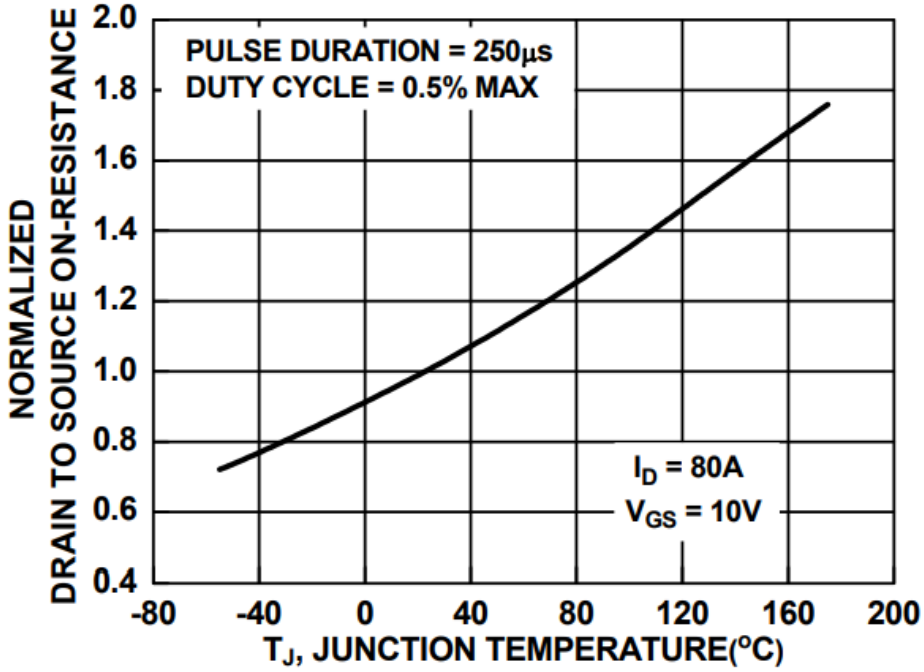
- Saturation Characteristics



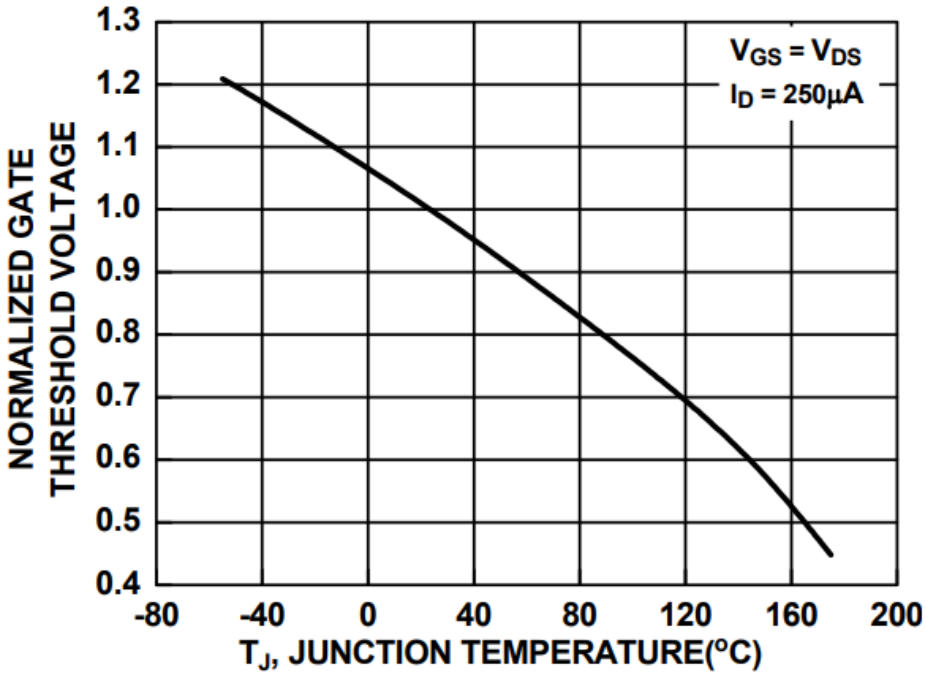
- Saturation Characteristics



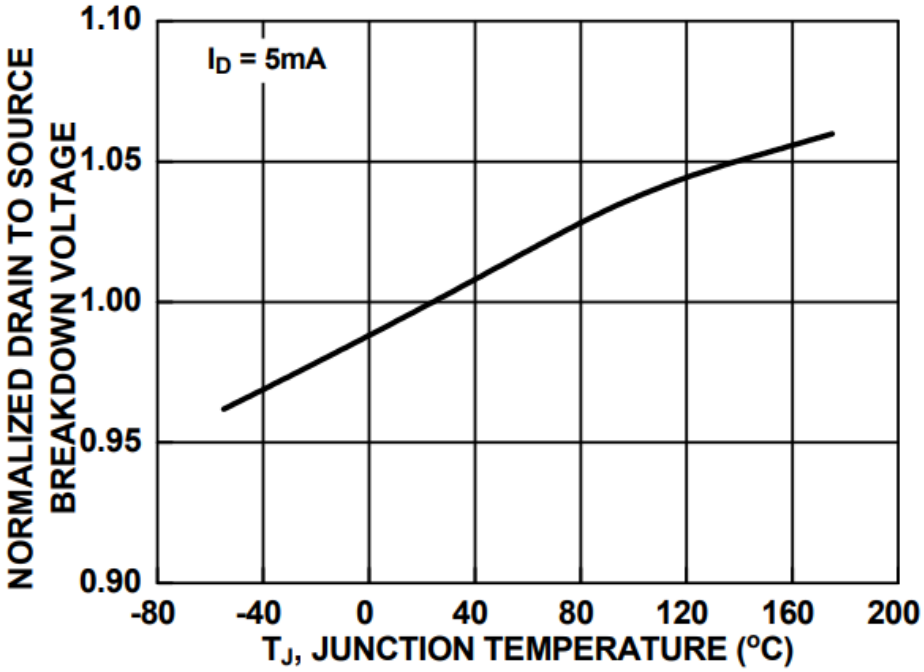
- RDSoN VS. Gate Voltage



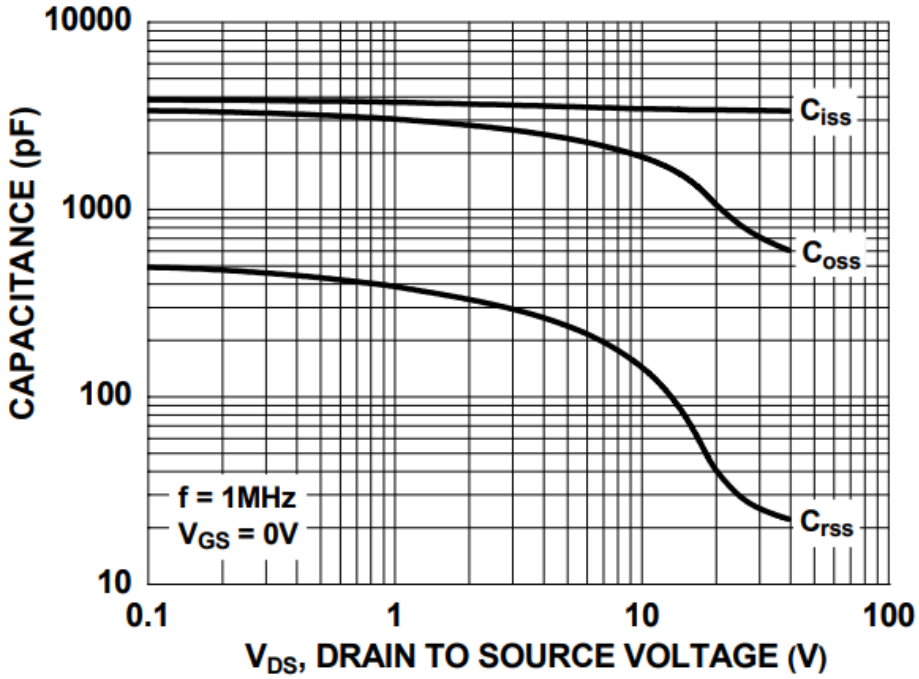
- Normalized Roson VS. Junction Temperature



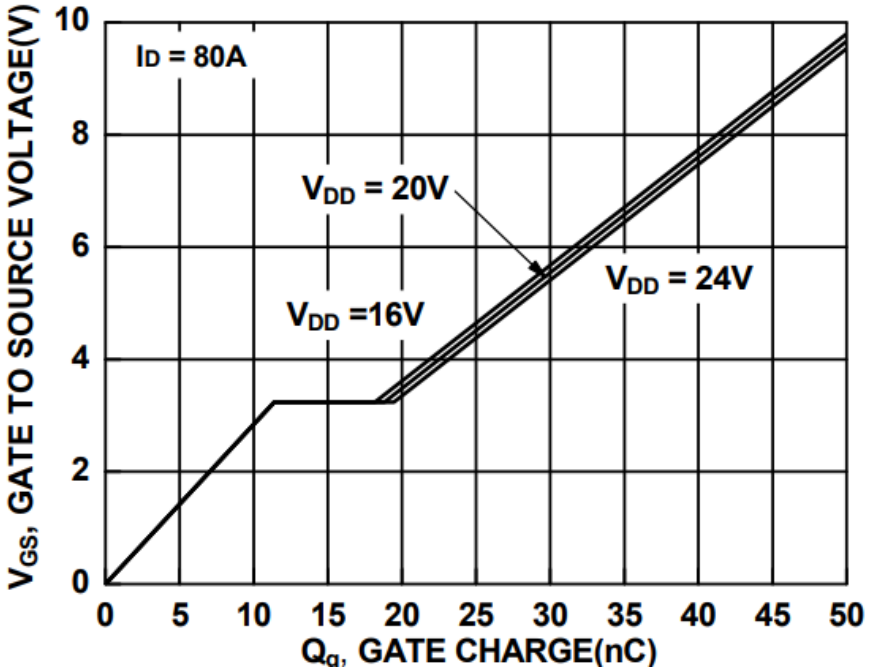
- Normalized Gate Threshold Voltage vs. Temperature



- Normalized Drain to Source Breakdown Voltage vs. Junction Temperature



- Capacitance vs. Drain to Source Voltage



- Gate Charge vs. Gate to Source Voltage

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FAQs

Q: What is the maximum thermal resistance of the product?

A: The maximum thermal resistance, junction to ambient, is 52°C/W.

Q: What are the off characteristics of the product?

A: The drain-to-source breakdown voltage is 40V, and the drain-to-source leakage current is specified under given conditions.

Q: How do I determine the gate-to-source threshold voltage?

A: The gate-to-source threshold voltage can be found with the specified test conditions provided in the manual.

Documents / Resources

	ON Semiconductor FDD9409L-F085 Channel Logic Level Power Trench [pdf] Owner's Manual FDD9409L-F085 Channel Logic Level Power Trench, FDD9409L-F085, Channel Logic Level Power Trench, Logic Level Power Trench, Level Power Trench, Power Trench

References

- User Manual

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