

NXP TEA2093DB2202 Synchronous Rectifier Evaluation Board User Manual

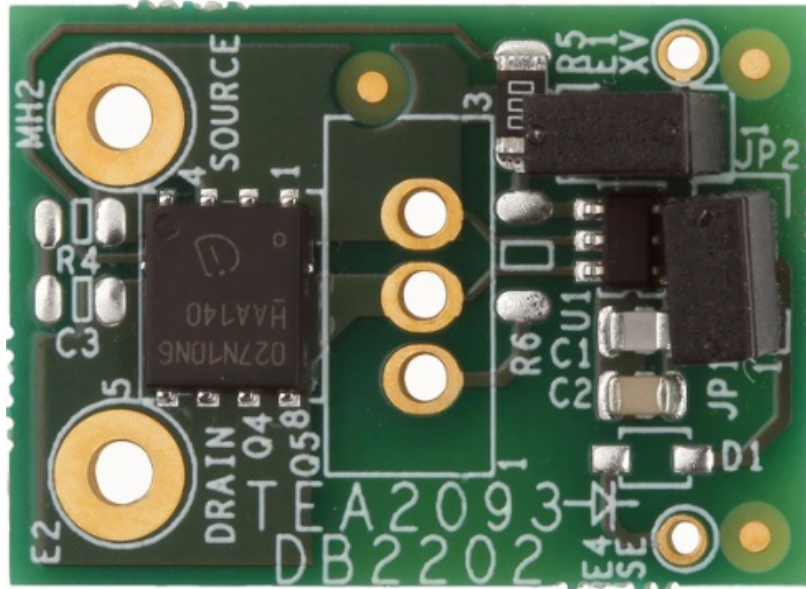
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NXP TEA2093DB2202 Synchronous Rectifier Evaluation Board



Product Information

Product Name	TEA2093DB2202 synchronous rectifier evaluation board
Revision	Rev. 1
Date	13 June 2022
Keywords	TEA2093DB2202, TEA2093TS, asymmetrical half-bridge converter, synchronous rectifier (SR) driver, TSOP-6, high efficiency, power supply, evaluation board
Abstract	Downloaded from Arrow.com. NXP Semiconductors

Product Usage Instructions

1. **Important Notice:** This product is intended for engineering development or evaluation purposes only.
2. **Safety Warning:** The board application is AC-mains voltage powered. Avoid touching the board while it is connected to the mains voltage and when it is in operation. An isolated housing is obligatory when used in uncontrolled, non-laboratory environments. Galvanic isolation from the mains phase using a fixed or variable transformer is always recommended.
3. **Introduction:** The TEA2093DB2202 evaluation board and user manual are intended for engineers involved in the evaluation and design of switch-mode power supplies (SMPS). This document contains all the information required to replace the secondary-side rectification of an existing SMPS with an asymmetrical half-bridge topology using the TEA2093DB2202 evaluation board.
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Document information

Information	Content
Keywords	TEA2093DB2202, TEA2093TS, asymmetrical half-bridge converter, synchronous rectifier (SR) driver, TSOP-6, high efficiency, power supply, evaluation board
Abstract	This user manual describes the TEA2093DB2202 evaluation board. A functional description is provided, including instructions about how to connect the board, for the best results and performance. The TEA2093DB2202 evaluation board contains the secondary part of a single output asymmetrical half-bridge converter, excluding the output capacitors and the feedback control hardware. To use the TEA2093DB2202 evaluation board correctly, an asymmetrical half-bridge converter board in which the evaluation board can replace the secondary rectifier part is required.

Revision history

Rev	Date	Description
v.1	20220613	Initial version

Important notice

IMPORTANT NOTICE

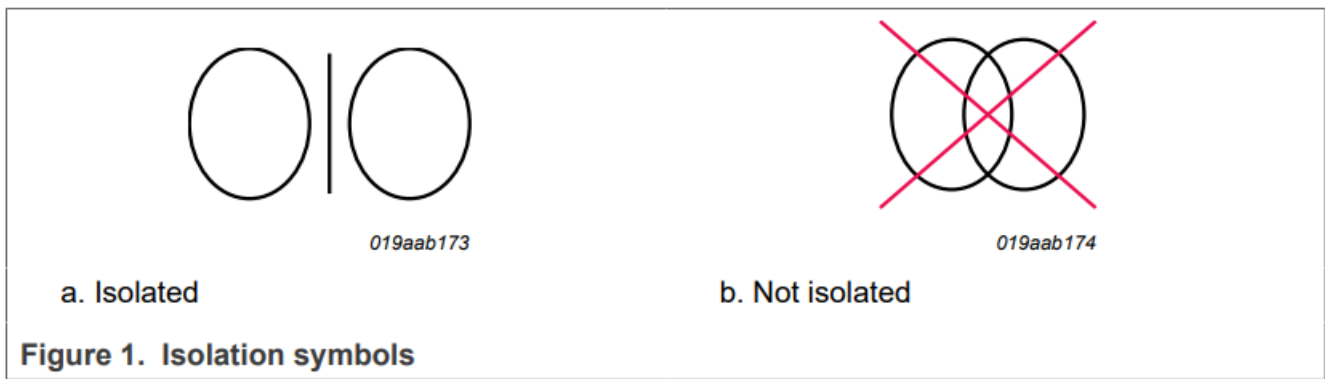
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Figure 1 shows the symbols on how to recognize these devices.



Introduction

WARNING-Lethal voltage and fire ignition hazard

The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/ or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with noninsulated mains voltages and high-voltage circuits. This product shall never be operated unattended. The TEA2093DB2202 evaluation board and user manual are intended for engineers involved in the evaluation and the design of switch-mode power supplies (SMPS). This document contains all the information required to replace the secondary-side rectification of an existing SMPS with an asymmetrical half-bridge topology with the TEA2093DB2202 evaluation board.

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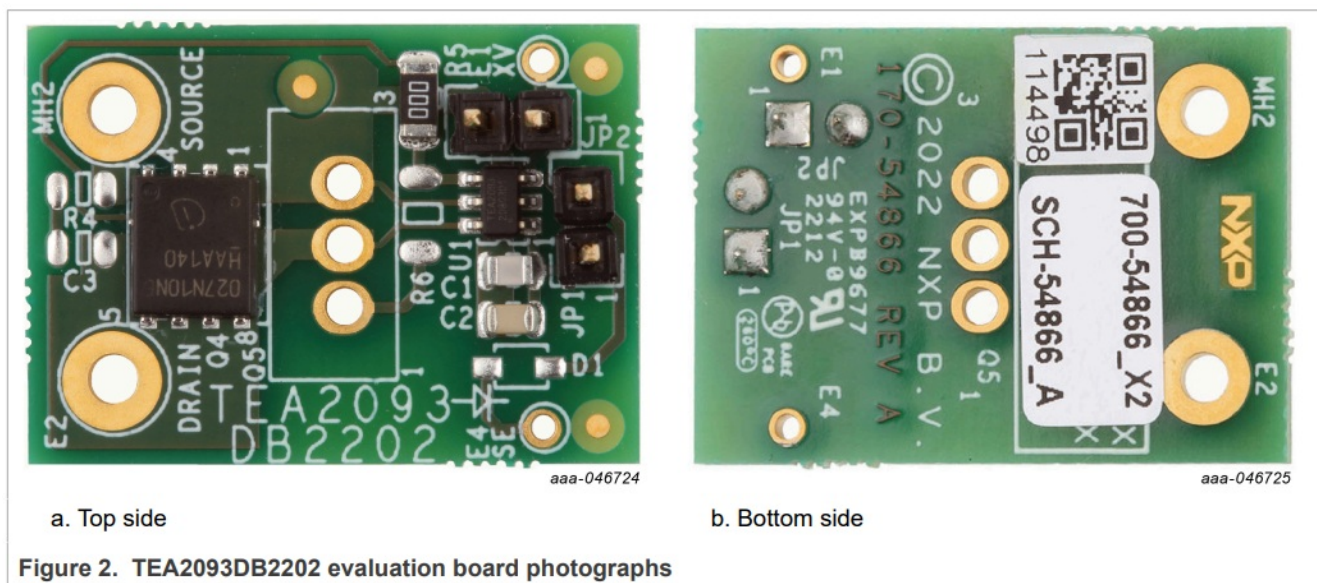
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Getting ready

• Box contents

The box contains the TEA2093DB2202 evaluation board, which incorporates the TEA2093TS in a TSOP-6 package and a MOSFET in a TDSO-FL package with a typical $R_{DS(on)}$ of 2.3 m Ω . Figure 2 shows the front side and the back side of the TEA2093DB2202 evaluation board. The TEA2093DB2202 evaluation board is a singlelayer board, which includes plated-through vias for external connections and a TO-220 MOSFET as a replacement for the mounted MOSFET Q4.



• Additional hardware

The TEA2093DB2202 evaluation board must be placed on an existing SMPS. Details can be found in Section 6.3 and Section 7.

Getting to know the hardware

Overview

The TEA2093DB2202 evaluation board contains a TEA2093TS SR controller in a TSOP-6 package and a 100 V MOSFET in a TDSON-FL package. It replaces the secondary-side rectification part of an SMPS with an asymmetrical half-bridge topology. Additionally, the TEA2093DB2202 evaluation board contains an option to replace the mounted MOSFET by a MOSFET in a TO-220 package. The TEA2093TS is a dedicated controller IC for synchronous rectification (SR) on the secondary side of asymmetrical half-bridge converters. It incorporates the sensing stage and the driver stage for driving the SR MOSFET, which rectifies the output of the secondary transformer winding. The TEA2093TS can generate its own supply voltage or operate with an external applied voltage. The self-supply function is intended for: .

- Battery-charging applications with a 2 V (USB BC) output voltage
- Applications with high-side rectification without an auxiliary winding
- Multiple output voltage applications with or without auxiliary winding

Features

- Easy replacement of secondary-side rectifier
- A 100 V/2.7 mΩ MOSFET is incorporated
- Self-supplying for low-side rectification with low output voltage (CC mode)
- Self-supplying for high-side rectification without the use of an auxiliary winding
- Operates with standard-level and logic-level SR MOSFETs

Block diagram

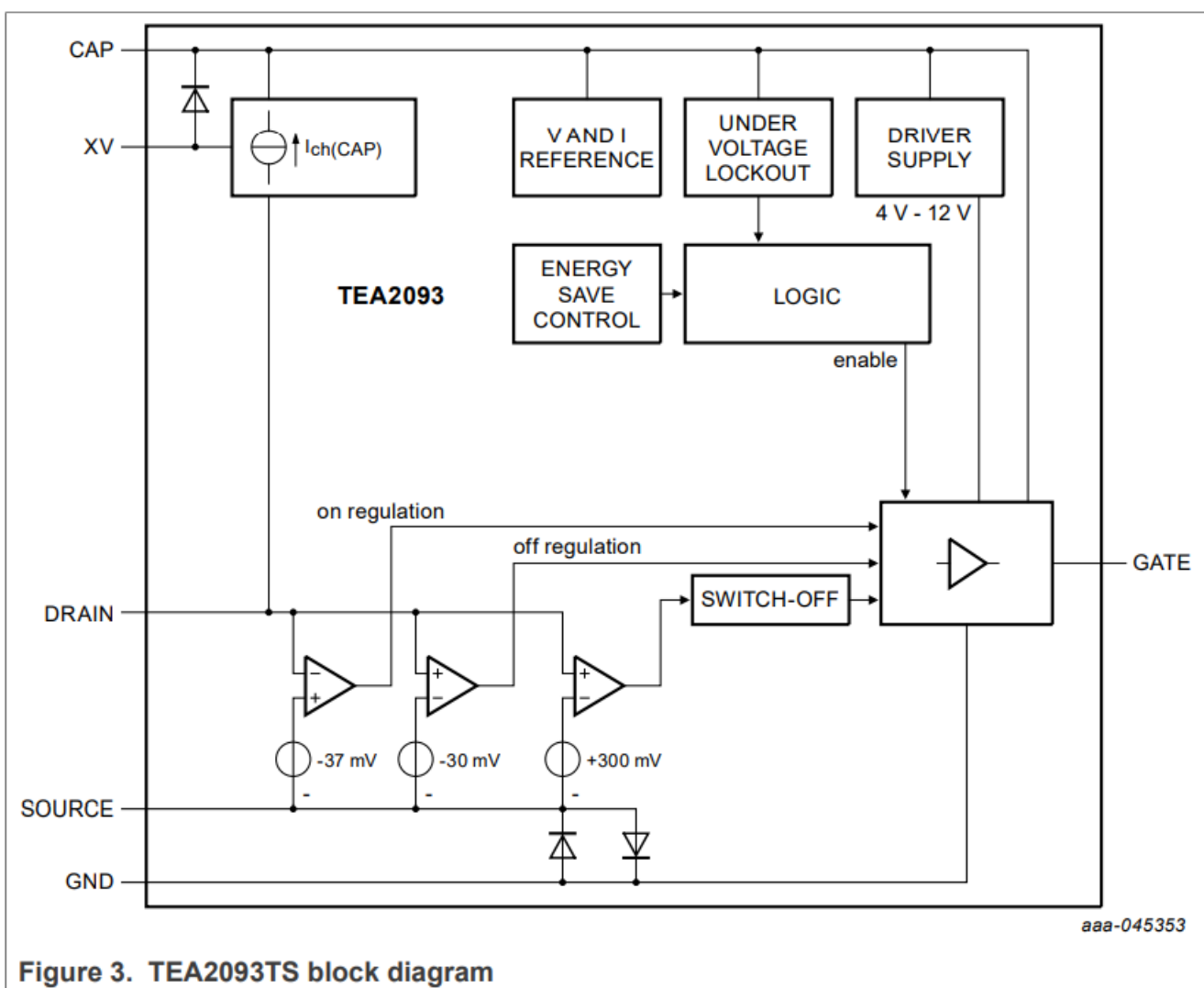


Figure 3. TEA2093TS block diagram

Board description

The board incorporates the TEA2093TS SR controller and a power MOSFET. The TEA2093TS acts as a controlled amplifier. The input is the voltage difference between the DRAIN and the SOURCE pins. The corresponding gate driver signal is the output. The amplifier regulates the source-to-drain voltage difference to 37 mV in the rectification phase. To facilitate easy layout design for a single-sided board, resistors R1 and R2 are added. They must be between 0 Ω and 10 Ω . For the fastest turn-off time, use the lowest value. By default, the TDSO-FL MOSFET Q4 is mounted with a 0 Ω gate resistor (R1). It is also possible to mount a TO220 MOSFET Q5 with gate resistor R2. Capacitors C1 and C2 are decoupling capacitors for the VCC of the TEA2093TS. To ensure sufficient charge power during the secondary stroke to drive the external MOSFET, a value of 100 nF is used for capacitor C2. To prevent unwanted oscillation of the VCC supply, capacitor C1 is added. A provision is made for snubber R3/C3. The components are not mounted. However, if high-voltage spikes occur on the drain-source connections of the MOSFETs, they can be added. To facilitate optimal configurations for either the low-side or the high-side connection, jumpers JP1 and JP2 are added (see the diagrams in Section 7).

Configuring the hardware

• Connected at low-side SR

The TEA2093DB2202 evaluation board must be incorporated in an existing asymmetrical half-bridge SMPS. Figure 4 shows the connection of the TEA2093DB2202 evaluation board to the secondary side of an asymmetrical half-bridge SMPS as low-side SR.

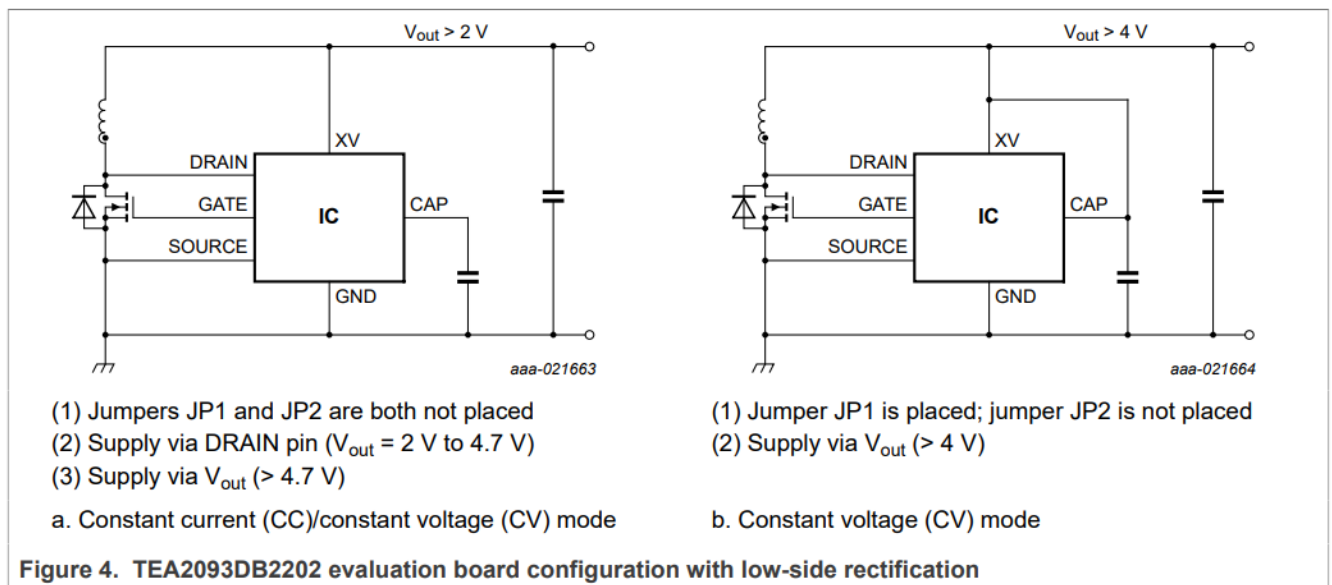


Figure 4(a) shows the configuration for SR low-side applications, which include CC mode (for example, USB BC specification for an operation between 2 V and 5 V). When $V_{out} \geq 4.7$ V, the TEA2093TS uses the voltage on the XV pin as supply. The resulting voltage on the CAP pin is typically 0.7 V below the voltage on the XV pin. It is used as supply voltage for the gate drive output to the external MOSFET. When $V_{out} < 4.7$ V (CC mode), the TEA2093TS uses the pulsed voltage on the drain input to generate the voltage for the CAP pin. When 0 V $< V_{out} < 4.7$ V, the regulated voltage on the CAP pin is 4.0 V (typical). Figure 4(b) shows the configuration for SR low-side application for CV mode only. V_{out} must be ≥ 4 V. In this case, the CAP pin can be connected directly to the XV pin. The result of connecting the CAP pin directly to the XV pin is 0.7 V additional gate drive voltage compared to the configuration in Figure 4(a). To achieve the best efficiency, the additional gate drive voltage drives the external MOSFET to a lower $R_{DS(on)}$. The maximum gate drive voltage is 12 V. Maximum voltage ratings for TEA2093TS pins:

- Pins XV and CAP: 38 V
- Pin DRAIN: 120 V

Connected at high-side SR

Figure 5 shows the connection of the TEA2093DB2202 evaluation board to the secondary side of an asymmetrical half-bridge SMPS as high-side SR.

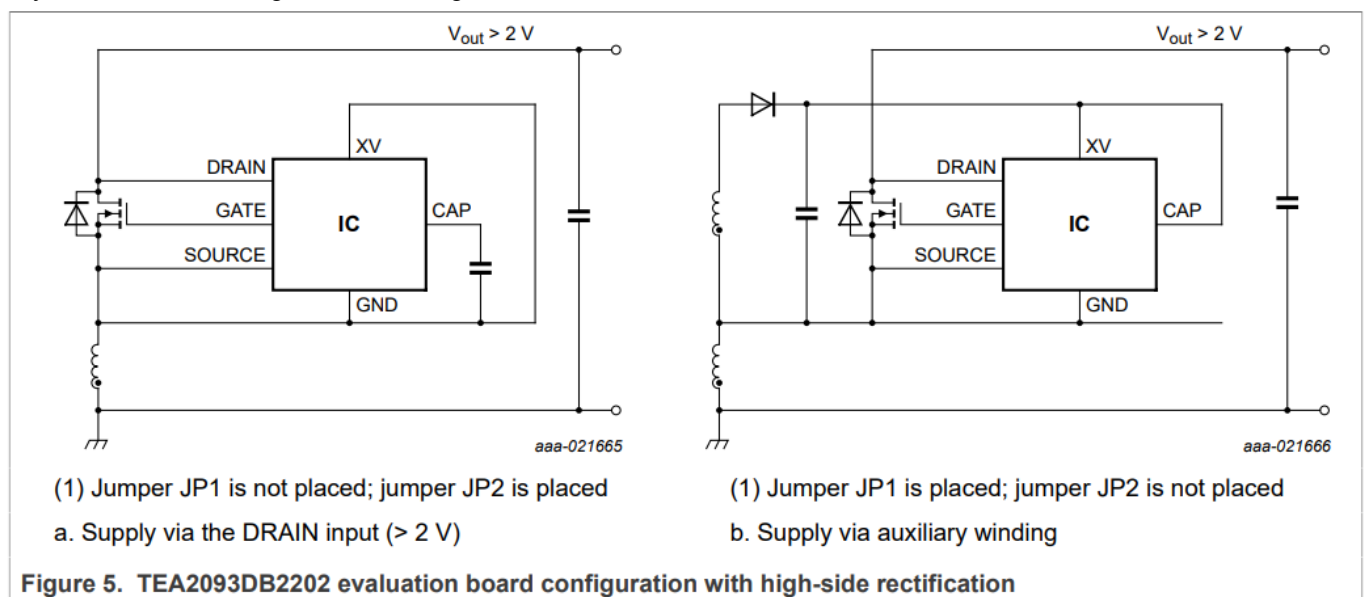


Figure 5(a) shows the configuration for SR high-side applications with self-supply. In this case, the TEA2093TS retrieves its supply from the pulsed voltage on the DRAIN input. The regulator inside the TEA2093TS converts these pulses to regulated DC voltage of approximately 9 V. If the XV pin is connected to the IC ground, the

TEA2093TS generates 9 V. This voltage is present on the CAP pin. It is the reference voltage for the gate drive of the external MOSFET. Figure 5(b) shows the configuration for SR high-side application which is supplied by an additional auxiliary winding. This configuration can deliver the best possible efficiency for high-side application. If the auxiliary voltage drops to below 4 V for the lower output voltages in a multiple outputs application, the TEA2093TS generates its own supply voltage. It maintains a minimum supply of 4 V on the CAP pin. The auxiliary voltage can then be optimized for the higher output voltages. In this way, maximum efficiency at maximum power is achieved.

Maximum voltage ratings for TEA2093TS pins:

- Pins XV and CAP: 38 V
- Pin DRAIN: 120 V

Schematic, board layout and bill of materials

Schematic

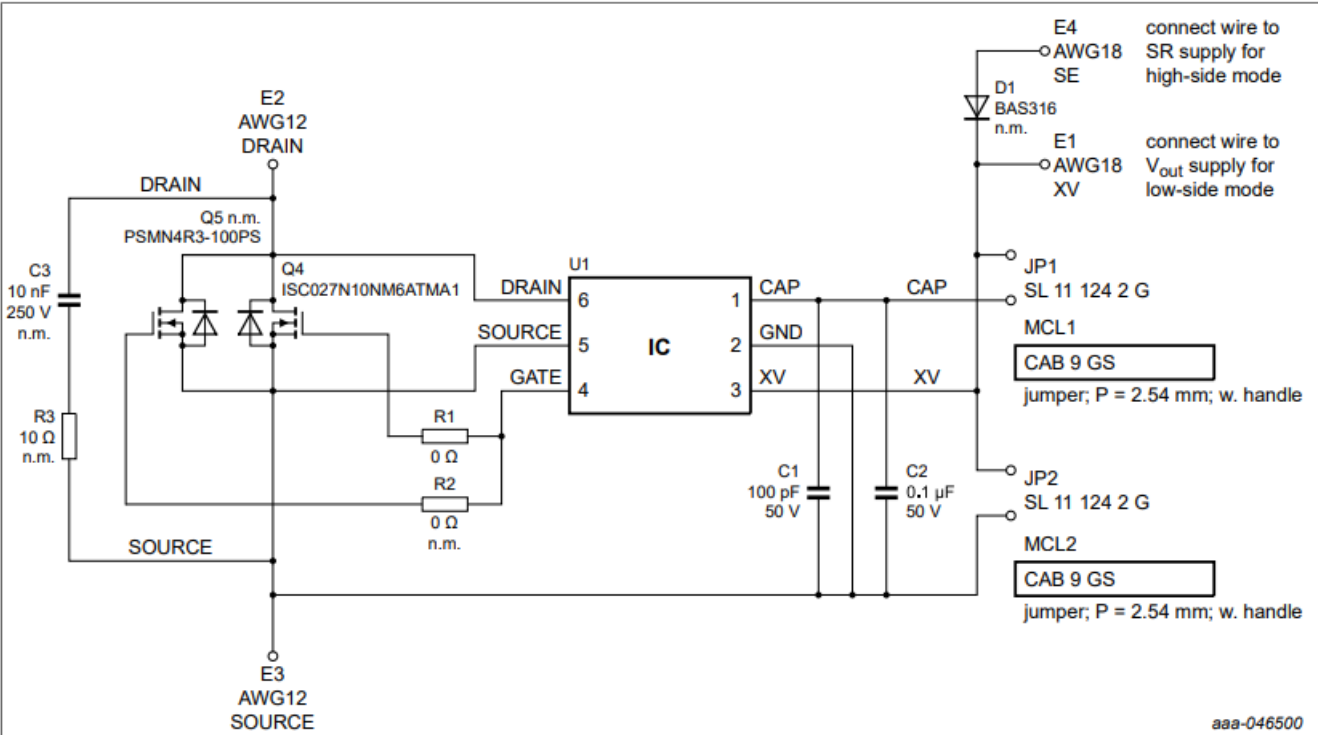


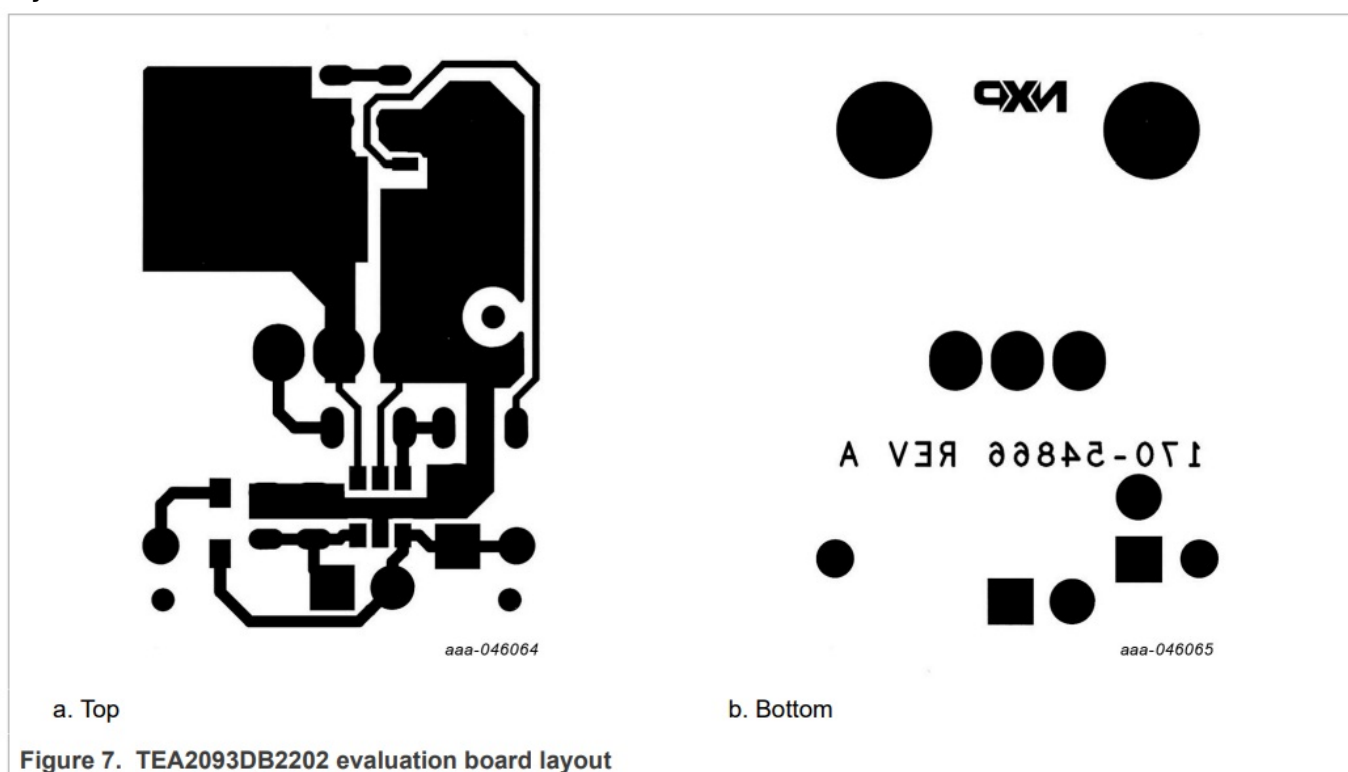
Figure 6. TEA2093DB2202 evaluation board schematic diagram

Bill of materials (BOM)

Table 1.

Reference	Description and values	Part number	Manufacturer
C1	capacitor; 100 pF; 50 V; 0805	08055A101KAT2A	AVX
C2	capacitor; 0.1 μ F; 50 V; 0805	X7R0805HTTD104K	Koa Speer
C3	capacitor; not mounted; 10 nF; 250 V; 0805	CGA4J3X7R2E103K125AA	TDK
D1	diode; not mounted; SOD323	BAS316	Nexperia
JP1; JP2	header; straight; 1 \times 2-way	SL 11 124 2 G	Fischer
MCL1; MCL2	jumper; with handle; P = 2.54 mm	CAB 9 GS	Fischer
R1	resistor; 0 Ω ; 1206	CRCW12060000Z0EA	Vishay
R2	resistor; not mounted; 0 Ω ; 1206	CRCW12060000Z0EA	Vishay
R3	resistor; not mounted; 10 Ω ; 0805	CR0805-JW-100ELF	Bourns
Q4	MOSFET; TDSON-FL	ISC027N10NM6ATMA1	Infineon
Q5	MOSFET; not mounted; TO220AB	PSMN4R3-100PS	Nexperia
U1	SR controller; TSOP6	TEA2093TS	NXP Semiconductors

Layout



Below are several important guidelines for a good layout:

- Keep the trace from the DRAIN pin to the MOSFET drain as short as possible.
- Keep the trace from the SOURCE pin to the MOSFET source as short as possible.
- Keep the area of the loop from the DRAIN pin to the MOSFET drain, to the MOSFET source, and to the SOURCE pin as small as possible. Ensure that the overlap of this loop over the power drain track or the power

source track is as small as possible. The two loops must not cross each other.

- Keep the track from the GATE pin to the gate of the MOSFET as short as possible.
- Use separate clean tracks for the XV and the GND pins. If possible, use a small ground plane underneath the IC, which improves the heat dispersion.
- Place capacitors C1 and C2 close to the IC.

Abbreviations

Table 2. Abbreviations

Acronym	Description
CC	constant current
CV	constant voltage
MOSFET	metal-oxide-semiconductor field-effect transistor
SMPS	switch-mode power supply
SR	synchronous rectifier

References

1. **TEA2093TS data sheet** — GreenChip synchronous rectifier controller; 2022, NXP Semiconductors.

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