NXP T2080RDBPCQS QorIQ T2080 Reference Design Board User Guide

Contents

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NXP-T2080RDBPCQS-QorIQ T2080 Reference-Design-Board

Introduction

The T2080 reference design board (T2080RDB-PC) system is a hardware board, supporting the NXP QorIQ® T2080 Power Architecture® processor with four dual-threaded e6500 cores and speed up to 1.8 GHz.
For the T2080 RDB system, the prototype part number is X-T2080RDB-PC and the production part number is T2080RDB-PC.

Related documentation

Some of the documents listed in the table below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1. Useful references

Document name	Description
QorIQ T2080 Reference Design Board (T2080RDB-PC) User Guide	**This document explains the procedure to build, configure, and use different components for the NXP T2080RDB board.**
QorIQ T2080 Reference Manual	**This document provides a detailed description on T2080 QorIQ multicore processor, and on some of its features, such as memory map, serial interfaces, power supply, chip features, and clock information.**
T2080 Product Brief	**This document provides an overview of the NXP T2080 features, and usage examples of T2080.**
QorIQ T2080 Data Sheet	**This document contains T2080 information on** **pin assignments, electrical characteristics, hardware design, considerations, package information, and ordering information.**

Preparing board

This board has two working modes, the Standalone mode and PCIe Endpoint mode. By default, the system is in Standalone working mode with 1U chassis. For the PCIe Endpoint mode operation, take the board out from the 1U chassis and install the PCIe bracket on the board. Now, the board can be plugged into a PCIe x4 slot in X86 server, and it can work as a PCIe card. Figure 1 shows the I/O of the front panel of the 1U chassis, and Figure 2 shows the PCIe card.

Figure 1. T2080RDB-PC front panel

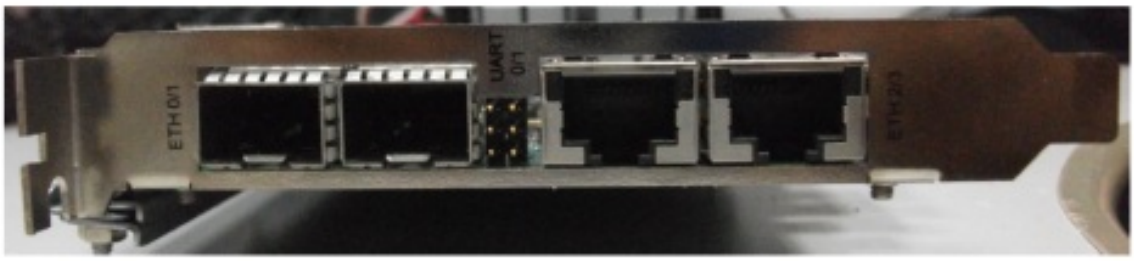


Figure 2. T2080RDB-PC PCIe card

To prepare the T2080RDB-PC for use, the default configuration should be:

- CPU: 1.8 GHz
- DDR: 1866 MT/s 4 GB

The steps to prepare a T2080RDB board are:

1. Attach an RS-232 cable between the T2080RDB UART0 port (Rx-GND-Tx 3 pins) and host computer.
2. Open a serial connection on the host computer to communicate with the T2080RDB board.
3. Configure the serial port of the host computer with the following settings:
    - Data rate: 115200 bit/s
    - Number of data bits: 8
    - Parity: None
    - Number of stop bits: 1
    - Flow control: Hardware/None
4. Push the power button on the front side of the chassis. The board boots up and shows the following U-Boot console messages:

```
U-Boot 2021.04-00117-g4ec2be0782c7 (Jul 28 2021 - 19:21:57 +0300)
```

```
CPU0:  T2080, Version: 1.1, (0x85300011)
Core:  e6500, Version: 2.0, (0x80400120)
Clock Configuration:
       CPU0:1799.820 MHz, CPU1:1799.820 MHz, CPU2:1799.820 MHz, CPU3:1799.820 MHz,
       CCB:599.940 MHz,
       DDR:933.310 MHz (1866.620 MT/s data rate) (Asynchronous), IFC:599.940 MHz
       FMAN1: 699.930 MHz
       QMAN:  299.970 MHz
       PME:   599.940 MHz
L1:    D-cache 32 KiB enabled
       I-cache 32 KiB enabled
Reset Configuration Word (RCW):
       00000000: 1207001b 15000000 00000000 00000000
```

```
        00000010: 66150002 00000000 ec027000 c1000000
        00000020: 00800000 00000000 00000000 000307fc
        00000030: 00000000 00000000 00000000 00000004
Model: fsl,T2080RDB
```

```
Board: T2080RDB, Board rev: D CPLD ver: 0x08, boot from NOR vBank4 SERDES Reference
Clocks: SD1_CLK1=156.25MHZ, SD1_CLK2=100.00MHZ SD2_CLK1=100.00MHZ, SD2_CLK2=100.00MHZ DRAM:
Initializing....using SPD Detected UDIMM D3X856082XL10AA 2 GiB left unmapped 2 GiB (DDR3, 64-
bit, CL=13, ECC on) DDR Chip-Select Interleaving Mode: CS0+CS1 VID: Bus 0 has no device with
address 0x38 VID: Bus 0 has no device with address 0x08 VID: Bus 0 has no device with address
0x09 VID: Could not find voltage regulator on I2C. Warning: Adjusting core voltage failed.
Flash: 128 MiB L2: 2 MiB enabled Corenet Platform Cache: 512 KiB enabled Using SERDES1 Protocol:
102 (0x66) Using SERDES2 Protocol: 21 (0x15) WARN: pls set popts->cpo_sample = 0x53 in <board>/
ddr.c to optimize cpo MMC: No max bus width provided. Assume 8-bit supported. FSL_SDHC: 0
Loading Environment from Flash... OK EEPROM: Invalid ID (ff ff ff ff) In: serial Out: serial
Err: serial Net: Fman1: Uploading microcode version 106.4.18 eth0: fm1-mac1, eth1: fm1-mac2,
eth2: fm1-mac3, eth3: fm1-mac4, eth4: fm1-mac9, eth5: fm1-mac10 Hit any key to stop autoboot: 0
```

The Linux system auto boots and shows the following messages on the login screen:

```
t208rdb
login: root
root@t2080rdb:~#
```

System board interface

Figure 3 shows the top view of the T2080RDB-PC system board interface.

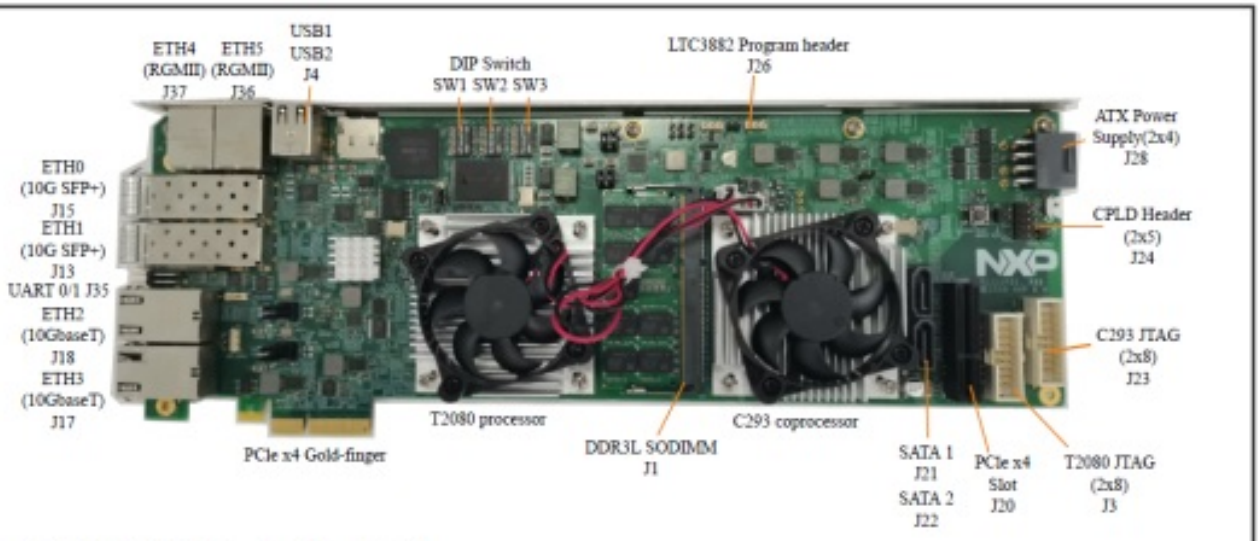
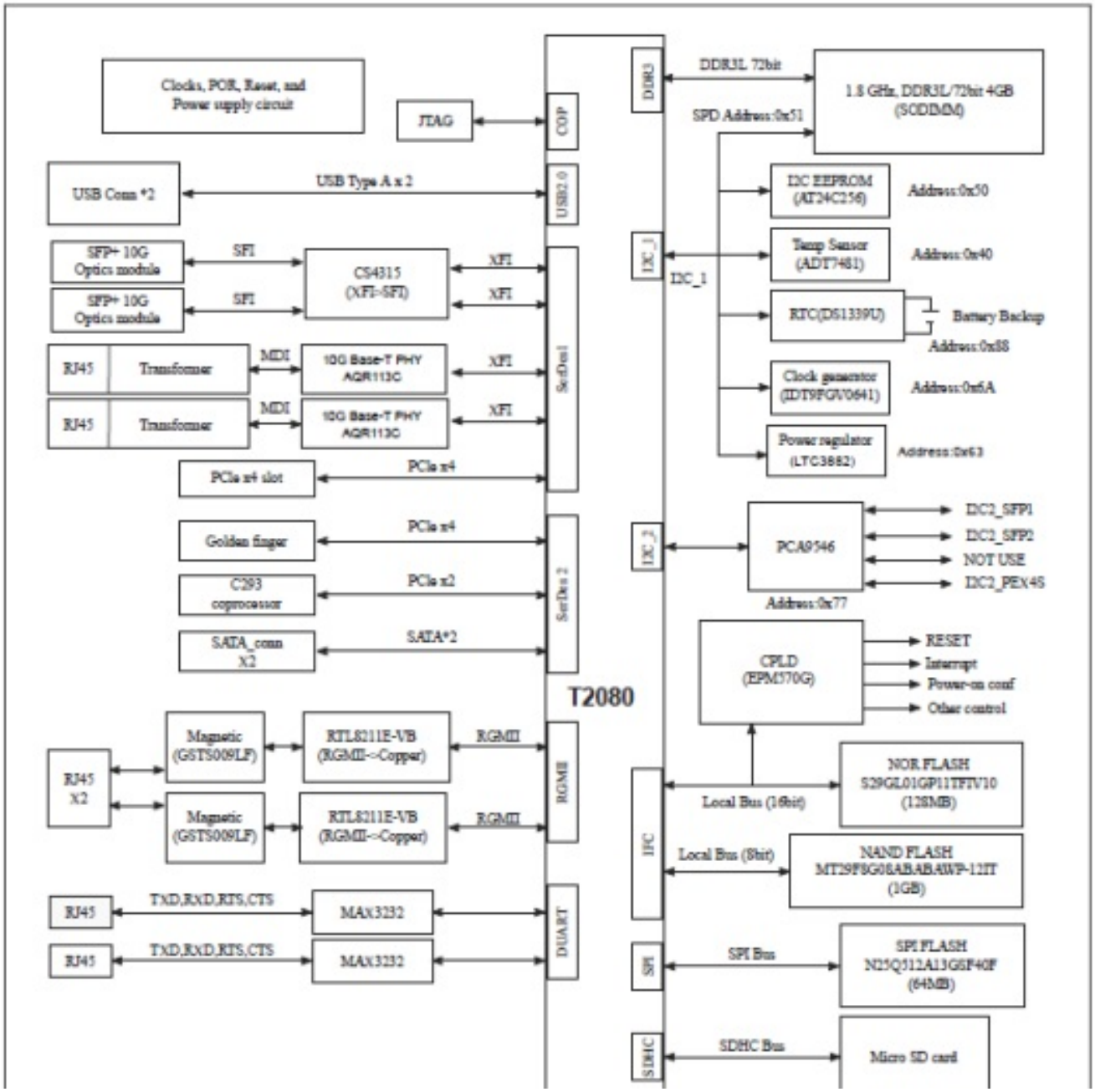


Figure 3. T2080RDB-PC system board interface

Block diagram

Figure 4 shows the high-level block diagram of the T2080RDB-PC.



Features

Some key features of the T2080RDB-PC are:

- NXP QorIQ processing platform
  - QorIQ T2080 SoC integrating four dual-threaded e6500 cores and speed up to 1.8 GHz
- Memory subsystem
  - DDR3 SDRAM
    - Single SODIMM, 72-bit DDR3L at or 1866 MT/s, based on actual DDR3L UDIMM
  - NOR flash
    - 128 MB 16-bit NOR flash, MICRON: JS28F00AM29EWHA
  - NAND flash
    - 1 GB SLC NAND flash, MICRON: MT29F8G08ABABAWP-ITX:B
  - One microSD/TF connector interface
  - Two SATA interfaces

Ethernet

- ETH 0 – ETH 1: XFI 10G SFP+, connected to Cortina CS4315 PHY
- ETH 2 – ETH 3: XFI 10GBase-T copper twisted-pair cable, connected to x2 AQR113C PHYs
- ETH 4 – ETH 5: 10 Mbit/s, 100 Mbit/s, or 1 Gbit/s RGMII, connected to RTL8211E PHY

PCIe

- One PCIe-x4 gold-finger
- One PCIe-x4 connector
- One crypto co-processor C293 PCIe Endpoint device

USB 2.0

- One dual-USB slot, connected to USB PHY

UART

- Supports two UARTs, up to 115200 bit/s for console display; uses dual RJ45 slot for the two UART ports

Real-time clock (RTC)

- Supports one DS1339U RTC

Port map

Table 2 shows how the Ethernet ports can be mapped to Linux and U-Boot.
Table 2. Ethernet port mapping

Label on front panel	Port in U-Boot	Port in Linux	FMan address	Comments
ETH0	fm1-mac9	fm1-mac9	0xfe4f0000	10GBase-T SFP+ (Cortina 4315)
ETH1	fm1-mac10	fm1-mac10	0xfe4f2000	10GBase-T SFP+ (Cortina 4315)
ETH2	fm1-mac1	fm1-mac1	0xfe4e0000	10GBase-T (AQR113C)
ETH3	fm1-mac2	fm1-mac2	0xfe4e2000	10GBase-T (AQR113C)
ETH4	fm1-mac3	fm1-mac3	0xfe4e4000	1G RGMII (RTL8211E)
ETH5	fm1-mac4	fm1-mac4	0xfe4e6000	1G RGMII (RTL8211E)

Flash image layout

Table 3 shows the flash image layout.
Table 3. Flash image layout

Start address	End address	Image	Maximum size
0xEFF40000	0xEFFFFFFF	U-Boot (current bank)	768 kB
0xEFF20000	0xEFF3FFFF	U-Boot environment (current bank)	128 kB
0xEFF00000	0xEFF1FFFF	FMan microcode (current bank)	128 kB

0xEFE00000	**0xEFE3FFFF**	**PHY CS4315 firmware**	**256 kB**
0xED300000	**0xEFEFFFFF**	**rootfs (alternate bank)**	**44 MB**
0xEC800000	**0xEC8FFFFF**	**Hardware device tree (alternate b ank)**	**1 MB**
0xEC020000	**0xEC7FFFFF**	**Linux.uImage (alternate bank)**	**7 MB + 875 kB**
0xEC000000	**0xEC01FFFF**	**RCW (alternate bank)**	**128 kB**
0xEBF40000	**0xEBFFFFFF**	**U-Boot (alternate bank)**	**768 kB**
0xEBF20000	**0xEBF3FFFF**	**U-Boot environment (alternate ba nk)**	**128 kB**
0xEBF00000	**0xEBF1FFFF**	**FMan microcode (alternate bank)**	**128 kB**
0xEBE00000	**0xEBE3FFFF**	**PHY CS4315 firmware (alternate b ank)**	**256 kB**
0xE9300000	**0xEBEFFFFF**	**rootfs (current bank)**	**44 MB**
0xE8800000	**0xE88FFFFF**	**Hardware device tree (current ba nk)**	**1 MB**
0xE8020000	**0xE87FFFFF**	**Linux.uImage (current bank)**	**7 MB + 875 kB**
0xE8000000	**0xE801FFFF**	**RCW (current bank)**	**128 kB**

Default RCW setting

Table 4 shows the default reset configuration word (RCW) settings.
Table 4. Default RCW settings

No	RCW words	Description
1	0x120c0017	120c: System PLL rate is 1:9 (SYSCLK is 66.66 MHz) and DDR PLL rate is 1:12 (DDRCLK is 133.33 MHz) 0017: Cluster 1 core PLL rate is 1:23 (SYSCLK is 66.66 MHz)
2	0x15000000	1500: Cluster 2 core PLL rate is 1:21 (SYSCLK is 66.66 MHz) 0000: Reserved
3	0x00000000	Reserved
4	0x00000000	Default setting
5	0x66150002	0x66: SerDes1 protocol is 0x66 (choose four XFI and PCIe x4 on SerDes1) 0x15: SerDes2 protocol is 0x15 (choose one PCIe x4, one PCIe x2, and two SATA on SerDes2) 0x02: FMan runs 1x frequency of MAC

No	RCW words	Description
6	0x00000000	SerDes clock choice
7	0xec027000	Boot location choice
8	0xc1000000	PME frequency and DDR latency choice
9	0x00800000	PCIe1 in agent mode, others in host mode
10	0x00000000	Default setting, GPIO information
11	0x00000000	Default setting, TDM option
12	0x000307fc	0003: UART option 07fc: ASLEEP, RTC, SDHC_BASE, IRQ_OUT, IRQ_BASE, SPI_BASE option
13	0x00000000	Default setting, IFC option
14	0x00000000	0000: 1588, SDHC, RGMII, I2C, TDM option 0000: LVDD, L1VDD, CVDD, EVDD, HDLC, DMA option
15	0x00000000	Reserved
16	0x00000004	Reserved

Switch settings

The dual inline package (DIP) switch is used to configure the boot source and to power on or reset some bits. It can choose a NOR
flash vBank as a boot vBank.

Switch default settings (NOR flash boot)
NOR flash boot is the default boot mode. To boot from the NOR flash, the DIP switches should be configured, as shown in the table below.

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW1	0001 0011	ON	ON	ON	OFF	ON	ON	OFF	OFF
SW2	1011 1111	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW3	1110 0001	OFF	OFF	OFF	ON	ON	ON	ON	OFF

Other boot source settings
To boot from the NAND flash, the DIP switches should be configured, as shown in the table below.

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW1	1000 0010	OFF	ON	ON	ON	ON	ON	OFF	ON

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW2	1011 1111	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW3	1111 0001	OFF	OFF	OFF	OFF	ON	ON	ON	OFF

To boot from the SPI flash, the DIP switches should be configured, as shown in the table below.

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW1	0010 0010	ON	ON	OFF	ON	ON	ON	OFF	ON
SW2	1011 1111	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW3	1110 0001	OFF	OFF	OFF	ON	ON	ON	ON	OFF

To boot from the SD card, the DIP switches should be configured, as shown in the table below.

DIP switch	Switch binary value	1	2	3	4	5	6	7	8
SW1	0010 0000	ON	ON	OFF	ON	ON	ON	ON	ON
SW2	0011 1111	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW3	1110 0001	OFF	OFF	OFF	ON	ON	ON	ON	OFF

Switch detailed description

Table 5 shows the detailed switch description.
Table 5. Switch description

Switch	POR configuration	Signal name	Signal meaning	Setting
SW1[1]	cfg_rcw_src0	IFC_AD8	RCW source	010011011: Hard-coded RCW for JTAG debug 000100111: NOR flash boot mode 100 000101: NAND boot mode 001000101: SPI boot mode
SW1[2]	cfg_rcw_src1	IFC_AD9		
SW1[3]	cfg_rcw_src2	IFC_AD10		
SW1[4]	cfg_rcw_src3	IFC_AD11		
SW1[5]	cfg_rcw_src4	IFC_AD12		
SW1[6]	cfg_rcw_src5	IFC_AD13		
SW1[7]	cfg_rcw_src6	IFC_AD14		
SW1[8]	cfg_rcw_src7	IFC_AD15		
SW2[1]	cfg_rcw_src8	IFC_CLE		
SW2[2]	cfg_ifc_te	IFC_TE		OFF(1): IFC drives logic 0 for TE assertion
SW2[3]	cfg_pll_config_sel_b	IFC_A18		
SW2[4]	cfg_por_ainit	IFC_A19		

Switch	POR configuration	Signal name	Signal meaning	Setting
SW2[5]	cfg_svr0	IFC_A16		
SW2[6]	cfg_svr1	IFC_A17		
SW2[7]	cfg_dram_type	IFC_A21		
SW2[8]	cfg_rsp_dis	IFC_AVD		
SW3[1]	cfg_eng_use0	IFC_WE_N		OFF(1): SYSCLK clock source ON (0): Single-clock source using diff_sys_clk
SW3[2]	cfg_eng_use1	IFC_OE_N		
SW3[3]	cfg_eng_use2	IFC_WP_N		
SW3[4]		BOOT_FLASH_SE L		ON(0): Select NOR flash on CS0 ON(1): Select NAND flash on CS0
SW3[5]		CFG_VBANK0	Alter flash bank	000: NOR flash vBank 0 select 100: NOR flash vBank 4 select
SW3[6]		CFG_VBANK1		
SW3[7]		CFG_VBANK2		
SW3[8]		TEST_SEL_N		

How to program flash for the first time (without U-Boot)

To program flash for the first time (without U-Boot), perform the following steps:

1. Set DIP switches as:
    - SW1: 0100 1110 (ON is 0 and OFF is 1)
    - SW2: 1011 1111
    - SW3: 1100 0001
2. Run T2080RDB_RCW_override.cfg in CodeWarrior connection server (CCS) to override RCW.
3. Download SPI U-Boot at 0xfff40000, and set PC reg to 0xfffffffc.
4. Run with the CodeWarrior IDE, and enter U-Boot at the console.
5. Exit the CodeWarrior IDE.
6. Download the following images:
    - u-boot.bin at 0x100000
    - fman_ucode at 0x200000
    - t2080.rcw at 0x300000
    - cs4315-ucode.txt at 0x400000
7. In U-Boot, run the following commands:
8. Power down, set DIP switches as:
    - SW1: 0001 0011
    - SW2: 1011 1111
    - SW3: 1100 0001
9. Turn on power. The system enters the U-Boot environment.

Revision history

This table summarizes revisions to this document.
Table 6. Revision history

Revision	Date	Topic cross-reference	Description
Rev. 1	**08/2021**	**System board interface**	**Updated Figure 3.**
		Block diagram	**Updated Figure 4 for LTC3882 device and AQR113C PHYs detail.**
		Port map	**Updated Table 2 for AQR113C PHYs description and port names in U-Boot.**
		Preparing board	**Updated U-Boot log.**
Rev. 0	**02/2015**	**–**	**Initial public release.**

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