NXP LPC55S0x M33 Based MicroController User Manual

Contents

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Document information

Keywords

- LPC55S06JBD64. LPC55S06JHI48, LPC55S04JBD64, LPC55S04JHI48,
- LPC5506JBD64, LPC5506JHI48, LPC5504JBD64, LPC5504JHI48,
- LPC5502JBD64, LPC5502JHI48

Abstract

- LPC55S0x/LPC550x errata

Revision history

Rev	Date	Description
1.3	20211110	Added CAN-FD.1 note in Section 3.3 “CAN-FD.1: Bus transaction abort could occu r when CAN-FD peripheral is using secure alias.”.
1.2	20210810	Added VBAT_DCDC.1: Section 3.2 “VBAT_DCDC.1: The minimum rise time of the power supply must be 2.6 ms or slower for Tamb = -40 C, and 0.5 ms or slower for Tamb = 0 C to
		+105 C”
1.1	20201006	Second version.
1.0	20200814	Initial version.

Product identification

The LPC55S0x/LPC550x HTQFP64 package has the following top-side marking:

- First line: LPC55S0x/LPC550x
- Second line: JBD64
- Third line: xxxx
- The fourth line: xxxx
- The fifth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision A

The LPC55S0x/LPC550x HVQFN48 package has the following top-side marking:

- First line: LPC55S0x/LPC550x
- Second line: JHI48
- Third line: xxxxxxxx
- The fourth line: xxxx
- Fifth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision A

Errata overview

Functional problems table

Table 1. Functional problems table			
Functional problems	**Short description**	**Revision identifier**	**Detailed description**
ROM.1	ROM fails to enter ISP mode when image is corrupted with flash pages in an erased or unprogrammed state.	A	Section 3.1
VBAT_DCDC.1	The minimum rise time of the power supply must be 2.6 ms or slower for Tamb = -40 C, and 0.5 ms or slower for Tamb = 0 C to +105 C.	A	Section 3.2
CAN-FD.1	Bus transaction abort could occur when CAN-FD peripheral is using secure alias.	A	Section 3.3.

AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Errata notes

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Functional problems detail

ROM.1: ROM fails to enter ISP mode when the image is corrupted with flash pages in an erased or unprogrammed state

Introduction
On the LPC55S0x/LPC550x, if the image is corrupted with flash pages in an erased or unprogrammed state, the ROM may fail to automatically enter ISP mode.

Problem
When secure boot is enabled in CMPA, and the flash memory contains an erased or unprogrammed memory page inside the memory region specified by the image size field in the image header, the device does not automatically enter into ISP mode using the fallback mechanism, as in the case of a failed boot for an invalid image. This problem occurs when the application image is only partially written or erased but a valid image header is still present in memory.

Workaround
Perform a mass-erase to remove the incomplete and corrupted image using one of the following methods:

- Execute the erase command using Debug The device will enter directly into ISP mode after exiting the mailbox.
- Enter into ISP mode using the Debug Mailbox command and use the flash-erase command.
- Reset the device and enter into ISP mode using the ISP Use the flash-erase command to erase the corrupted (incomplete) image.

VBAT_DCDC.1: The minimum rise time of the power supply must be 2.6 ms or slower for Tamb = -40 C, and 0.5 ms or slower for Tamb = 0 C to +105 C

Introduction
The datasheet specifies no power-up requirements for the power supply on the VBAT_DCDC pin.

Problem
The device might not always start up if the minimum rise time of the power supply ramp is 2.6 ms or faster for Tamb = -40 C, and 0.5 ms or faster for Tamb = 0 C to +105 C.

Workaround
None.

CAN-FD.1: Bus transaction abort could occur when CAN-FD peripheral is using secure alias

Introduction
Unlike CM33, for other AHB masters (CAN-FD, USB-FS, DMA), the security level of the transaction is fixed based on the level assigned for the master in SEC_AHB->MASTER_SEC_LEVEL register. So, if the application needs to restrict the CAN-FD to secure, the following steps are required:

- Set the security level of CAN-FD to secure-user (0x2) or secure privilege (0x3) in SEC_AHB->MASTER_SEC_LEVEL register.
- Assign secure-user or secure-privilege level for CAN-FD register space in SEC_AHB-> SEC_CTRL_AHB_PORT8_SLAVE1 Register.
- Assign secure-user or secure-privilege level for message RAM.

Example:
If 16KB of SRAM 2 (0x2000_C000) bank is used for CAN message RAM. Then set rules in SEC_AHB-> SEC_CTRL_RAM2_MEM_RULE0 register to secure-user (0x2) or secure privilege (0x3).

Problem
The shared memory used by the CAN-FD controller and CPU should be accessible using secure alias with address bit 28 set (example 0x3000_C000). However, when CAN-FD makes a bus transaction using secure alias (address bit 28 set), the transaction is aborted.

Workaround

- When CPU is accessing the CAN-FD register or message RAM it should always use secure alias i.e., 0x3000_C000 for message RAM manipulation. .
- For any structure the CAN-FD peripheral uses to fetch or write, memory should be set to use 0x2000_C000 in order for bus transactions to work. CAN-FD software driver should set “Message RAM base address register (MRBA, offset 0x200)” with the physical address of RAM instead of secure alias.

AC/DC deviations detail

No known errata.

Errata notes detail

No known errata.

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Documents / Resources

	**NXP LPC55S0x M33 Based MicroController** [pdf] User Manual LPC55S0x, M33 Based MicroController, Based MicroController, LPC55S0x, MicroController

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