



# NXP LPC55S0x M33 Based MicroController User Manual

[Home](#) » [NXP](#) » NXP LPC55S0x M33 Based MicroController User Manual 

## Contents

- 1 NXP LPC55S0x M33 Based MicroController
- 2 Document information
- 3 Product identification
- 4 Errata overview
- 5 Functional problems detail
- 6 AC/DC deviations detail
- 7 Errata notes detail
- 8 Limited warranty and liability
- 9 Documents / Resources
  - 9.1 References
- 10 Related Posts



**NXP LPC55S0x M33 Based MicroController**



## Document information

### Keywords

- LPC55S06JBD64, LPC55S06JHI48, LPC55S04JBD64, LPC55S04JHI48,
- LPC5506JBD64, LPC5506JHI48, LPC5504JBD64, LPC5504JHI48,
- LPC5502JBD64, LPC5502JHI48

### Abstract

- LPC55S0x/LPC550x errata

### Revision history

Rev	Date	Description
1.3	20211110	Added CAN-FD.1 note in Section 3.3 “CAN-FD.1: Bus transaction abort could occur when CAN-FD peripheral is using secure alias.”.
1.2	20210810	Added VBAT_DCDC.1: Section 3.2 “VBAT_DCDC.1: The minimum rise time of the power supply must be 2.6 ms or slower for Tamb = -40 C, and 0.5 ms or slower for Tamb = 0 C to
		+105 C”
1.1	20201006	Second version.
1.0	20200814	Initial version.

### Product identification

The LPC55S0x/LPC550x HTQFP64 package has the following top-side marking:

- First line: LPC55S0x/LPC550x
- Second line: JBD64
- Third line: xxxx
- The fourth line: xxxx
- The fifth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision A

The LPC55S0x/LPC550x HVQFN48 package has the following top-side marking:

- First line: LPC55S0x/LPC550x
- Second line: JHI48
- Third line: xxxxxxxx
- The fourth line: xxxx
- Fifth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision A

## Errata overview

### Functional problems table

Table 1. Functional problems table			
Functional	Short description problems	Revision identifier	Detailed description
ROM.1	ROM fails to enter ISP mode when image is corrupted with flash pages in an erased or unprogrammed state.	A	Section 3.1
VBAT_DCDC.1	The minimum rise time of the power supply must be 2.6 ms or slower for Tamb = -40 C, and 0.5 ms or slower for Tamb = 0 C to +105 C.	A	Section 3.2
CAN-FD.1	Bus transaction abort could occur when CAN-FD peripheral is using secure alias.	A	Section 3.3.

### AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

### Errata notes

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

## Functional problems detail

### ROM.1: ROM fails to enter ISP mode when the image is corrupted with flash pages in an erased or unprogrammed state

#### Introduction

On the LPC55S0x/LPC550x, if the image is corrupted with flash pages in an erased or unprogrammed state, the ROM may fail to automatically enter ISP mode.

#### Problem

When secure boot is enabled in CMPA, and the flash memory contains an erased or unprogrammed memory page inside the memory region specified by the image size field in the image header, the device does not automatically enter into ISP mode using the fallback mechanism, as in the case of a failed boot for an invalid image. This problem occurs when the application image is only partially written or erased but a valid image header is still present in memory.

#### Workaround

Perform a mass-erase to remove the incomplete and corrupted image using one of the following methods:

- Execute the erase command using Debug The device will enter directly into ISP mode after exiting the mailbox.
- Enter into ISP mode using the Debug Mailbox command and use the flash-erase command.
- Reset the device and enter into ISP mode using the ISP Use the flash-erase command to erase the corrupted (incomplete) image.

### VBAT\_DCDC.1: The minimum rise time of the power supply must be 2.6 ms or slower for Tamb = -40 C, and 0.5 ms or slower for Tamb = 0 C to +105 C

#### Introduction

The datasheet specifies no power-up requirements for the power supply on the VBAT\_DCDC pin.

#### Problem

The device might not always start up if the minimum rise time of the power supply ramp is 2.6 ms or faster for Tamb = -40 C, and 0.5 ms or faster for Tamb = 0 C to +105 C.

#### Workaround

None.

### CAN-FD.1: Bus transaction abort could occur when CAN-FD peripheral is using secure alias

#### Introduction

Unlike CM33, for other AHB masters (CAN-FD, USB-FS, DMA), the security level of the transaction is fixed based on the level assigned for the master in SEC\_AHB->MASTER\_SEC\_LEVEL register. So, if the application needs to restrict the CAN-FD to secure, the following steps are required:

- Set the security level of CAN-FD to secure-user (0x2) or secure privilege (0x3) in SEC\_AHB->MASTER\_SEC\_LEVEL register.
- Assign secure-user or secure-privilege level for CAN-FD register space in SEC\_AHB->SEC\_CTRL\_AHB\_PORT8\_SLAVE1 Register.
- Assign secure-user or secure-privilege level for message RAM.

**Example:**

If 16KB of SRAM 2 (0x2000\_C000) bank is used for CAN message RAM. Then set rules in SEC\_AHB-> SEC\_CTRL\_RAM2\_MEM\_RULE0 register to secure-user (0x2) or secure privilege (0x3).

**Problem**

The shared memory used by the CAN-FD controller and CPU should be accessible using secure alias with address bit 28 set (example 0x3000\_C000). However, when CAN-FD makes a bus transaction using secure alias (address bit 28 set), the transaction is aborted.

**Workaround**

- When CPU is accessing the CAN-FD register or message RAM it should always use secure alias i.e., 0x3000\_C000 for message RAM manipulation. .
- For any structure the CAN-FD peripheral uses to fetch or write, memory should be set to use 0x2000\_C000 in order for bus transactions to work. CAN-FD software driver should set “Message RAM base address register (MRBA, offset 0x200)” with the physical address of RAM instead of secure alias.

**AC/DC deviations detail**

No known errata.

**Errata notes detail**

No known errata.

**Limited warranty and liability**

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by the customer’s technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [nxp.com/SalesTermsandConditions](http://nxp.com/SalesTermsandConditions).

**Right to make changes**

NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Security**


The customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. The customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customers’ applications and products. The customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in

customers' applications. NXP accepts no liability for any vulnerability. Customers should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security-related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at [PSIRT@nxp.com](mailto:PSIRT@nxp.com)) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.







NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREEN CHIP, HITAG, ICODE, JCOP, LIFE, VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROAD LINK, SMARTLX, SMART MX, STARPLUG, TOP FET, TRENCHMOS, UCODE, Freescale, the Freescale logo, Altivec, CodeWarrior, ColdFire, ColdFire+, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, Tower, TurboLink, EdgeScale, EdgeLock, eIQ, and Immersive3D are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro,  $\mu$ Vision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. M, M Mobileye and other Mobileye trademarks or logos appearing herein are trademarks of Mobileye Vision Technologies Ltd. in the United States, the EU and/or other jurisdictions.

© NXP B.V. 2020-2021. For more information, please visit: <http://www.nxp.com>. For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com).

## Documents / Resources

	<a href="#">NXP LPC55S0x M33 Based MicroController</a> [pdf] User Manual LPC55S0x, M33 Based MicroController, Based MicroController, LPC55S0x, MicroController
---	---

## References

-  [NXP® Semiconductors Official Site | NXP Semiconductors](#)
-  [Our Terms And Conditions Of Commercial Sale | NXP Semiconductors](#)
-  [Support | NXP Semiconductors](#)
- [S Domain Registered at Safenames](#)
-  [NXP® Semiconductors Official Site | NXP Semiconductors](#)
-  [Our Terms And Conditions Of Commercial Sale | NXP Semiconductors](#)
-  [Support | NXP Semiconductors](#)