

# NXP IMXQSUG Config Tools for i.MX User Guide

Home » NXP » NXP IMXQSUG Config Tools for i.MX User Guide



#### **Contents**

- 1 NXP IMXQSUG Config Tools for
- i.MX
- 2 Introduction
- 3 Start with a new configuration
- 4 Import an existing configuration
- **5 Pins Tool**
- **6 DDR Tool**
- 7 Generate code
- 8 Revision history
- 9 Documents / Resources
  - 9.1 References
- **10 Related Posts**



# **NXP IMXQSUG Config Tools for i.MX**

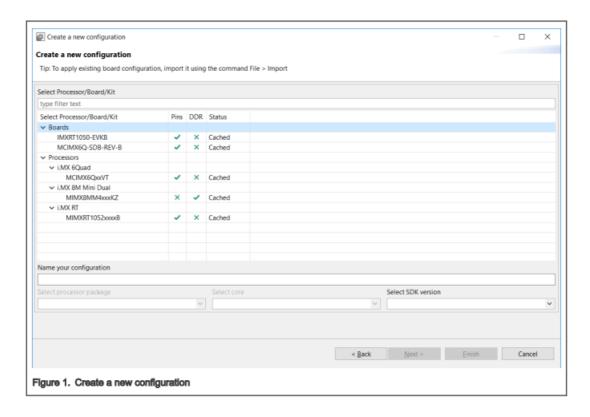
NXP IMXQSUG Config Tools for i.MX-fig1

#### Introduction

- Config Tools for i.MX is a suite of tools intended for configuration of NXP i.MX Cortex-A and Cortex-M based processors.
- Use the Pins tool to customize pin routing configuration of the device, including configuration of electrical properties related to all respective pin signals, and to create source codes applicable for a device initialization either as direct initialization of register(s) or code for SDK API and/or device tree code snippet(if supported).
- Use the DDR tool to configure and validate the double data rate RAM configuration.

# Start with a new configuration

On starting Config Tools for i.MX the first time you will be greeted by the Start Development window. You can use this window to create a new configuration or load an existing one.



#### To create a new configuration for selected processor, board or kit at any time, do the following:

- 1. Start the tool or select File > New.
- 2. Select option Create new configuration for processor, board or kit.
- 3. Select Next.
- 4. Expand the tree and select any processor, board or kit configuration. You can also use the filter field to quickly find desired item.
- Customize name of the configuration and select Finish.
   Use File > Save to save existing configuration to the disk.

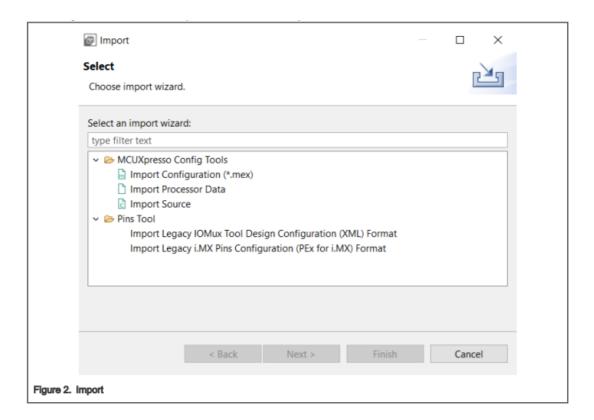
# Import an existing configuration

You can also import an existing configuration using a built-in import wizard for getting pins and DDR configuration either from legacy project formats (IO Mux Tool Design Configuration XML or PEx for i.MX) or an other already existing configuration file (MEX) or Pins tool-generated source files containing YAML configuration details.

# To import an existing configuration:

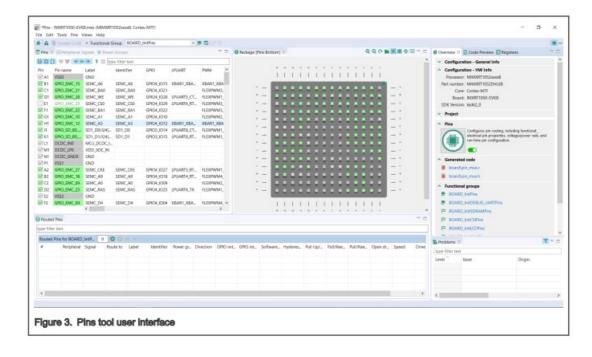
- 1. Select File > Import.
- 2. Choose the import wizard, select Next and follow the instructions.
- 3. Select Browse and then the required input file(s).
- 4. Select Finish to import files.

New configuration is created if the import is finished successfully, then use File > Save to save it to the disk.

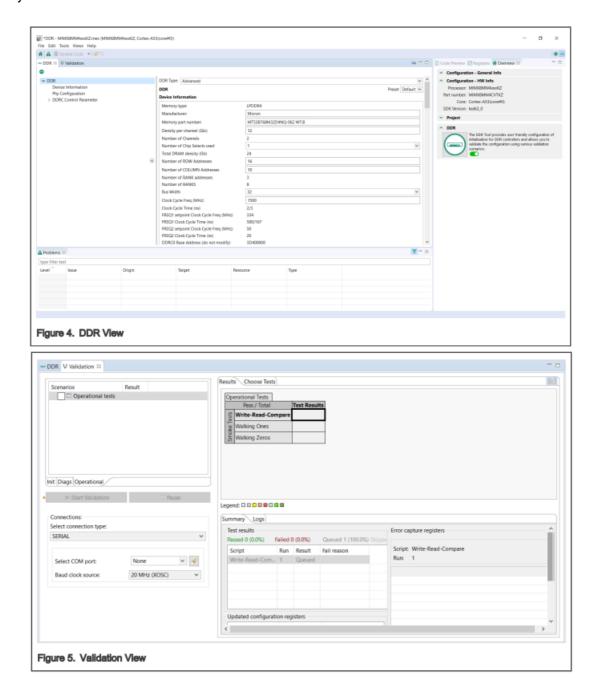


# **Pins Tool**

- In the Pins tool, you can display and configure the pins of selected processor. Basic configuration can be done in the Pins, Peripheral Signals or Package views.
- More advanced settings (pin electrical properties and features) can be viewed and configured in the Routed Pins view.
- Moreover, Config Tools for i.MX allows you to verify possible voltage level issues on HW level within given functional group for pins configuration from different power rails (if specified for given processor). Individual voltage level for supported power groups can be configured globally per current configuration in Power Groups view.



- In the DDR view you can view and configure basic DDR attributes, such as memory type, frequency, number of channels and others.
- In the Validation view, you can submit the DDR configuration to a variety of tests. After you've specified the connection type, you can choose scenarios, tests to run in these scenarios, and view the test results, logs, and summary.



#### Generate code

Pins tool generates the output code for current configuration automatically. You can also select Pins. Refresh from the Main Menu to update the code manually. All output code files are displayed in the Code Preview view. To copy the code, perform the copy/paste operation or click the Export icon in the right up corner of Code Preview view.

```
A Overview Code Preview Registers
                   pin_mux.c pin_mux.h
                     2 * This file was generated by the MCUXpresso C
                     3 * will be overwritten if the respective MCUXp
                     6/3
                     7 * TEXT BELOW IS USED AS SETTING FOR TOOLS ***
                     8!!GlobalInfo
                     9 product: Pins v7.0
                    10 processor: MIMXRT1052xxxxB
                    11 package_id: MIMXRT1052DVL6B
                    12 mcu_data: ksdk2_0
                    13 processor_version: 0.0.1
                    14 board: IMXRT1050-EVKB
                    15 * BE CAREFUL MODIFYING THIS COMMENT - IT IS Y
                    16 */
                    18 #include "fsl_common.h"
                    19 #include "fsl_iomuxc.h"
                    20 #include "pin_mux.h"
                    22 /* FUNCTION ********************
                    23
                    24 * Function Name : BOARD_InitBootPins
                    25 * Description : Calls initialization functi
                    26 *
                    27 * END ***********************
                    28 void BOARD_InitBootPins(void) {
                    29 BOARD_InitPins();
                          BOARD_InitDEBUG_UARTPins();
                     <
Figure 6. Generate code
```

Alternatively, you can also export generated output in various types of output like source files, plain pins configuration data in CSV, modified registers content or as pins configuration report in HTML format per specific export wizard selectable from File > Export from the Main Menu.

#### **Revision history**

Table 1. Revision history

Revision number	Date	Substantive changes
0	23 June 2021	Initial release
1	22 December 2021	Minor updates

• How To Reach Us Home Page:

#### nxp.com

• Web Support:

#### nxp.com/support

- Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.
- NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any

particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

- While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.
- NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX,
   EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC,
   MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE,
   MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE,
   Freescale, the Freescale logo, AltiVec, C-5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C-Ware, the
   Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor
   Expert, QorlQ, QorlQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony,
   VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine,
   SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service
   names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan,
   big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed
   Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME,
   ULINK-PLUS, ULINKpro, μVision,
- Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© NXP B.V. 2017-2021.

For more information, please visit: <a href="http://www.nxp.com">http://www.nxp.com</a>

For sales office addresses, please send an email to: <a href="mailto:salesaddresses@nxp.com">salesaddresses@nxp.com</a>

Date of release: 22 December 2021 Document identifier: IMXQSUG

**Documents / Resources** 



# NXP IMXQSUG Config Tools for i.MX [pdf] User Guide IMXQSUG, Config Tools for i.MX, IMXQSUG Config Tools for i.MX

NP

# References

- NXP® Semiconductors Official Site | NXP Semiconductors
- Our Terms And Conditions Of Commercial Sale | NXP Semiconductors
- Support | NXP Semiconductors
- S Domain Registered at Safenames
- NXP® Semiconductors Official Site | NXP Semiconductors
- Our Terms And Conditions Of Commercial Sale | NXP Semiconductors
- Support | NXP Semiconductors

Manuals+,