

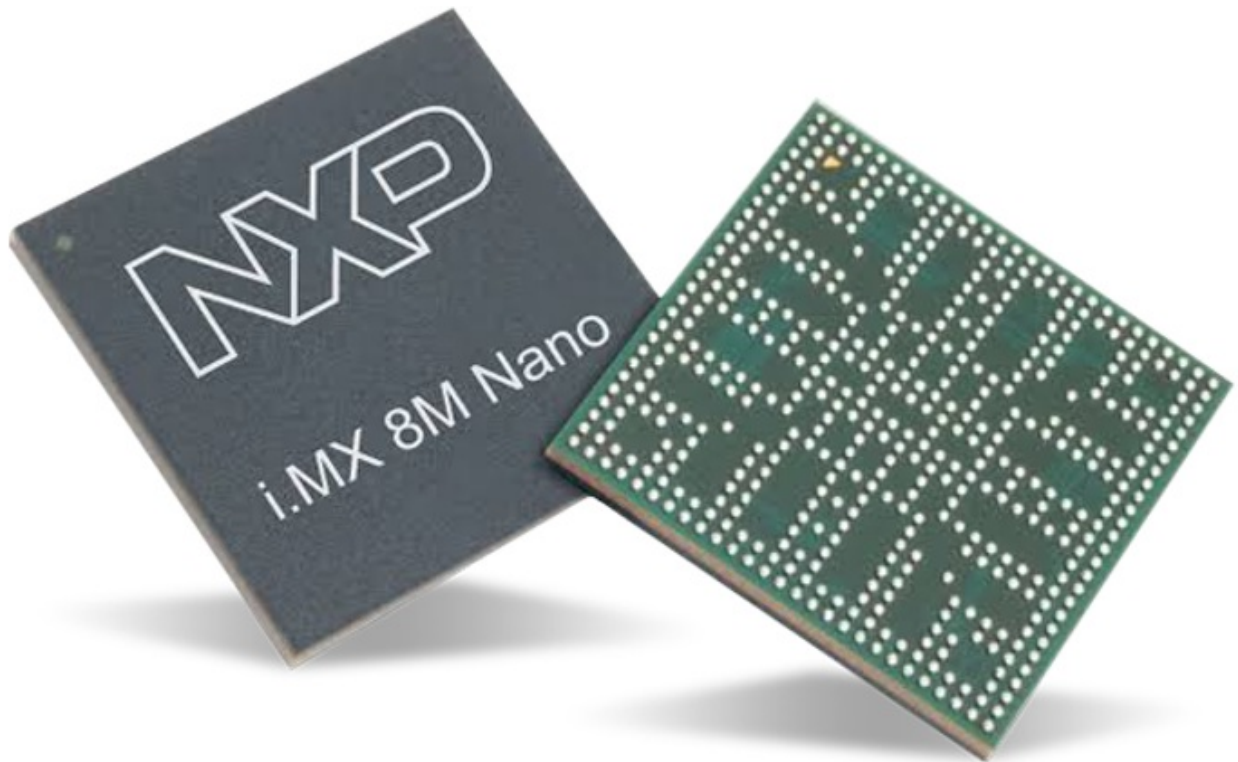


NXP i.MX 8M Mini Applications Processor Instruction Manual

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**i.MX 8M Mini Applications Processor
Instruction Manual**



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i.MX 8M Mini Applications Processor

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Chapter 1 Introduction

1.1 Product Overview

This chapter introduces the architecture of the i.MX 8M Mini Applications Processor. The i.MX 8M Mini is a family of products focused on delivering an excellent video and audio experience, combining media-specific features with high-performance processing optimized for low power consumption.

1.2 Target Applications

The i.MX 8M Mini Media Applications Processor is built to achieve both high performance and low power consumption and relies on a powerful fully coherent core complex based on a quad Cortex-A53 cluster with video and graphics accelerators. The i.MX 8M Family provides additional computing resources and peripherals:

- Advanced security modules for secure boot, cipher acceleration, and DRM support
- General purpose Cortex-M4 processor for low power processing
- A wide range of audio interfaces including I2S, AC97, TDM, and S/PDIF
- A large set of peripherals that are commonly used in consumer/industrial markets including USB 2.0, PCIe, and Ethernet

1.3 Acronyms and Abbreviations

The table below contains acronyms and abbreviations used in this document.

Acronyms and Abbreviated Terms

Acronyms and Abbreviations

Term	Meaning
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AIPS	Arm IP Bus
ALU	Arithmetic Logic Unit
AMBA	Advanced Microcontroller Bus Architecture

APB	Advanced Peripheral Bus
ASRC	Asynchronous Sample Rate Converter
AXI	Advanced eXtensible Interface
BIST	Built-In Self Test
CA/CM	Arm Cortex-A/Cortex-M
CAAM	Cryptographic Acceleration and Assurance Module
CA53	ARM Cortex A53 Core
CAN	Controller Area Network
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
CSU	Central Security Unit
CTI	Cross Trigger Interface
D-cache	Data cache
DAP	Debug Access Port
DDR	Double data rate
DMA	Direct memory access
DPLL	Digital phase-locked loop
DRAM	Dynamic random access memory
ECC	Error correcting codes
CSPI	Enhanced Configurable SPI
LIPPI	Low-power SPI
EDMA	Enhanced Direct Memory Access
AIM	External Interface Module
ENET	Ethernet
EDIT	Enhanced Periodic Interrupt Timer
EPROM	Erasable Programmable Read-Only Memory
ETF	Embedded Trace FIFO
ITEM	Embedded Trace Macrocell
FIFO	First-In-First-Out

GO	General Interrupt Controller
GPC	General Power Controller
GPIO	General-Purpose I/O
GPU	General-Purpose Register
GPS	Global Positioning System
GPT	General-Purpose Timer
GPU	Graphics Processing Unit

Chapter 1 Introduction

Term	Meaning
GPV	Global Programmers View
HAB	High-Assurance Boot
I-cache	Instruction cache
I2C or I2 C	Inter-Integrated Circuit
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
COMIX	Input-Output Multiplexer
IP	Intellectual Property
IrDA	Infrared Data Association
JTAG	Joint Test Action Group (a serial bus protocol usually used for test purposes)
ELCDIF	Liquid Crystal Display Interface
LDO	Low-Dropout
LIFO	Last-In-First-Out
LRU	Least-Recently Used
LSB	Least-Significant Byte
LUT	Look-Up Table
LVDS	Low Voltage Differential Signaling
MAC	Medium Access Control
MCM	Miscellaneous Control Module
MMC	Multimedia Card
MSB	Most-Significant Byte

MT/s	Mega Transfers per second
OCRAM	On-Chip Random-Access Memory
OCTOPUS	On-Chip One-Time Programmable Controller
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCMCIA	Personal Computer Memory Card International Association
PGC	Power Gating Controller
PIC	Programmable Interrupt Controller
PMU	Power Management Unit
POR	Power-On Reset
PSRAM	Pseudo-Static Random Access Memory
PWM	Pulse Width Modulation
PXP	Pixel Pipeline
QoS	Quality of Service
R2D	Radians to Degrees
RISC	Reduced Instruction Set Computing
ROM	Read-Only Memory
ROMCP	ROM Controller with Patch
RTOS	Real-Time Operating System
Rx	Receive

Features

Term	Meaning
SAI	Synchronous Audio Interface
SKU	Snoop Control Unit
SD	Secure Digital
STUDIO	Secure Digital Input/Output
SDLC	Synchronous Data Link Control
CDMA	Smart DMA
SIM	Subscriber Identification Module
SNVS	Secure Non-Volatile Storage
SoC	System-on-Chip
SPBA	Shared Peripheral Bus Arbiter
SPDIF	Sony Phillips Digital Interface
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SRC	System Reset Controller
TFT	Thin-Film Transistor
TOPIC	Trace Port Interface Unit
TIGER	Time Stamp Generator
Tx	Transmit
TASK	TrustZone Address Space Controller
CART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USDHC	Ultra Secure Digital Host Controller
WDOG	Watchdog
WLAN	Wireless Local Area Network
WXGA	Wide Extended Graphics Array

1.4 Features

1.4.1 Arm Cortex-A53 MPCore™ Platform

The i.MX 8M Family Applications Processors are based on the Arm Cortex-A53 MPCore™ Platform, which has the following features:

- Quad symmetric Cortex-A53 processors, including
- 32 KB L1 Instruction Cache
- 32 KB L1 Data Cache

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i.MX 8M Plus Applications Processor Reference Manual, Rev. 1, 06/2021
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