NXP Semiconductors FRDM-K66F Development Platform User Guide

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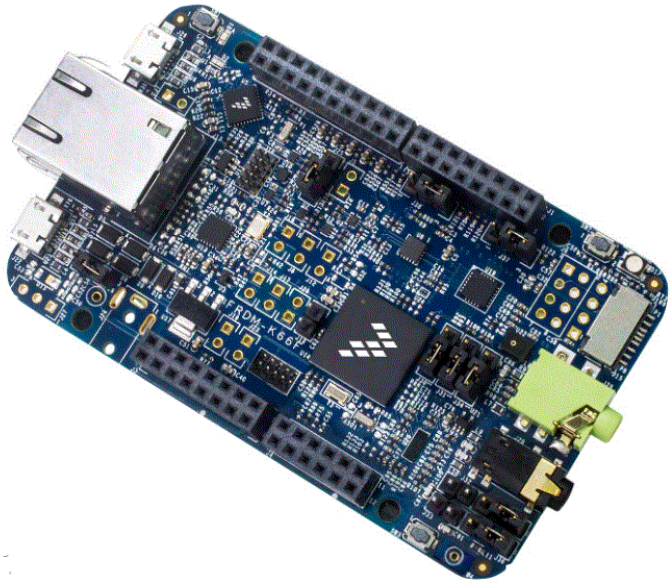

Introduction

The NXP Freedom development platform is a set of software and hardware tools for evaluation and development. It is ideal for rapid prototyping of microcontroller-based applications. The NXP Freedom K66F hardware, FRDM-K66F, is a simple, yet sophisticated design featuring a Kinetis K series microcontroller, built on the ARM© Cortex®-M4 core.
FRDM-K66F can be used to evaluate the K66 and K26 Kinetis K series devices. It features an MK66FN2M0VMD18, which boast a maximum operation frequency of 180MHz, 2MB of flash, 256KB RAM, a high-speed USB controller, an Ethernet controller, Secure Digital Host controller, and loads of analog and digital peripherals.

The FRDM-K66F hardware is form-factor compatible with the ArduinoTM R3 pin layout, providing a broad range of expansion board options. The onboard interface includes a digital accelerometer & magnetometer, gyroscope, audio codec, digital MEMS mic, tricolor LED, SDHC, Bluetooth Add-on module, RF Add-on module (for use over SPI), and Ethernet.
The FRDM-K66F platform features OpenSDAv2.1, the NXP open source hardware embedded serial and debug adapter running an open-source bootloader. This circuit offers several options for serial communication, flash programming and run-control debugging. The openSDAv2.1 is loaded with JLink firmware for rapid prototyping and product development, with a focus on connected Internet of Things devices.

FRDM-K66F Hardware Overview

The features of the FRDM-K66F hardware are as follows:

- MK66FN2M0VMD18 MCU (180 MHz, 2MB Flash, 256KB RAM, 144MBGA package)
- Dual role High-speed USB interface with micro-B USB connector
- RGB LED
- FXOS8700CQ – Accelerometer and Magnetometer
- FXAS21002 – Gyroscope
- Two user push buttons
- Flexible power supply options – OpenSDAv2.1 USB, K66F USB, and external sources
- Easy access to MCU I/O via Arduino R3TM compatible I/O connectors

- Programmable OpenSDAv2.1 debug interface with multiple applications available including:
  - SWD debug interface over a USB HID connection providing run-control debugging and compatibility with IDE tools
  - Virtual serial port interface
- Ethernet
- Micro SD
- Audio features
  - Digital MEMS microphone
  - Auxiliary input jack
  - Headset/Analog microphone jack
  - Two optional input for analog microphone
- Optional header for add-on RF module: RF24L01+ Nordic 2.4 GHz Radio
- Optional header for add-on Bluetooth module: JY-MCU BT Board V1.05 BT

  Figure 1 shows a block diagram of the FRDM-K66F design. Figure 2 explains the primary components and their placement on the hardware assembly.

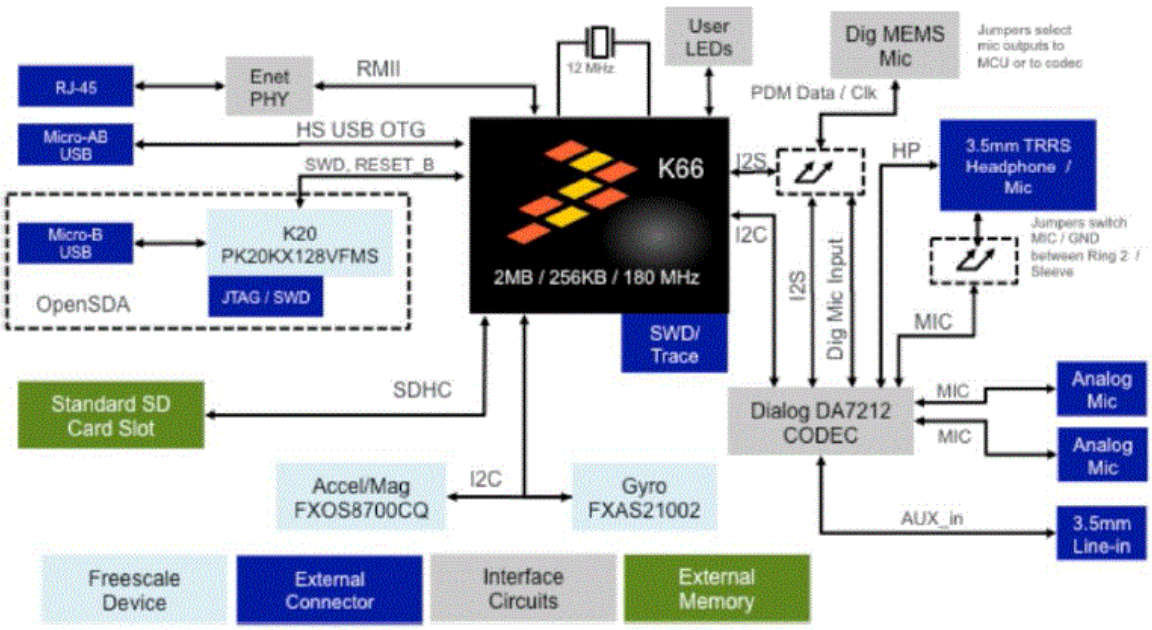

Figure 1. FRDM-K66F block diagram

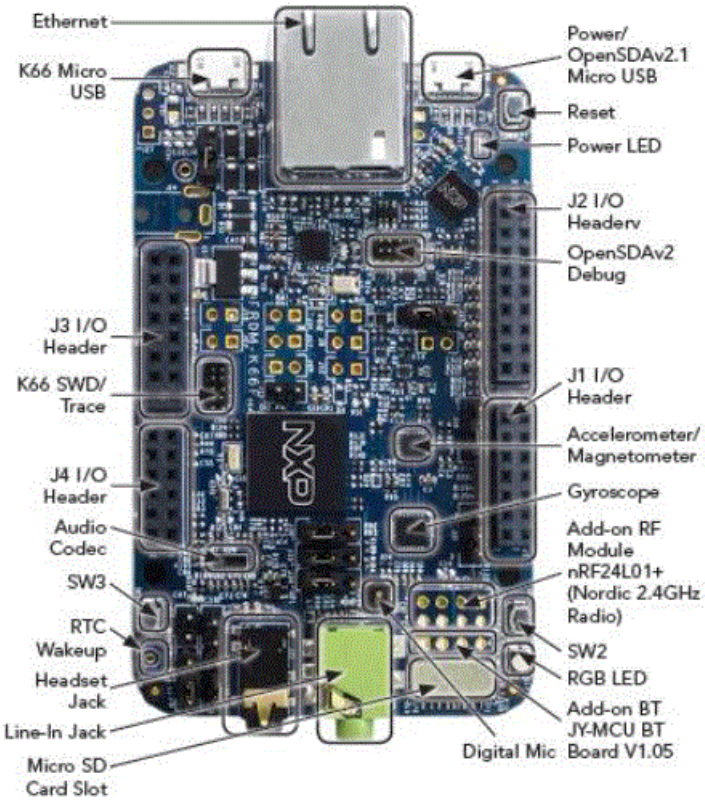

Figure 2. FRDM-K66F main components placement

FRDM-K66F Hardware Description

Power supply

There are multiple power supply options on the FRDM-K66F. It can be powered from either of the USB connectors, the VIN pin on the J3 I/O header, DC Jack (Not populated), or an off-board 1.71-3.6 V supply from the 3.3 V pin on the J20 header. The USB, DC Jack, and VIN supplies are regulated onboard using a 3.3 V linear regulator to produce the main power supply. The 3.3 V Header (J20) is not regulated onboard. Table 1 provides the operational details and requirements for the power supplies.

Supply Source	Valid Range	OpenSDAv2.1 Operational?	Regulated onboard?
OpenSDAv2.1 USB	5V	Yes	Yes
K66F USB	5V	No	Yes
VIN Pin	5V – 9V	No	Yes
3.3V Header (J20)	1.71 – 3.6V	No	No
DC Jack (Not Populated)	5V	No	No

NOTE

The OpenSDAv2.1 circuit is only operational when a USB cable is connected and supplying power to OpenSDAv2.1 USB. However, protection circuitry is in place to allow multiple sources to be powered at once.

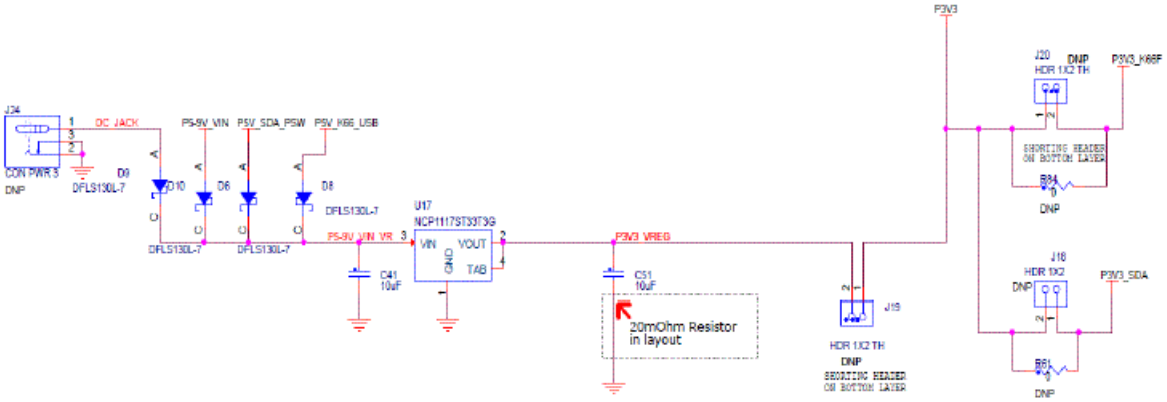

Figure 3. Power supply schematic

Table 2. FRDM-K66F power supplies

Power supply name	Description
P5-9V_VIN	Power supplied from the **VIN pin of the I/O headers** (J3 pin 16). A Schottky diode provides back drive protection *1*.
P5V_SDA_PSW	Power supplied from the **OpenSDA USB** connector. A Schottky diode provides back drive protection
P5V_K66_USB	Power supplied from the **K66F USB** connector. A Schottky diode provides back drive protection
DC_JACK	Power supplied from the **DC Jack** (Not populated) connector. A Schottky diode provides back drive protection. (Note: Must use 5V supply)
P3V3_VREG	**Regulated 3.3V supply**. Sources power to the P3V3 supply rail through a back drive protection Schottky diode *2*.
P3V3_K66	**K66F MCU supply**. Header J20 provides a convenient means for energy consumption measurements *3*.
P3V3_SDA	**OpenSDA circuit supply**. Header J18 provides a convenient means for energy consumption measurements *2*.
P5V_USB	Nominal **5V supplied to the I/O headers** (J3 pin 10)

1. A 5 VDC regulator is required at J27 when USB Host mode is used. The USB host mode requires a 5 V supply

to USB device.

2. By default the linear regulator, U17, is a 3.3 V output regulator. This is a common footprint that would allow the user to modify the assembly to utilize an alternative device such as 1.8V. The K66F microcontroller has an operating range of 1.71 V to 3.6 V.
3. J18 and J20 are not populated by default. P3V3_K66 rail is connected by shorting trace at bottom layer of J20. To measure the energy consumption of the K66F MCU, the trace between J20 pins 1 and 2 must first be cut. A current probe or shunt resistor and voltage meter can then be applied to measure the energy consumption on these rails.

Series and debug adapter (OpenSDAv2.1)

OpenSDAv2.1 is a serial and debug adapter circuit that includes an open-source hardware design, and open-source bootloader, and debug interface software. It bridges serial and debug communications between a USB host and an embedded target processor as shown in Figure 4. The hardware circuit is based on a NXP Kinetis K20 family microcontroller (MCU) with 128 KB of embedded flash and an integrated USB controller. OpenSDAv2.1 comes preloaded with the CMSIS-DAP bootloader—an open-source mass storage device (MSD) bootloader, and the JLink interface firmware, which provides a virtual serial port interface, and a JLink debug protocol interface. For more information on the OpenSDAv2.1 software, see mbed.org and **https://github.com/mbedmicro/CMSIS-DAP** and **http://www.segger.com/opensda.html**.

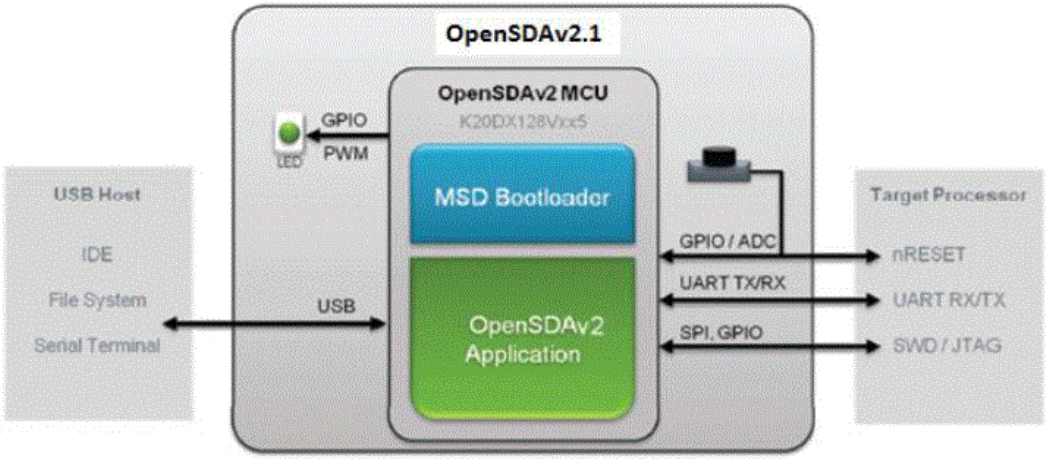

Figure 4. OpenSDA high-level block diagram

OpenSDAv2.1 is managed by a Kinetis K20 MCU built on the ARM® Cortex™-M4 core. The OpenSDA circuit includes a status LED (D2) and a pushbutton (SW1). The pushbutton asserts the Reset signal to the K66F target MCU. It can also be used to place the OpenSDAv2.1 into Bootloader mode. SPI and GPIO signals provide an interface to either the SWD debug port of the K20. Additionally, signal connections are available to implement a UART serial channel. The OpenSDA circuit receives power when the USB connector J26 is plugged into a USB host.

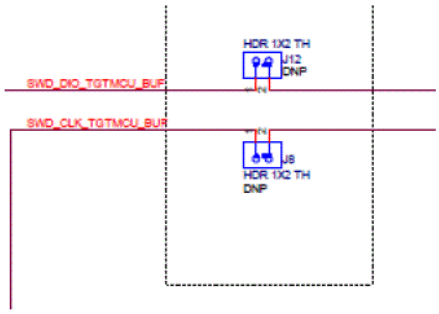

Figure 5. SWD signals isolation

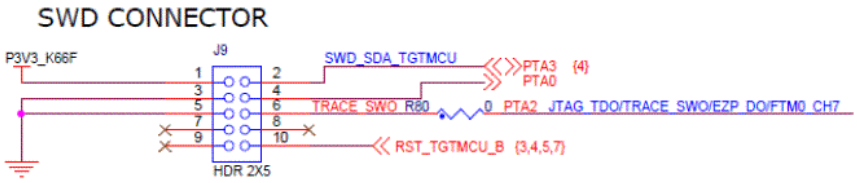

Figure 6. SWD connector

J9 is populated by default. A mating cable, such as a Samtec FFSD IDC cable, can then be used to connect from the OpenSDAv2.1 of the FRDM-K66F to an off-board SWD connector.

Virtual Serial Port
A serial port connection is available between the OpenSDAv2.1 MCU and pins PTB16 and PTB17 of the K66F.

Microcontroller

The FRDM-K66F features the MK66FN2M0VMD18 MCU. This 180 MHz microcontroller is part of the Kinetis K6x family and is implemented in a 144 MBGA package. The following table notes some of the features of the MK66FN2M0VMD18 MCU.

Feature	Description
Ultra low power	• 11 low-power modes with power and clock gating for optimal peripheral activity and rec overy times • Full memory and analog operation down to 1.71V for extended battery life • Low-leakage wake-up unit with up to six internal modules and sixteen pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLSx) modes • Low-power timer for continual system operation in reduced power states

Table 3. Features of MK66FN2M0VMD18

Feature	Description

Flash and SRAM	• 2048-KB flash featuring fast access times, high reliability, and four levels of security protection • 256 KB of SRAM • No user or system intervention to complete programming and erase functions and full operation down to 1.71 V • Flash access control
Mixed-signal capability	• High-speed 16-bit ADC with configurable resolution • Single or differential output modes for improved noise rejection • 500-ns conversion time achievable with programmable delay block triggering • Three high-speed comparators providing fast and accurate motor overcurrent • protection by driving PWMs to a safe state • Optional analog voltage reference provides an accurate reference to analog blocks • Two 12-bit DACs
Performance	• 180-MHz ARM Cortex-M4 core with DSP instruction set, single cycle MAC, and single instruction multiple data (SIMD) extensions • Up to 32 channels DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput • Cross bar switch enables concurrent multi-master bus accesses, increasing bus bandwidth • Independent flash banks allowing concurrent code execution and firmware updating with no performance degradation or complex coding routines
Timing and Control	• Four Flex Timers with a total of 20 channels • Hardware dead-time insertion and quadrature decoding for motor control • Carrier modulator timer for infrared waveform generation in remote control applications • Four-channel 32-bit periodic interrupt timer provides time base for RTOS task scheduler or trigger source for ADC conversion and programmable delay block • One Low power Timer • One independent real time clock

Connectivity and Communications	• High-Speed USB Device/Host • Full-Speed USB Device/Host/On-The-Go with device charge detect capability • Optimized charging current/time for portable USB devices, enabling longer battery life • USB low-voltage regulator supplies up to 120 mA off chip at 3.3 volts to power external components from 5-volt input • Five UARTs: — One UART supports RS232 with flow control, RS485, and ISO7816 — Four UARTs support RS232 with flow control and RS485 • One low-power UART (LPUART) • One Inter-IC Sound (I2S) serial interface for audio system interfacing

Feature	**Description**
	• Three DSPI modules and three I2C modules • Secured digital host controller (SDHC) • One FlexCAN module • One Ethernet module with 1588 • A multi-function external bus interface (FlexBUS) controller capable of interfacing to slave- only devices.
Reliability, Safety and Security	• Hardware Encryption co-processor for secure data transfer and storage. Faster than software implementations and with minimal CPU loading. Supports a wide variety of algorithms - DES, 3DES, AES, MD5, SHA-1, SHA-256 • System security and tamper detection with secure real-time clock (RTC) and independent battery supply. Secure key storage with internal/external tamper detection for unsecured flash, temperature, clock, and supply voltage variations and physical attack detection • Memory protection unit provides memory protection for all masters on the cross bar switch, increasing software reliability • Cyclic redundancy check (CRC) engine validates memory contents and communication data, increasing system reliability • Independently-clocked COP guards against clock skew or code runaway for fail-safe applications such as the IEC 60730 safety standard for household appliances • External watchdog monitor drives output pin to safe state for external components in the event that a watchdog timeout occurs • Included in NXP’s product longevity program, with assured supply for a minimum of 10 years after launch

Clocking

WARNING
The resonator is NOT recommended when HS USB is used.

The Kinetis MCUs start up from an internal digitally-controlled oscillator (DCO). Software can enable the main external oscillator (EXTAL0/XTAL0) if desired. The external oscillator/resonator can range from 32.768 KHz up to a 50 MHz. The default external source for the MCG input is a 12 MHz crystal. The 12 MHz reference clock is suitable for both audio codec and HS USB features.

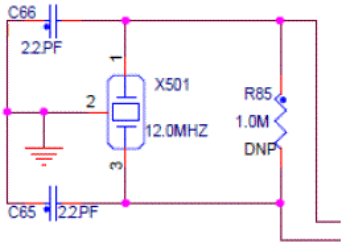

Figure 7. 12 MHz crystal clock source for MCU

By default, the 32.768 KHz crystal is connected to the RTC oscillator inputs.

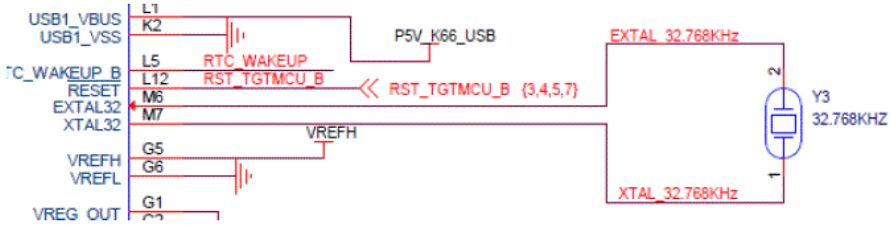

Figure 8. 32.768 KHz crystal for RTC

Universal Serial Bus (USB)

The MK66FN2M0VMD18 features an HS USB with Host/Device capability and a built-in transceiver. The FRDM-K66F routes the USB1 D+ and D- signals from the MK66FN2M0VMD18 MCU directly to the onboard micro USB connector (J22).

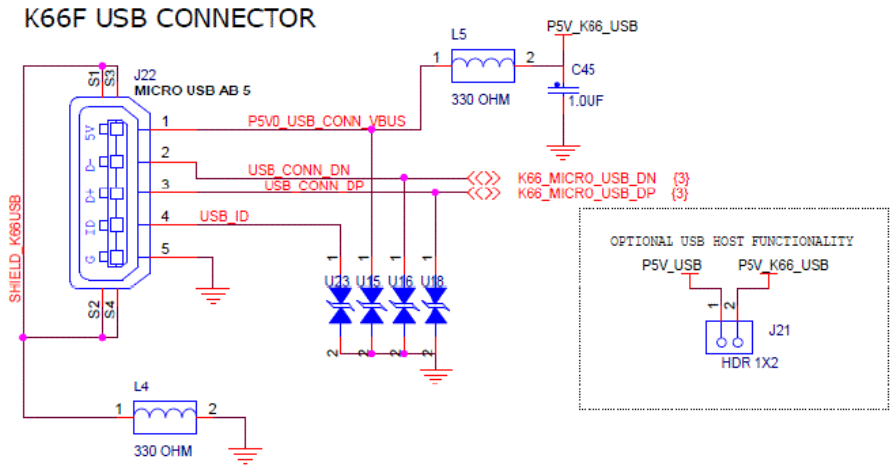

Figure 9. K66F USB port

When the FRDM-K66F is operating in USB Host mode, a 5 V power must be supplied to VBUS of J22 and J21 must be shunt. The 5 V power can be sourced from either OpenSDAv2.1 USB port (J26), pin 10 of J3 I/O header, 5V DC_Jack, and P5-9V_VIN DC-DC converter of J27.

NOTE
DC_Jack (J24) and 5 V regulator (J27) are not populated by default. J200 and J201 are not populated by default.

Power source	Voltage	J202	J200	J201
OpenSDAv2.1 USB Port (J26)	5V	Shunt	Off	Off
DC_Jack (5V only)	5V	Off	Shunt	Off
P5-9V_VIN	9V	Off	Off	Shunt

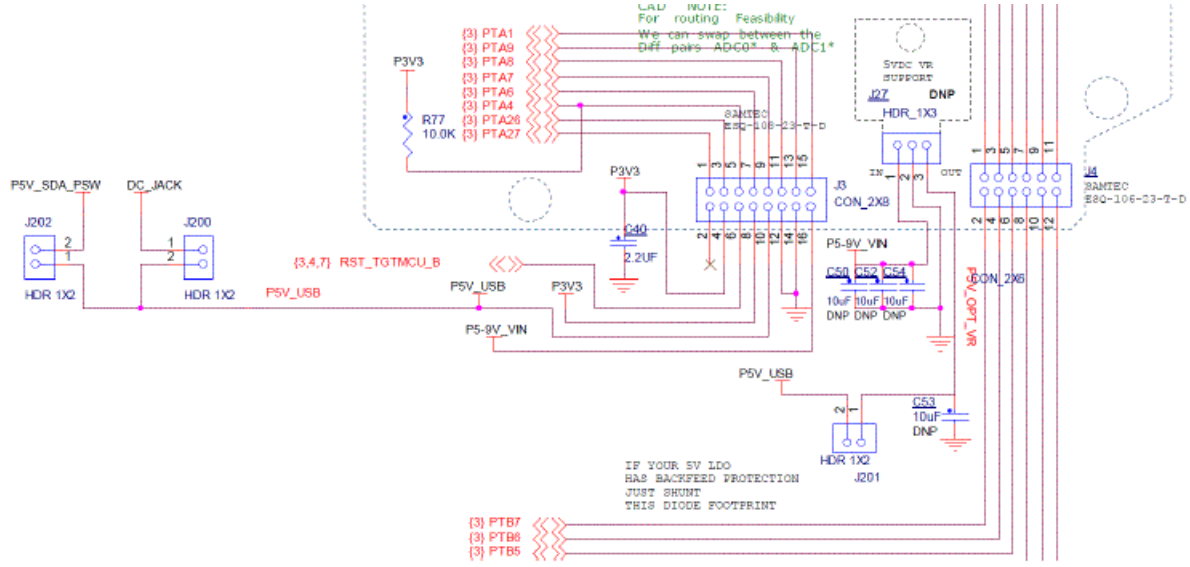

Figure 10. K66F USB power input for host mode

Secure Digital Card

A micro Secure Digital (SD) card slot is available on the FRDM-K66F connected to the SD Host Controller (SDHC) signals of the MCU. This slot will accept micro format SD memory cards. The SD card detect pin is an open switch that shorts with VDD when card is inserted. Table 5 shows the SDHC signal connection details.

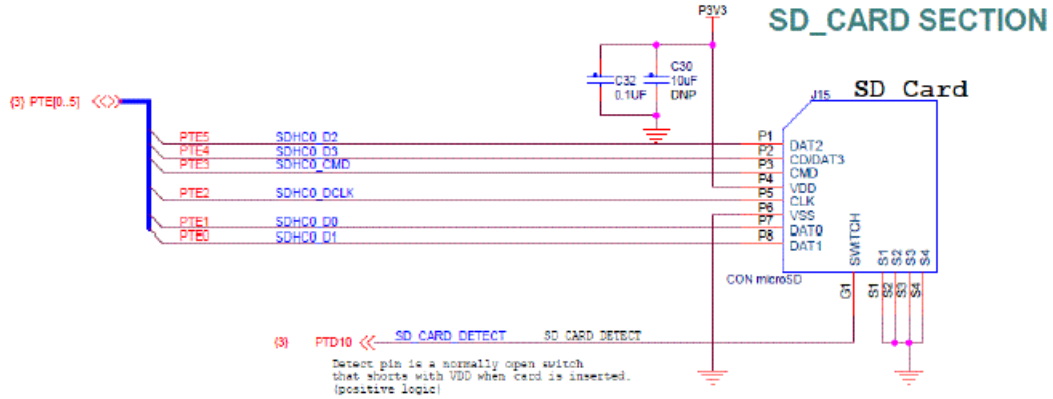

Figure 11. Micro SD interface

Table 5. Micro SD card socket connection

Pin	Function	FRDM-K66F connection
1	DAT2	PTE5/SPI1_PCS2/UART3_RX/**SDHC0_D2**/FTM3_CH0
2	CD/DAT3	PTE4/LLWU_P2/SPI1_PCS0/UART3_TX/**SDHC0_D3**/TRACE_D0
3	CMD	PTE3/ADC1_SE7A/SPI1_SIN/UART1_RTS/**SDHC0_CMD**/TRACE_D1/SPI1_SOUT
4	VDD	3.3 V Board supply (V_BRD)
5	CLK	PTE2/LLWU_P1/ADC1_SE6A/SPI1_SCK/UART1_CTS/**SDHC0_DCLK**/TRACE_D2
6	VSS	Ground
7	DAT0	PTE1/LLWU_P0/ADC1_SE5A/SPI1_SOUT/UART1_RX/**SDHC0_D0**/TRACE_D3/I2C1_SCL/SPI 1_SIN
8	DAT1	PTE0/ADC1_SE4A/SPI1_PCS1/UART1_TX/**SDHC0_D1**/TRACE_CLKOUT/I2C1_SDA/RTC_CL KOUT
G1	SWITCH	**PTD10**/LPUART0_RTS/FB_A18
S1-S4	S1, S2, S3, S4	Shield Ground

Ethernet

The MK66FN2M0VMD18 features a 10/100 Mbps Ethernet MAC with MII and RMII interfaces. The FRDM-K66F routes RMII interface signals from the K66F MCU to onboard Micrel 32-pin Ethernet PHY.
When the K66F Ethernet MAC is operating in RMII mode, synchronization of the MCU clock and the 50 MHz RMII transfer clock is important. The MCU input clock must be kept in phase with external PHY. The 32-pin Micrel Ethernet PHY has the ability to provide 50 MHz clock to MK66FN2M0VMD18 MCU PTE26 (ENET_1588_CLKIN) and Ethernet PHY itself.

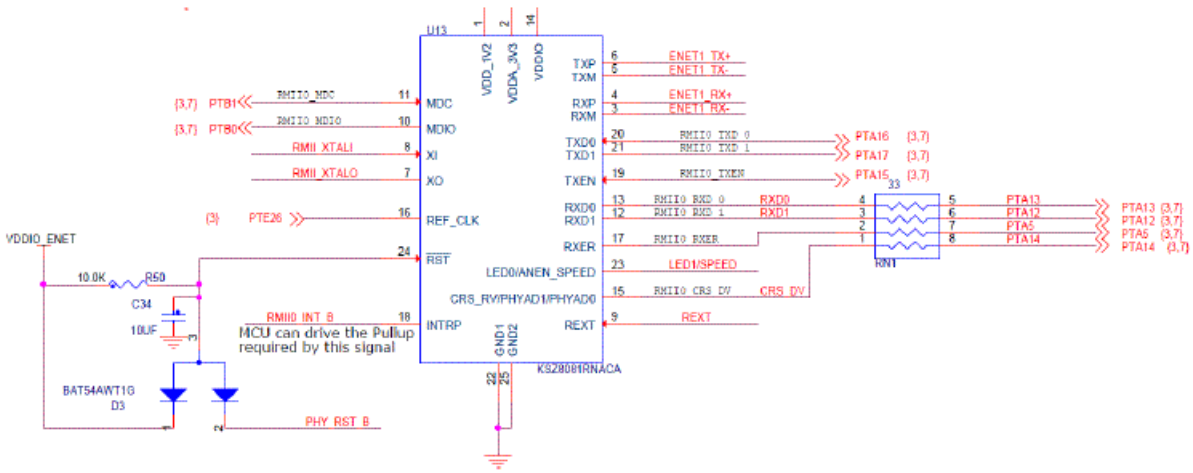

Figure 12. RMII to Ethernet PHY

There is no external pull up on MDIO signal when MK66FN2M0VMD18 is requesting status of the Ethernet link connection. Internal pull is required when enabled in port configuration for MDIO signal.

Accelerometer and Magnetometer

An NXP FXOS8700CQ low-power, 6-axis Xtrinsic sensor combines 14-bit accelerometer and 16-bit magnetometer sensors is interfaced through an I2C bus and two GPIO signals, as shown in Table 6 below. By default, the I2C address is 0x1D (SA0 pulled high and SA1 pulled low).

FXOS8700CQ	K66F Connection
SCL	PTD8/LLWU_P24/**I2C0_SCL**/LPUART0_RX/FB_A16
SDA	PTD9/**I2C0_SDA**/LPUART0_TX/FB_A17
INT1	**PTC17**/CAN1_TX/UART3_TX/ENET0_1588_TMR1/FB_CS4/FB_TSIZ0/FB_BE31_24_BLS7_0/SDRAM _DQM3
INT2	**PTC13**/UART4_CTS/FTM_CLKIN1/FB_AD26/SDRAM_D26/TPM_CLKIN1

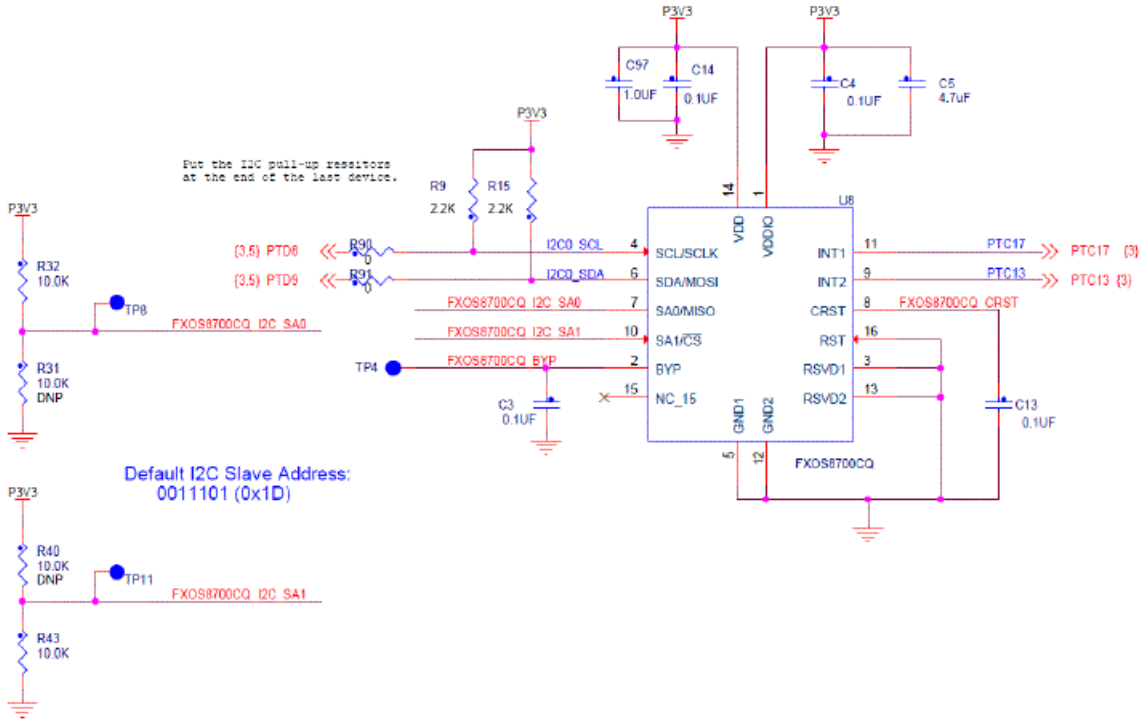

Figure 13. Accelerometer and magnetometer

Gyroscope

An NXP FXAS21002 low-power, 3-axis gyroscope with 16-bit ADC resolution is interfaced through an I2C bus and two GPIO signals, as shown in Table 7. By default, the I2C address is 0x21 (SA0 pulled high). The I2C signals is also shared with the FXOS8700CQ sensor.

FXOS8700CQ	K66F Connection
SCL	PTD8/LLWU_P24/**I2C0_SCL**/LPUART0_RX/FB_A16
SDA	PTD9/**I2C0_SDA**/LPUART0_TX/FB_A17
INT1	**PTA29**/MII0_COL/FB_A24
INT2	**PTA28**/MII0_TXER/FB_A25

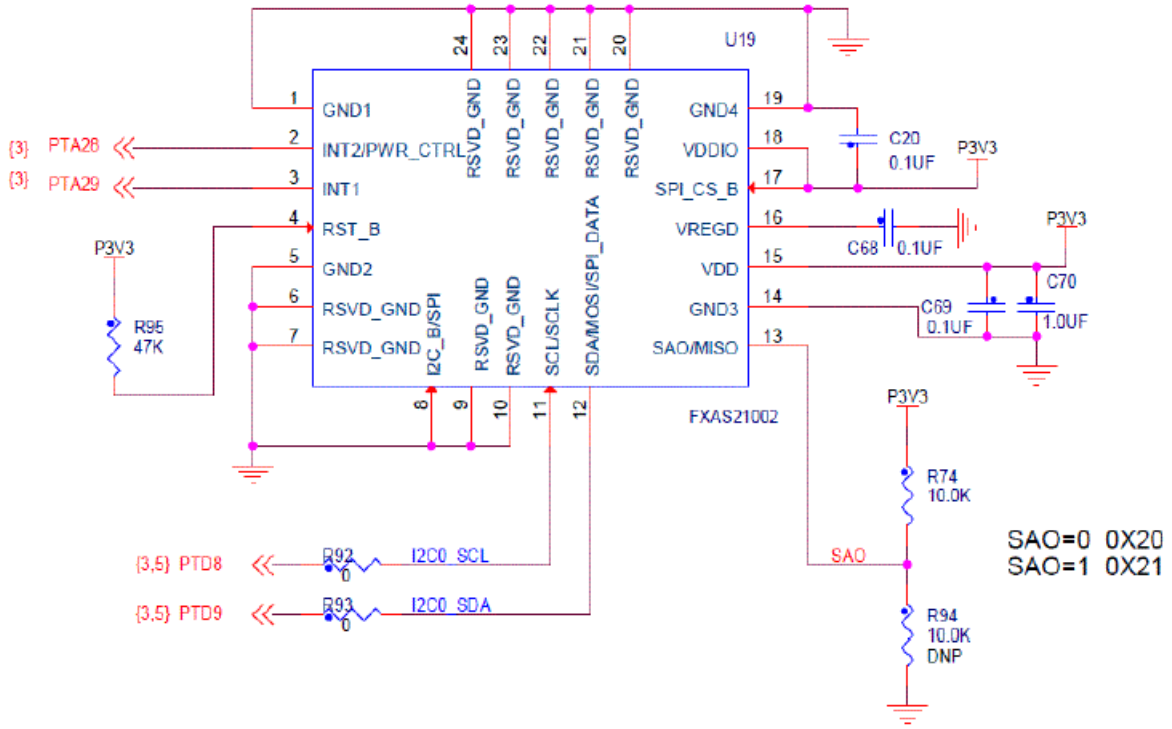

Figure 14. Gyroscope

RGB LED

An RGB LED is connected through GPIO. Table 8 shows the signal connections.

LED	K66F Connection
RED	**PTC9**/ADC1_SE5B/CMP0_IN3/FTM3_CH5/I2S0_RX_BCLK/FB_AD6/SDRAM_A14/FTM_FLT0
GREEN	**PTE6**/LLWU_P16/SPI1_PCS3/UART3_CTS/I2S0_MCLK/FTM3_CH1/USB0_SOF_OUT
BLUE	**PTA11**/LLWU_P23/FTM2_CH1/MII0_RXCLK/I2C2_SDA/FTM2_QD_PHB/TPM2_CH1

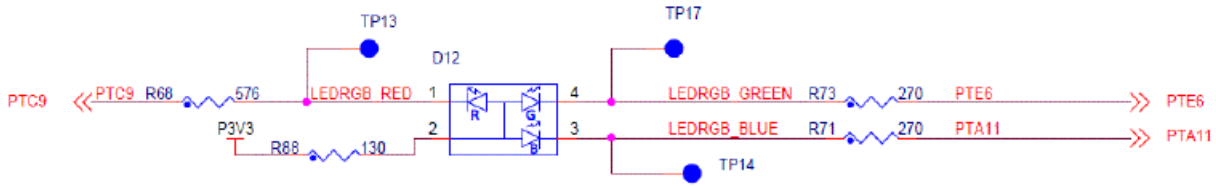

Figure 15. Tri-color LED

Serial Port

The primary serial port interface signals are PTB16 UART1_RX and PTB17 UART1_TX. These signals are connected to the OpenSDAv2.1.

Reset

The RESET signal on the K20 is connected externally to a pushbutton, SW1, and also to the OpenSDAv2.1 circuit. The reset button can be used to force an external reset event in the target MCU. The reset button can also be used to force the OpenSDAv2.1 circuit into bootloader mode. For more details, see Series and debug adapter (OpenSDAv2.1).
When using other power source and OpenSDAv2.1 is not powered, J25 2-3 must be shunt for proper reset operation.

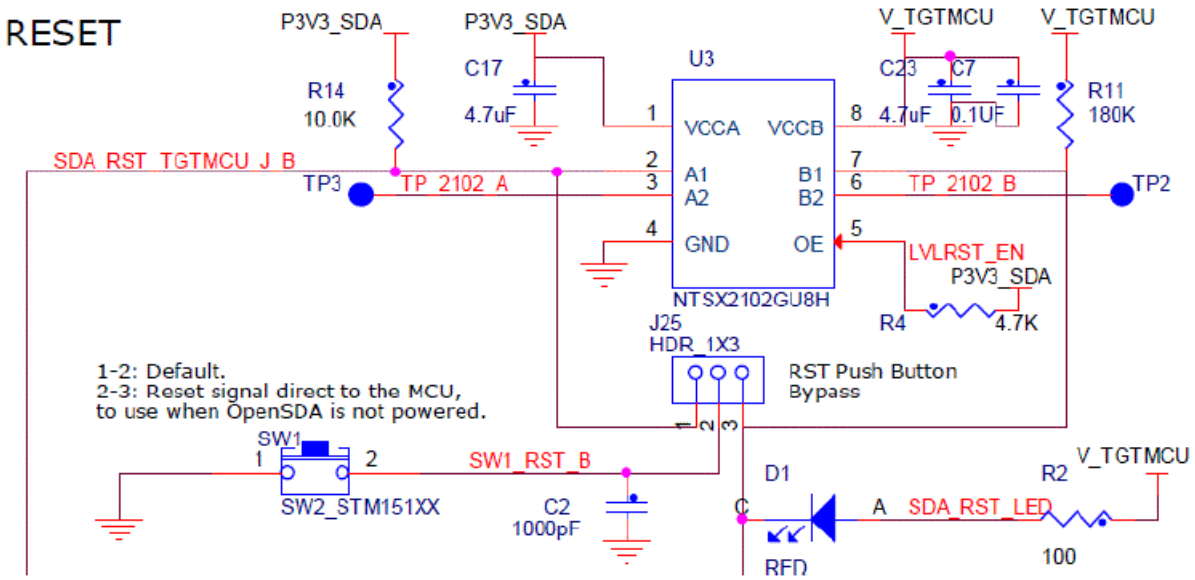

Figure 16. Reset circuit

Push Button Switches

Two push-button switches, SW2 and SW3, are available on the FRDM-K66F board. SW2 is connected to PTD11 and SW3 is connected to PTA10. Beside the general purpose IO function, both SW2 and SW3 can be used as a low-leakage wakeup (LLWU) source.
Table 9. Push button GPIO function

Switch	K66F switches connection
SW2	**PTD11**/**LLWU_P25**/SPI2_PCS0/SDHC0_CLKIN/LPUART0_CTS/FB_A19
SW3	**PTA10**/**LLWU_P22**/FTM2_CH0/MII0_RXD2/FTM2_QD_PHA/TPM2_CH0/TRACE_D0

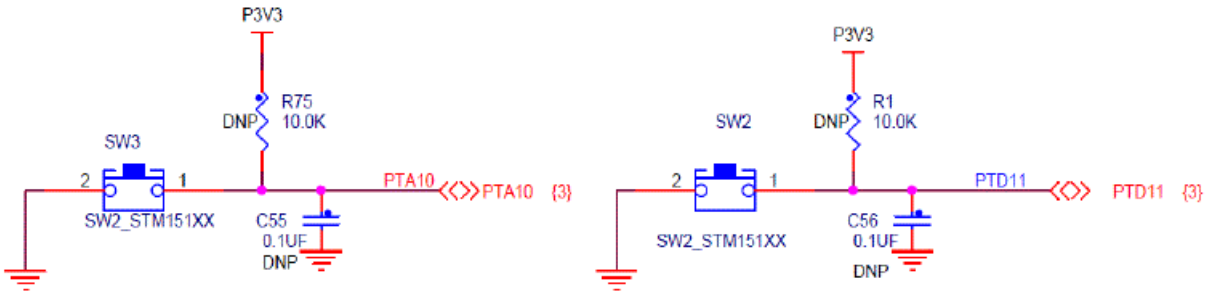

Figure 17. Push button switches

Debug

The debug interface on MK66FN2M0VMD18 is a Serial Wire Debug (SWD) port with trace output capability. There are two debug interfaces on the FRDM-K66F – an onboard OpenSDAv2.1 circuit (J22) and K66F direct SWD connection (J9) via a 10-pin header. To use an external debugger, such as J-Link on J9, you may need to disconnect the OpenSDAv2.1 SWD circuit from the K66F by cut trace at the bottom of the J8 and J12.

Audio

Audio codec

FRDM-K66F board features a Dialog DA7212 ultra-low power audio codec processor with four analog (or two analogs and two digitals) microphones with two independent microphone biases, headphone output a true-ground

Class G with integrated charge pump, stereo auxiliary input, flexible analog and digital mixing path, and DSP for ALC, 5-band EQ, noise gate, beep generator.
The Dialog audio codec (DA7212) connects to the FRDM-K66F over I2C serial communication for control, and over I2S for digital audio data. By default, the I2C address is 0x1A (Write address: 0x34 and Read address: 0x35).

The maximum I2C clock rate that the DA7212 is capable of is 1 MHz, whereas the K66F is capable of 1 MHz. However, due to the FRDM board configuration, the maximum I2C clock that the FRDM can support is 400 KHz. Digital audio data is transported between the DA7212 and the MCU over I2S data lines. The master/slave configuration is defined by software drivers. When DA7212 is in slave mode, DA7212 receives BCLK and WCLK. When DA7212 is in master mode, DA7212 generates BCLK and WCLK.

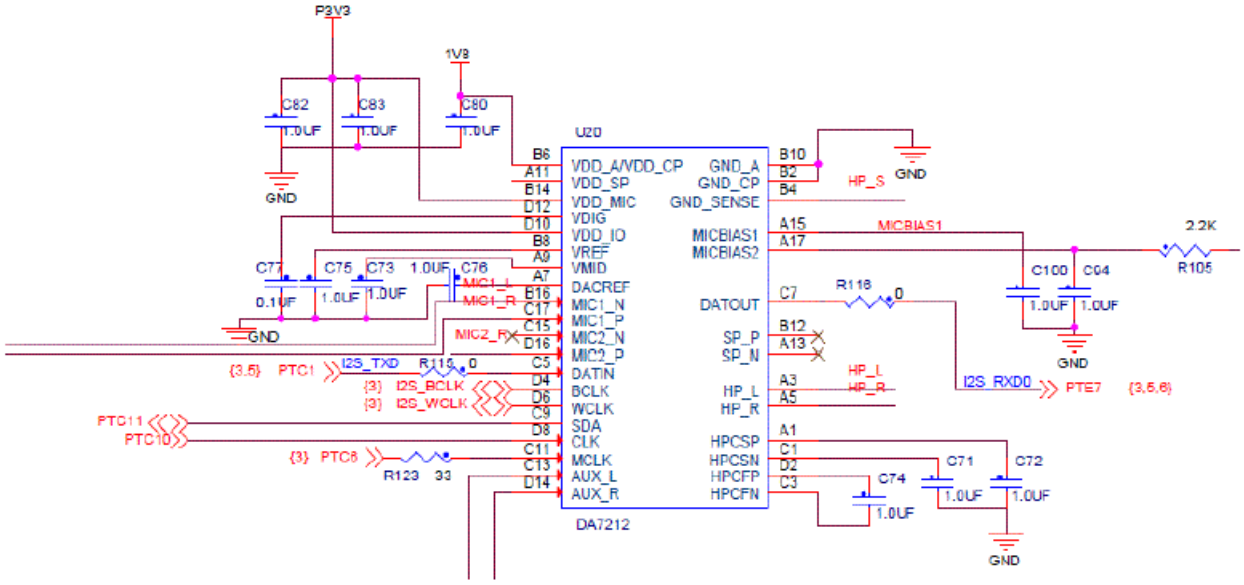

Figure 18. FRDM-K66F Audio Codec DA7212

Digital MEMS microphone
An Akustica AKU242 high-definition onboard Micro-Electrical Mechanical System (MEMS) microphone (U22) is interfaced through a Pulse Density Modulated (PDM). There are two available options either for K66F direct PDM communication which requires additional software protocol and CPU cycles to handle PDM protocol or uses DA7212 to convert PDM on the fly to Pulse-code modulation (PCM) for K66F communication. By default, J30 and J31 are shunt 1-2 to DA7212.

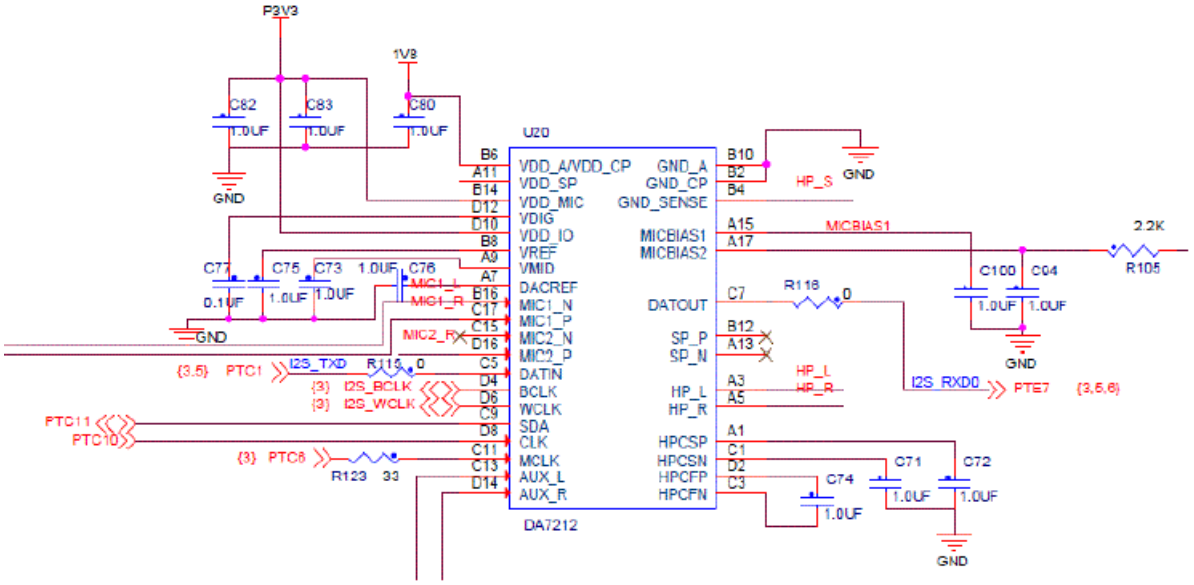

Figure 19. Digital Mic connection

I/O connectors

Headset

A standard headset with a microphone can be attached to the FRDM-K66F via a 3.5 mm 4-pole socket J28. There are two configurations on headset depending on the headset manufacturer. J35 1-2 and J36 1-2 (Default setup) or J35 2-3 and J36 2-3 can be used to route the MIC and GND signals for the two configurations. The headphone left and right channels remain fixed.

Figure 20. Headset Jack diagram

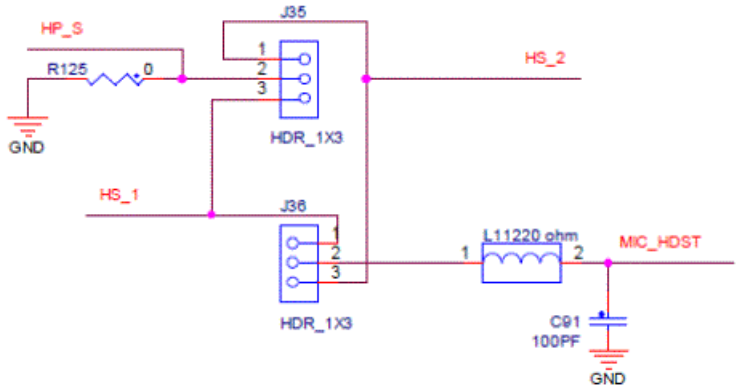

Figure 21. FRDM-K66F headset configuration

The DC bias for the headset microphone is sourced from MICBIAS2. The microphone signal is input to the DA7212 on MIC2_R.

Jumper configuration J35 & J36	FRDM-K66F headset configurations
Shunt 1-2	L/R/GND/MIC (default)
Shunt 2-3	L/R/MIC/GND

16.3.2. Auxiliary audio input (AUX_IN)

Analogue signals can be connected to auxiliary input AUX_L/AUX_R via a 3.5 mm jack socket J29. The analog inputs are DC biased and a series DC blocking capacitor is added to the input path.

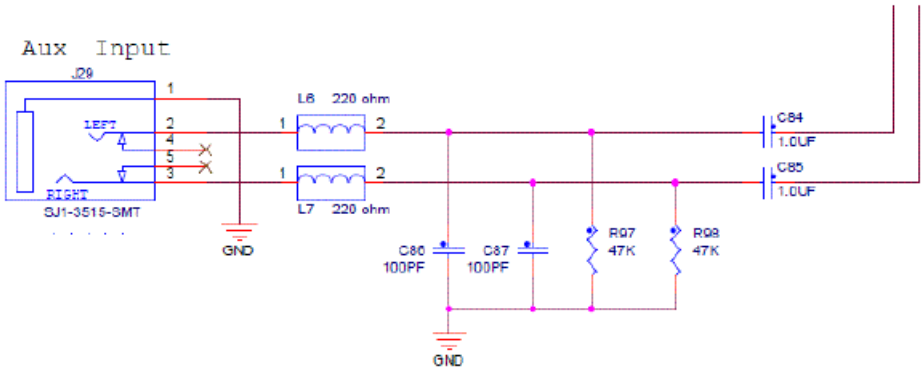

Figure 22. FRDM-K66F AUX_IN

Analog microphone

Two external analog microphones can be attached to the board via jumper header 1×2 J32 and J33. J32 pin 1 is routed to MIC1_R and J33 pin 1 is routed to MIC2_R. Both J32 and J33 pin 2 is ground. MIC2_R is too connected to 3.5 mm dual role headset J28. The DC bias for MIC1_R is sourced from MICBIAS1 and MIC2_R is sourced from MICBIAS2.

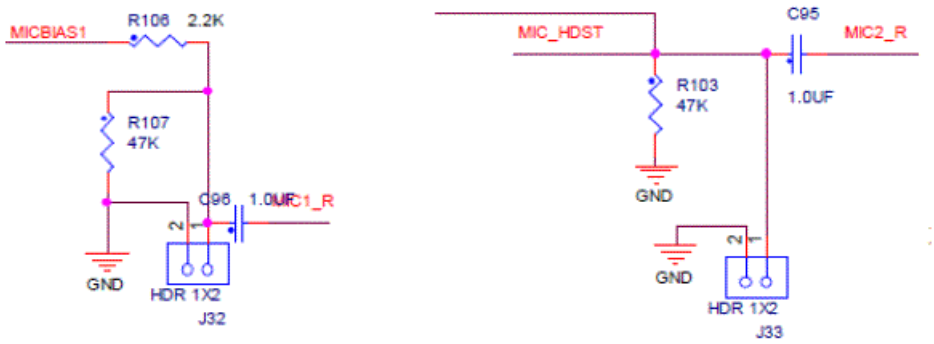

Figure 23. Analog microphone

Add-on Modules

RF module

An optional header (J6) on the FRDM-K66F supports communication with a 2.4 GHz nRF24L01+ Nordic Radio module over SPI. Alternatively, any SPI-based device or module can be used with this header.

Pin	Function	FRDM-K66F RF connection
1	GND	Ground
2	P3V3	3.3 V Board supply
3	CE	**PTB20**/SPI2_PCS0/FB_AD31/SDRAM_D31/CMP0_OUT
4	CS	PTD4/LLWU_P14/SPI0_PCS1/UART0_RTS/FTM0_CH4/FB_AD2/SDRAM_A10/EWM_IN/**SPI1_PCS0**
5	SCK	PTD5/ADC0_SE6B/SPI0_PCS2/UART0_CTS/UART0_COL/FTM0_CH5/FB_AD1/SDRAM_A9/EWM_O UT/**SPI1_SCK**
6	MOSI	PTD6/LLWU_P15/ADC0_SE7B/SPI0_PCS3/UART0_RX/FTM0_CH6/FB_AD0/FTM0_FLT0/**SPI1_SOUT**
7	MISO	PTD7/CMT_IRO/UART0_TX/FTM0_CH7/SDRAM_CKE/FTM0_FLT1/**SPI1_SIN**
8	IRQ	**PTC18**/UART3_RTS/ENET0_1588_TMR2/FB_TBST/FB_CS2/FB_BE15_8_BLS23_16/SDRAM_DQM1

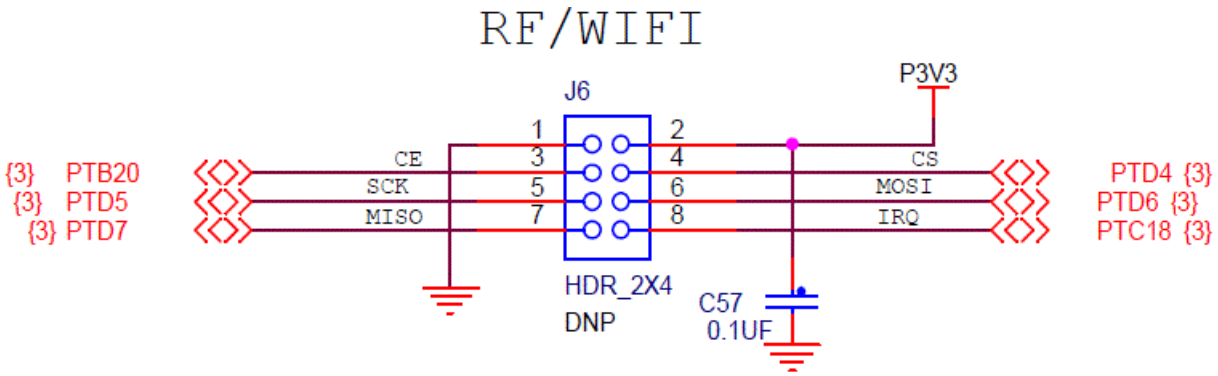

Figure 24. Optional add-on RF/SPI module

Bluetooth module

An optional header (J199) on the FRDM-K66F supports communication with add-on Bluetooth, such as the JY-

MCU BT Board V1.05 BT wireless Bluetooth module, over a UART.
Alternatively, and serial (SCI) module can be used with this connector. Note that the serials are 3 V levels and do not conform to RS-232 logic levels, so a level shifter such as Maxim DS3232 should be used with RS-232 devices.

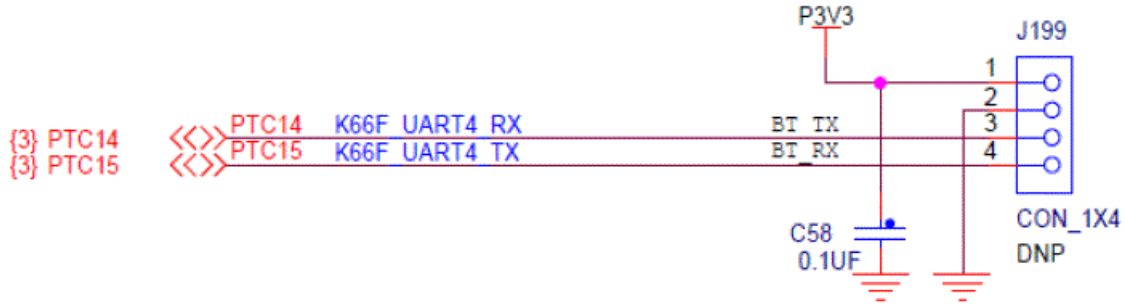

Figure 25. Optional add-on bluetooth/SCI module

Input/Output connectors

The MK66FN2M0VMD18 microcontroller is packaged in a 144-pin MapBGA. Some pins are used in onboard circuitry, but some are directly connected to one of four I/O headers (J1, J2, J3 and J4).
The pins on the K66F microcontroller are named for their general-purpose input/output port pin function. For example, the 1st pin on Port A is referred to as PTA1. The name assigned to the I/O connector pin corresponds to the GPIO pin of the K66F.

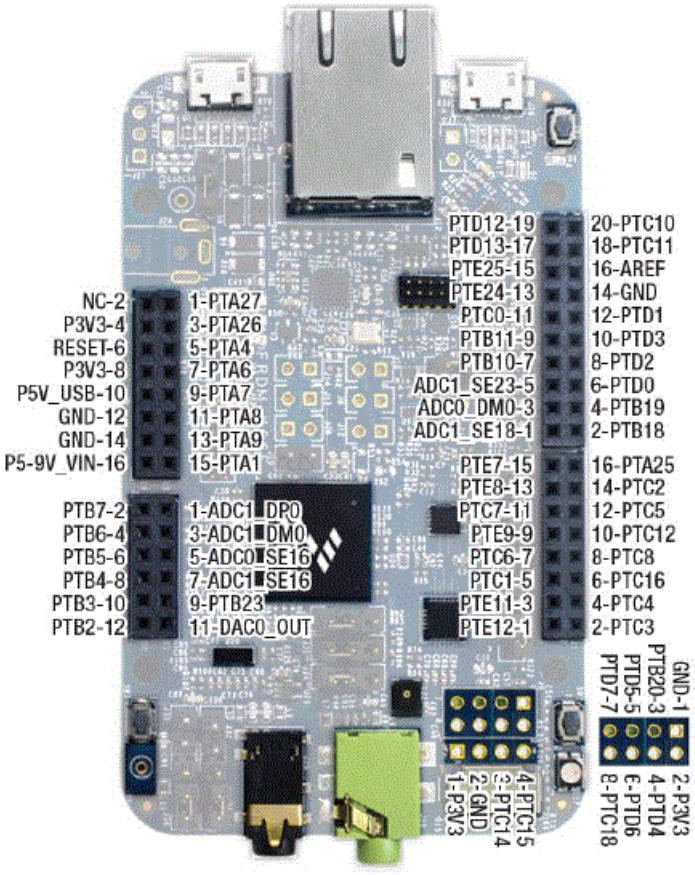

Figure 26. FRDM-K66F I/O header pinout

Arduino Compatibility

The I/O headers on the FRDM-K66F are arranged to allow compatibility with peripheral boards (known as shields) that connect to Arduino and Arduino-compatible microcontroller boards. The outer rows of pins (Even numbered pins) on the headers share the same mechanical spacing and placement as the I/O headers on the Arduino Revision 3 (R3) standard.

Miscellaneous

PTA4

References

The following references are available on www.NXP.com/FRDM-K66F

- FRDM-K66F Quick Start Guide
- FRDM-K66F Schematic, FRDM-K66F-SCH
- FRDM-K66F Design Package

Other references:

- DA7212 (**http://www.dialog-semiconductor.com/products/audio/audio-codecs/da7212**)
- AKU240 (**http://www.akustica.com/DigitalHDvoicemic.asp**)

Revision History

Table 12. Revision history

Revision number	Date	Substantial changes
0	02/2016	Initial release

How to Reach Us:
Home Page: **nxp.com**
Web Support: **nxp.com/support**

Documents / Resources

	NXP Semiconductors FRDM-K66F Development Platform [pdf] User Guide FRDM-K66F Development Platform, FRDM-K66F, Development Platform, Platform

References

- Free open source IoT OS and development tools from Arm | Mbed
- NXP® Semiconductors Official Site | NXP Semiconductors
- Our Terms And Conditions Of Commercial Sale | NXP Semiconductors
- Support | NXP Semiconductors
- FRDM-K66F|Freedom Development Platform|Kinetis® MCUs | NXP Semiconductors
- OpenSDA V2 Firmware