multiLane AT4039D 4-Lane 23-29 GBaud Bit Error Ratio Tester User Manual

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Notices

publication supersedes that in all previously published material. Specifications and price change privileges reserved.

General Safety Summary
Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified. Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the General Safety Summary in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Only use the power cord specified for this product and certified for the country of use.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal that exceeds the maximum rating of that terminal. Do Not Operate Without Covers.

Do not operate this product with covers or panels removed. Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate with Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions. Do Not Operate in an Explosive Atmosphere. Keep Product Surfaces Clean and Dry

 Caution statements identify conditions or practices that could result in damage to this product or other property.

Contents

INTRODUCTION

This is the user operation manual for the AT4039D. It covers the installation of its software package and explains

how to operate the instrument for pattern generation and error detection; how to control the clocking system, inputs/outputs and all the available measurements.

Acronym	Definition
BERT	Bit Error Rate Tester
API	Application Programming Interface
NRZ	Non-Return to Zero
GBd	Gigabaud
PLL	Phase-Locked Loop
PPG	Pulse Pattern Generator
GHz	Gigahertz
PRD	Product Requirements Document
I/O	Input/Output
R&D	Research & Development
HW, FW, SW	Hardware, Firmware, Software
GUI	Graphical User Interface
ATE	Automatic Test Equipment
HSIO	High-Speed I/O

API and SmarTest Documents

- This manual supports the instrument AT4039D and it is compatible with the Advantest V93000 HSIO test head extender frame/twinning.
- All APIs are available for Linux and tested under Smartest 7. For the list of APIs and how to use them please refer to the “API” folder on the AT4039D webpage.
- This manual does not explain how to operate the instrument using SmarTest environment. Refer to Advantest’s website below for SmarTest document noting that it may change without notice and also require login privileges provided through Advantest.
  https://www.advantest.com/service-support/ic-test-systems/software-informationanddownload/v93000-software-information-and-download

Product Software

The instrument includes the following software:

AT4039D GUI.
Instrument GUI runs on Windows XP (32/64 bit), Windows 7,8 and 10.

NOTE. These applications require the Microsoft .NET Framework 3.5.

If the Microsoft.NET Framework 3.5 is needed, it can be downloaded through this link:

http://download.microsoft.com/download/2/0/e/20e90413-712f-438c-988efdaa79a8ac3d/dotnetfx35.exe.

For more products updates, check the following webpage: https://multilaneinc.com/products/at4039d/

Minimum PC Requirements

The Windows PC properties for the AT4039D GUI application should meet the following specifications:

- Windows 7 or greater
- Minimum 1 GB RAM
- 1 Ethernet card to establish connection with the device
- USB connector
- Pentium 4 processor 2.0 GHz or greater
- .NET Framework 3.5 sp1

NOTE: It is recommended to connect the BERT via Ethernet to one PC only to prevent conflict from multiple user commands.

NOTE: It is not recommended to hook up the instrument to a slow network or to connect to it through WiFi

Installation

This section address installation and bring-up of the instrument, addressing the following topics:

- System start-up
- Connection guide

First Steps

When you first receive the instrument, it has a pre-configured IP address from the factory. This IP address is printed on a label on the instrument. You may choose to keep this IP or to change it. If you need to change the IP address refer to “How to change IP and update firmware” section.

Connect through Ethernet:
Connect the PC to the RJ45 connectors located on the side of the V93000 twinning frame through an Ethernet cable. Ethernet is the only way to control the Multilane cassettes. In order to connect via Ethernet, you need to know the IP address of the instrument you need to connect to. Check labeling on the cassette shell.

A simple ping using the windows command line interface is recommended to check if your controlling terminal is able to reach the instrument.

When To change the IP address of the board, you need to install the USB drivers (refer to section USB Driver Installation).

The instrument is now powered up and connected through the right IP address. Next, you need to configure the signal generated.

GUI Overview

Although the AT4039D is an ATE type of instrument, it can be used as any other Multilane BERT and can be controlled from the general BERT GUI for Windows. This is for instance useful when troubleshooting a setup. The general BERT GUI can be downloaded from the company website, under the download section of the AT4039D.

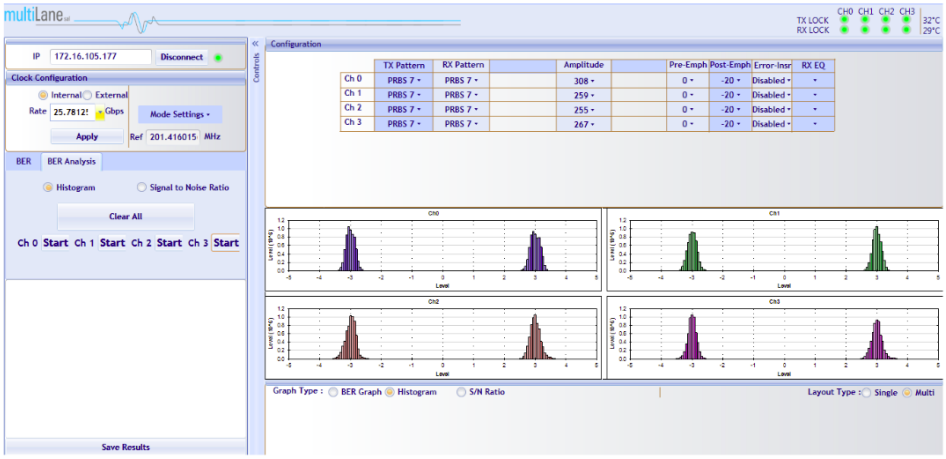


Figure 1: AT4039D GUI

In your instrument's GUI, there are several control fields that are each explained below.

Instrument Connect Field

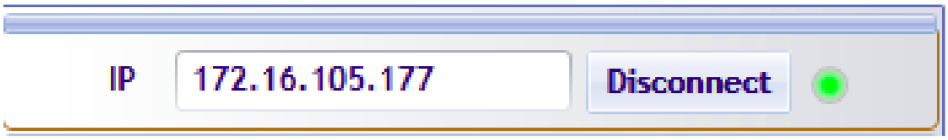


Figure 2: Connect Via Ethernet

The first thing you want to do is to make sure you are connected to the instrument. If you are, the connect button will read Disconnect and the green LED lights up.

PLL Lock and Temperature Status Field

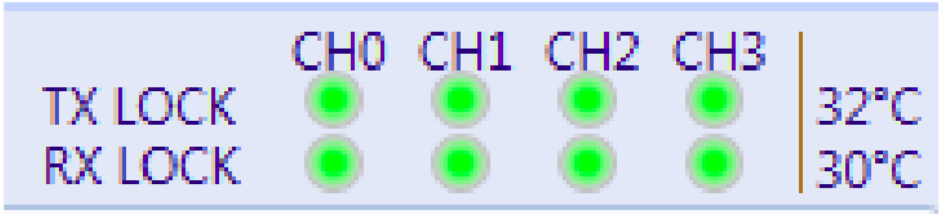


Figure 2: Connect Via Ethernet

Keep an eye on the LEDs and temperature readings on this field. TX Lock means that the PLL of the PPG is locked. RX lock goes green only if a signal of correct polarity and PRBS kind is detected on the error-detector.

If the temperature reaches 65 C, the electronics will auto shut off.

Reading the installed Firmware Revision

The installed firmware version is displayed in the upper right corner of the GUI.

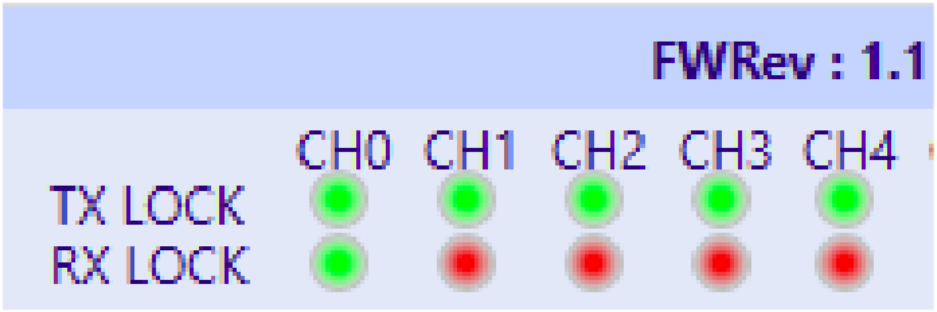


Figure 3: PLL Lock and Temperature Status

Figure 4: Reading the Installed Firmware Revesion

Line Rate Configuration (Applies to all channels at once)

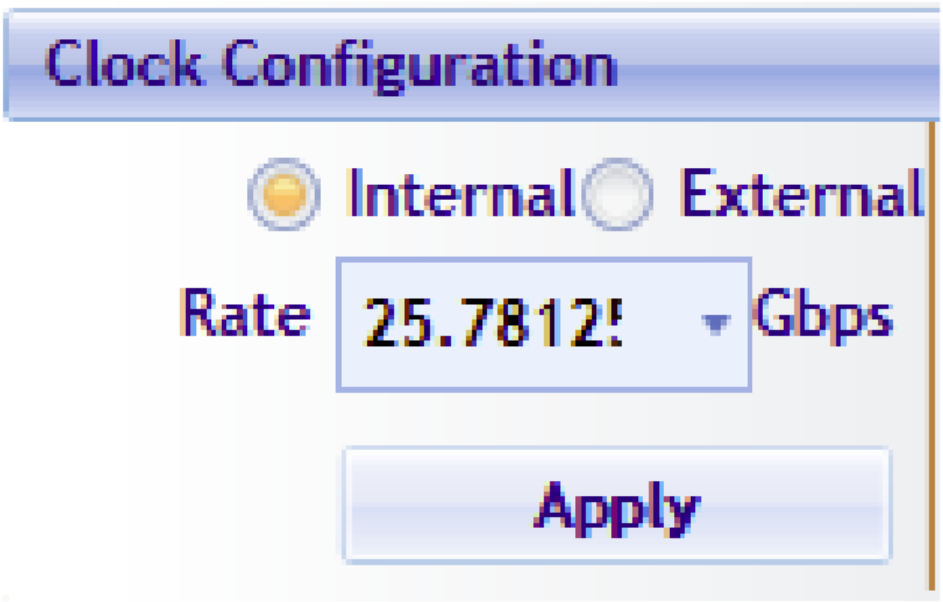


Figure 5: Line Rate Configuration

This is where you set the bitrate for all 4 channels by typing in the desired rate. The drop down menu lists a shortcut to the most widely used bitrates, however you are not limited only to that list. You can also select the clock input. The clock is internal by default. You should only change to external clock feed in when you need to synchronize two or more AT4039Ds to each other in a slave-master fashion; In that case you connect the clocks in daisy chain. After changing from internal to external clock and vice versa, you have to click apply for changes to take effect (this takes a few seconds).

Mode & Clock Out Settings (Apply to all channels at once)

Description

The “Ref” denotes the frequency of the clock output. This is a function of the bitrate and will vary according to your clock-out settings under the “Mode” menu. Knowing the clock frequency being output by the BERT is helpful when you want to trigger an oscilloscope.

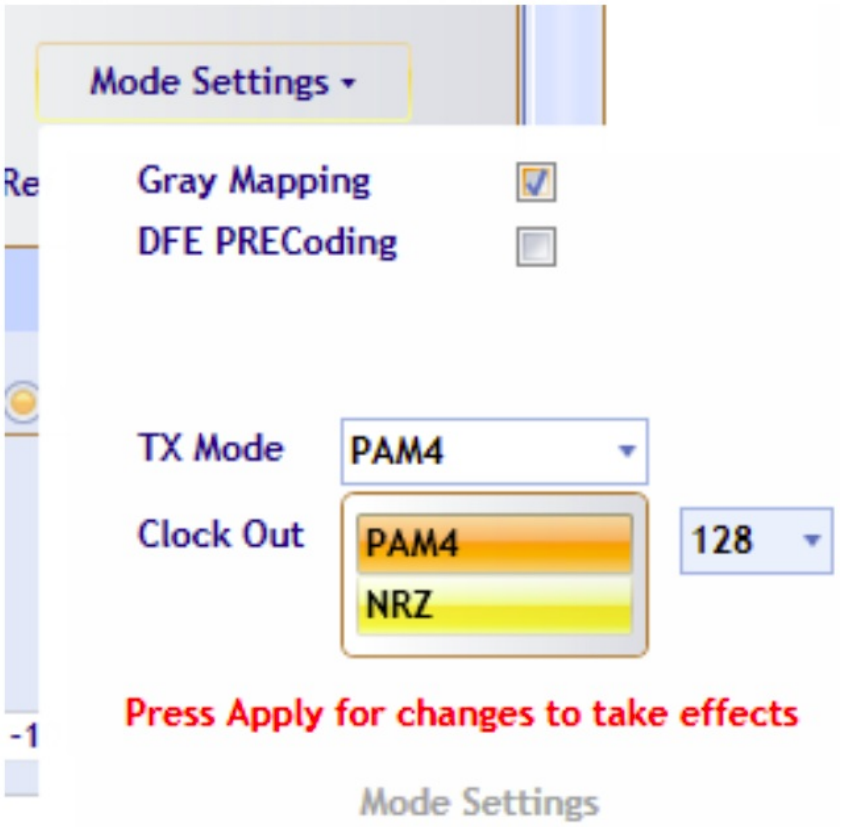
Some oscilloscopes require a clock frequency above 2 GHz. To get the AT4039D to output that, go under mode settings and select the Clock out to be “Monitor”. Choose the denominator so that the result is within the scope range. In the case of the AT4025 , the Ref Clk is used to generate clock from the AT4039D side.

To switch between NRZ and PAM-4 coding, use the TX Mode setting, then click Apply. The options Gray Mapping and DFE pre-coding are only available in PAM4 mode.

DFE Pre-coding sends a pre-amble for a DFE receiver to sync to before the actual PRBS pattern is transmitted, to avoid DFE error propagation. The decoder implements a 1+D scheme in response to an ? = ? ?+? encoding. Currently the DFE precoding is automatic and not user selectable.

Gray Mapping enables use of PRBSxxQ defined in IEEE802.3bs. When Gray mapping is enabled, the PRBS13 and PRBS31 under the pattern select menu turn into PRBS13Q and PRBS31Q respectively. Gray mapping basically re-arranges the symbol mapping to the following:

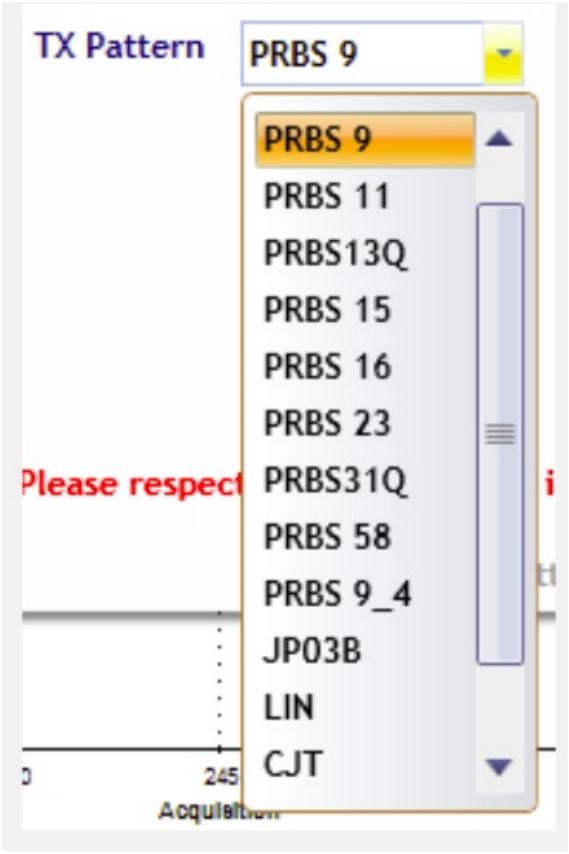
- 00 → 0
- 01 → 1
- 11 → 2
- 10 → 3



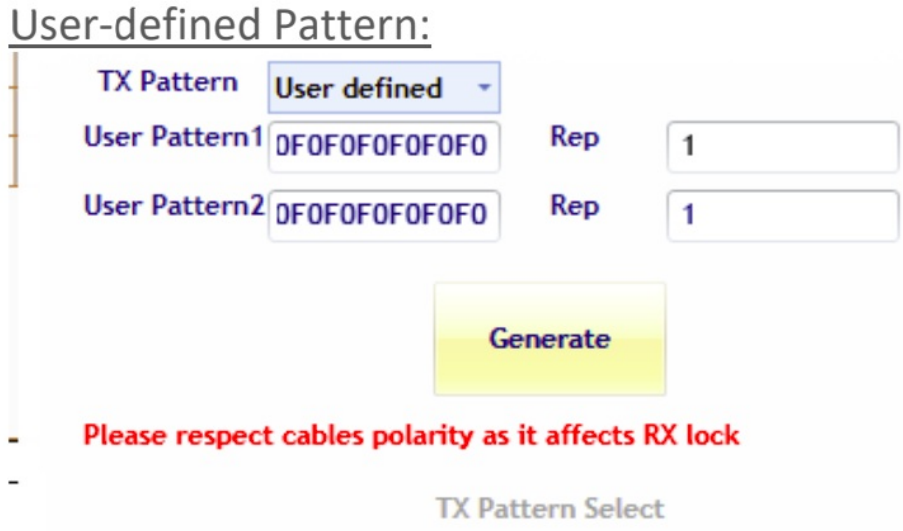
	TX Pattern	RX Patter n	I Outter Eye	Amplitude	Inner Eye	Pre-Em ph	Post-Emph Err or-Insr	RX EQ
Ch 0	PRBS 9 v	PRBS 9 –	2000 v	213 –	1000 v	0 –	0 v Disa bled v	0 –
Ch 1	PRBS 9 •	PRBS 9 –	2000 –	220 v	1000 –	0 –	0 – Disabled –	0 •
Ch 2	PRBS 9 w	PRBS 9 v	2000 w	210 •	1000 w	0 v	0 v Disa bled v	0 –
Ch 3	I PRBS 9 v	PRBS 9 •	2000 v	222 –	1000 v	0 y	0 v Disabled v	0 w

The AT4039D can output a wide range of predefined patterns. In addition to the PRBS patterns, there are linearity and jitter test patterns. Also, on top of the pre-defined patterns the user has the possibility of defining his/her own pattern – more on this further below.

Note: error detection only works on the PRBS patterns existing in the RX pattern drop down list. It isn't possible to do error detection on custom defined patterns.

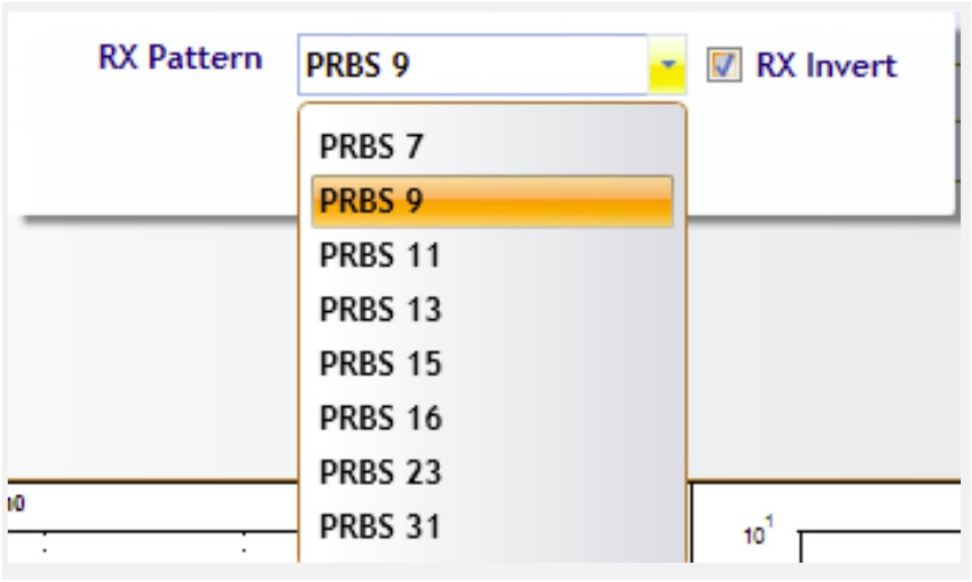


- The custom pattern is made up of 2 fields with 16 hexadecimal characters each. One must fill out both fields with all 32 hex characters.
- Every hex character is 4 bits wide, making up 2
- PAM4 symbols; example 0xF is 1111 so in Graycoded PAM domain this results in 22, assuming the
- PAM levels are denoted 0, 1, 2 and 3
- Example 2: to transmit a stair signal 0123, fill out the fields with repetitions of 1E



In the RX Pattern menu, one can browse all the patterns with which error detection is possible.

Note that TX and RX pattern must be the same to acquire RX lock and consequently be able to do measurements. Also the pattern polarity is very important and makes all the difference between having RX PLL lock or no lock at all. You can ensure correct polarity by connecting the TX-P side of the cable to the RX-P and the TX-N to the RX-N. if you do not respect this rule, you can still invert polarity from the GUI on the RX side only.

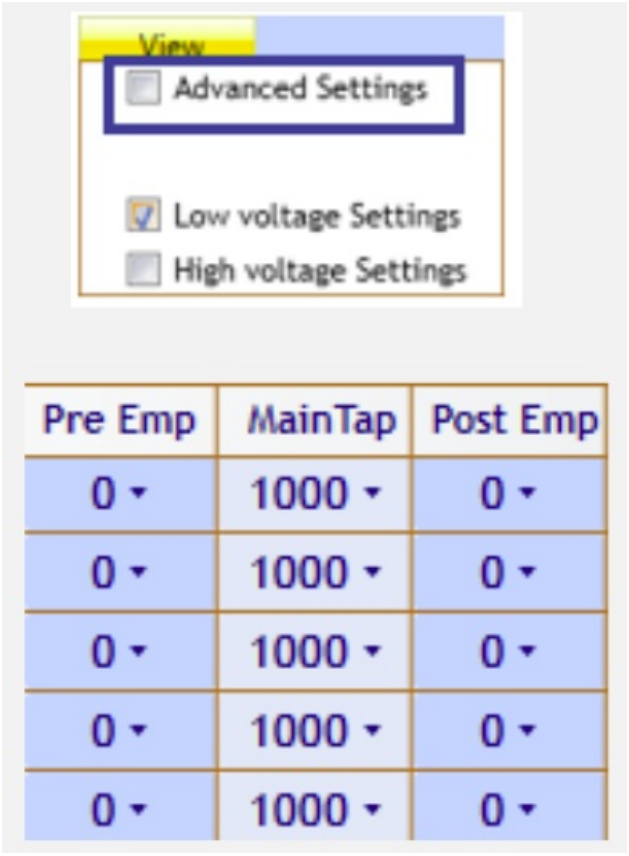


Inner and Outer eye level controls trim the high and low values of the middle PAM eye. Possible control values range from 500 to 1500 for the inner eye control and from 1500 to 2000 for the outer eye. Optimal values are typically in the middle of the range. Example of tweaking the Outer eye settings is shown below

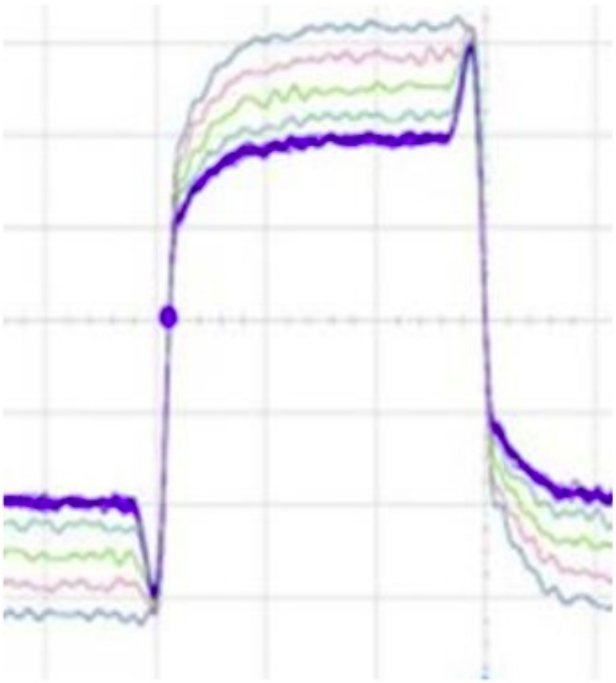
Inner Eye	Outter Eye
1000	2000
1000	2000
1000	2000
1000	2000

The default amplitude control is calibrated in millivolt values but does not allow you to change the equalizer settings. If you need to change the FFE tap settings, please go to then enable ‘Advanced Settings’. This enables you to controlpre- and post-emphasis values for each channel, but amplitude values will not be shown in millivolt. By default, three taps are shown and can be edited. Think of the amplitude as a digital equalizer with main tap, pre-cursor (pre-emphasis) and postcursor (post-emphasis). In the regular case, preand post cursors are set to zero; the amplitude is controlled using the main tap. The main, pre- and post-taps use digital values ranging between -1000 and +1000. Increasing and decreasing the pre and post cursors will also affect the amplitude. Please ensure that the sum of pre-, post and main cursors is ≤ 1000 to have optimal performance. If the sum of taps exceeds 1000, linearity of the TX signal cannot be maintained.

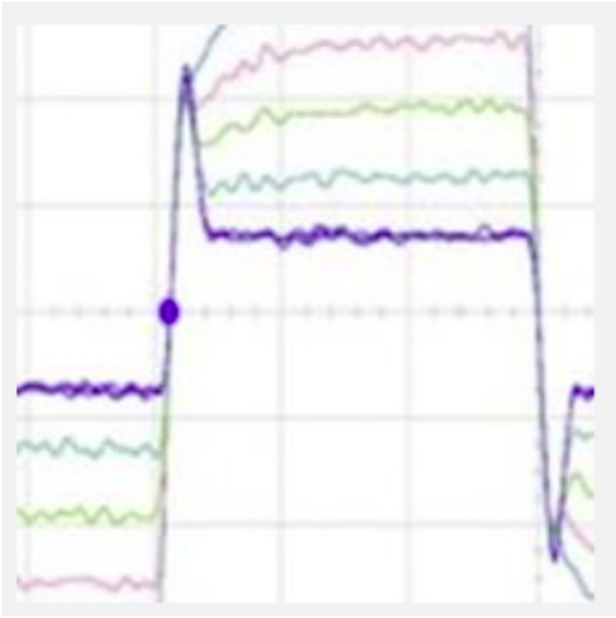
Amplitude Settings:



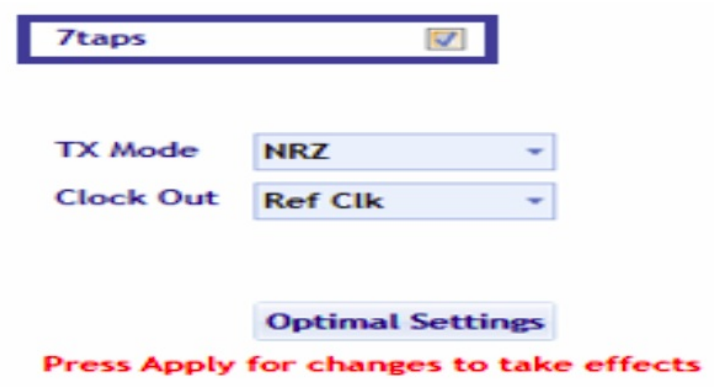
Pre-cursor effect on a pulse



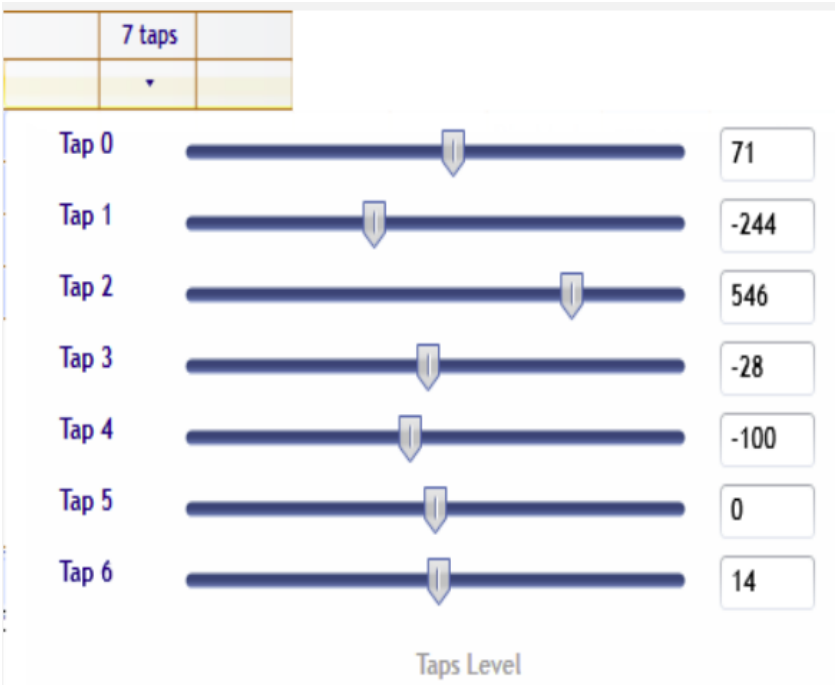
Post-cursor effect on a pulse



The user can also edit a 7 taps coefficients instead of just 3 taps by clicking on and then checking the box of.

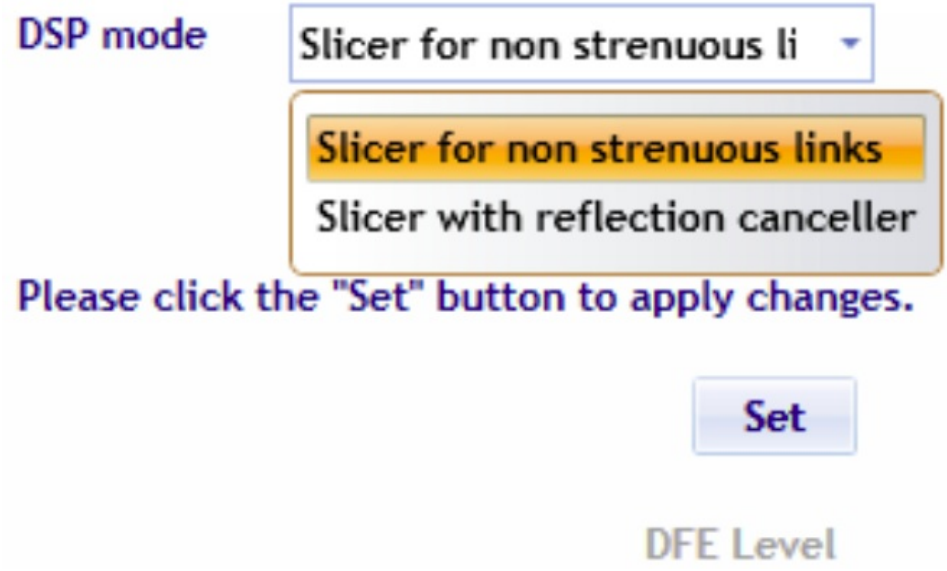


After applying the settings, the seven-tap control will be available for editing under the amplitude menu. Any one of the 7 taps can be defined as main tap; in this case, taps preceding it will be precursors. Likewise, taps following the main tap will be post-cursors.



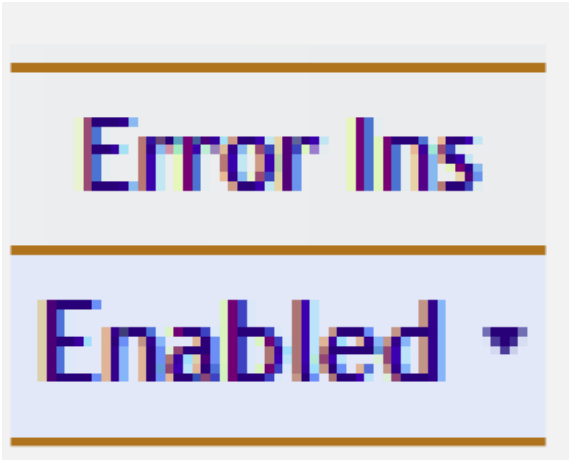
The slicer is the default mode. The reflection canceller consumes more power but is useful for strenuous channels containing transitions of impedance

RX Equalization



Error insertion is carried out on a block by block basis. Each block is 64 bits, divided into 32 MSBs and 32 LSBs.

Error Insertion



Example Inner and Outer Settings Effect:

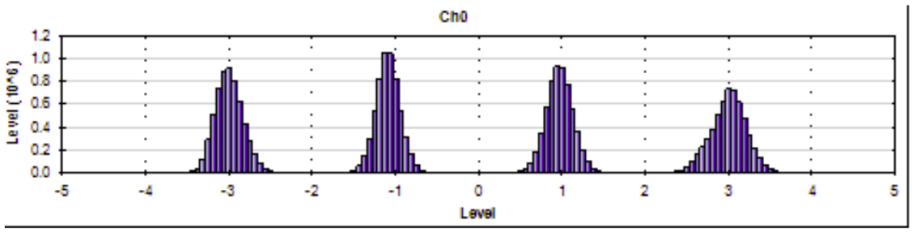


Figure 6: Default Inner and Outer settings of 1000 and 2000

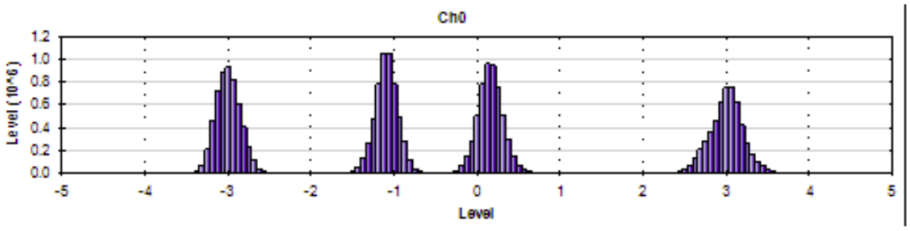


Figure 7: Outer Eye is set 1600; Inner eye kept at 2000

Taking Measurements

Bit Error Ratio Reading

To be able to start BER measurements, the instrument ports should be in the loopback mode, which means TX port should be connected to the RX port and the PPG and ED patterns should match. One does not necessarily need to supply a PRBS from the same physical instrument – the source can be a different instrument and the error-detector of the AT4039D can derive its own clock from the received data (no need for a separate clock link). However, if Gray coding is used in the source, one should tell the receiver to expect Gray coding as well. If there is a match in pattern, polarity, and coding but still no lock, there could be an MSB/LSB swap on one side.

BER Control

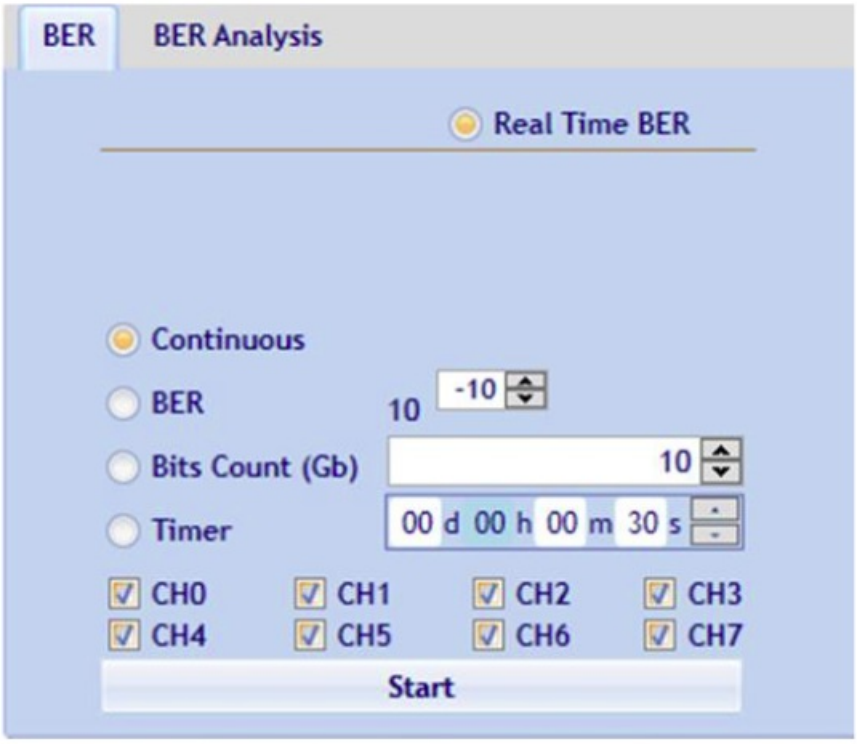
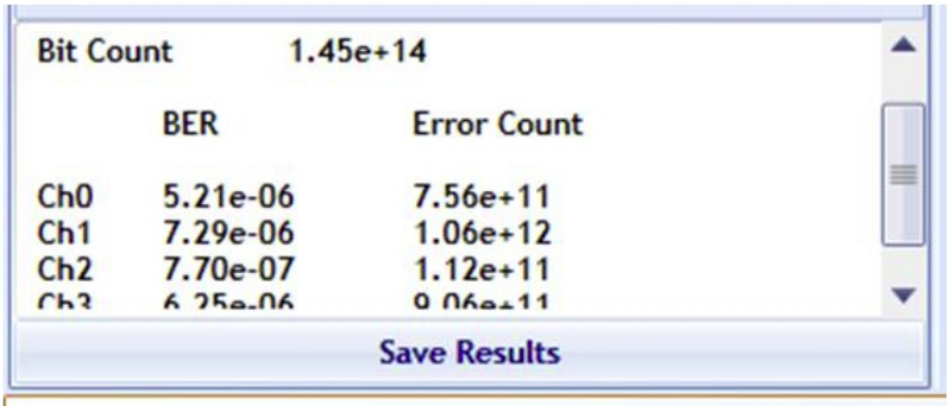


Figure 8: BER Control panel

A BER measurement can run in continuous mode and will not stop until the user intervenes and clicks the stop button. BER can also be set to run until a target value is reached or until a certain number of bits has been transmitted (units of 10 gigabits). The Timer lets the user set a time for the BER to stop.

BER Table of Results
The summary of BER measurements is shown in the following pane:



BER Graph
Plots BER values collected on the graph

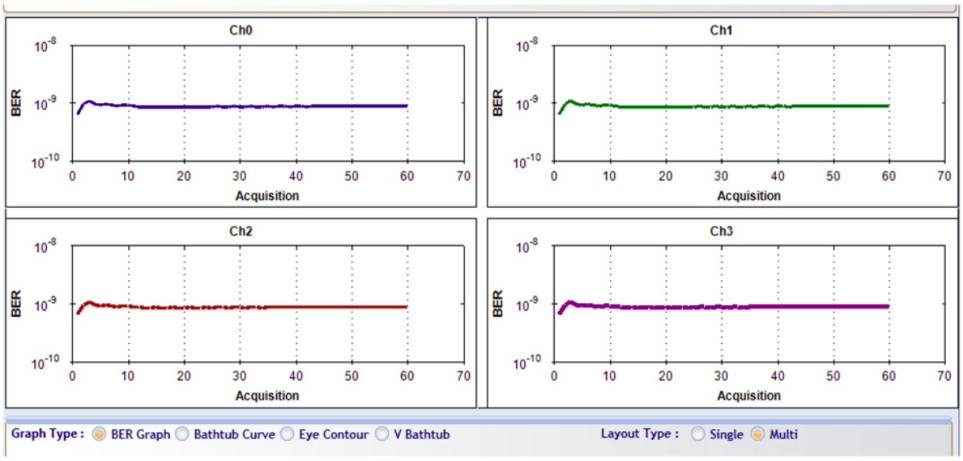


Figure 9: BER Graphs

Histogram Analysis

The histogram is the tool of choice to troubleshoot the link. You can think of it as a scope built into the receiver and it works even if you do not have pattern lock. For both NRZ and PAM signals, the histogram graph is shown as follows:

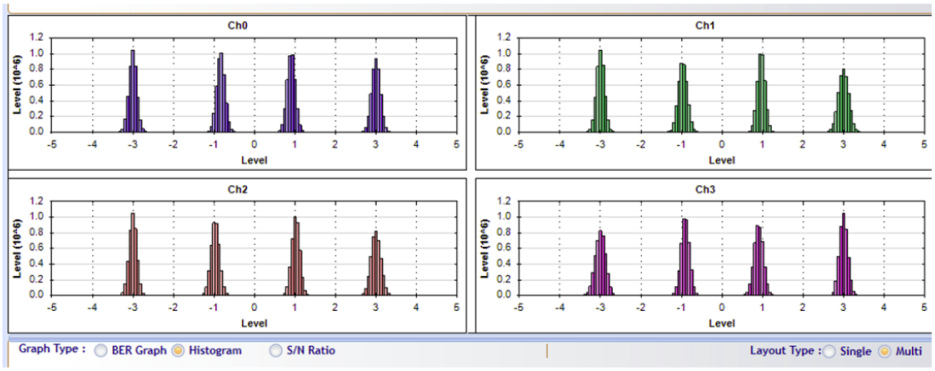


Figure 10: PAM Histogram

The thinner the peaks the better the performance of the PAM signal and the less the jitter. These peaks can be enhanced using the pre/post-emphasis available.

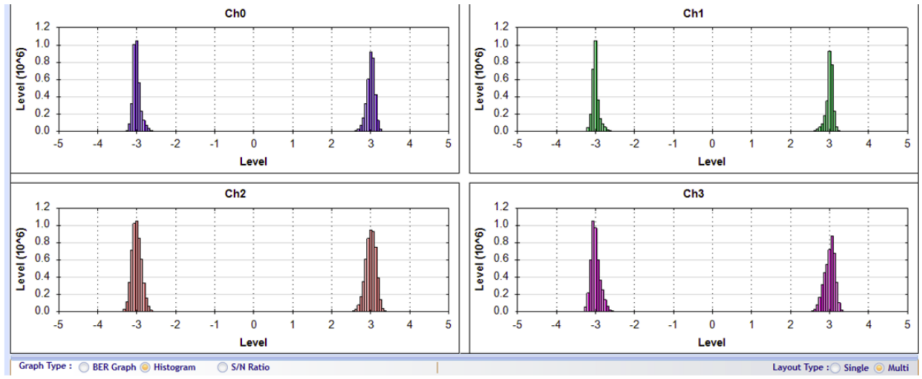


Figure 11: NRZ Histogram

The same analogy applies as that of the PAM histogram.

Signal to Noise Ratio Analysis

SNR is a quantitative way to measure the strength of the received signal – it is given in dB.

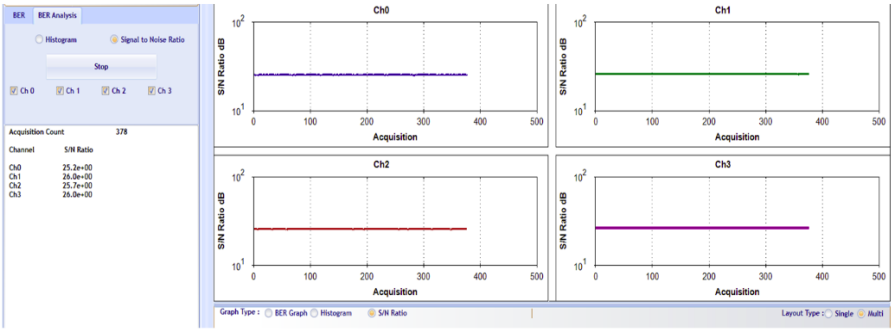


Figure 12: SNR ratio for PAM signal

Log file System
In the AT4039D BERT there is a log file system, where every exception handled or unhandled by the GUI will be saved. After the first run, the GUI creates a file in the main directory/exception log, and saves all the existed exceptions. In case the user had a problem with the software, he can send the exception file to our team.

Note: the exception file will be deleted automatically after every 1 week of work.

Saving and Loading Settings

The instrument always saves the last used settings in non-volatile memory. These settings are automatically restored the next time you connect to the BERT. In addition, you can create and save your own set of setup files and can revert to them when needed. Look for the Save/Load menu in the menu bar of the GUI.

How to Change IP Address and Update Firmware

For info regarding changing IP address and updating firmware of the AT4039D, kindly download “Maintenance” folder from https://multilaneinc.com/products/at4039d/. The folder consists of the following:

- ML Maintenance GUI
- USB Driver
- User Guide

Documents / Resources

	[multiLane AT4039D 4-Lane 23-29 GBaud Bit Error Ratio Tester](#) [pdf] User Manual AT4039D 4-Lane 23-29 GBaud Bit Error Ratio Tester, AT4039D, 4-Lane 23-29 GBaud Bit Error Ratio Tester, 23-29 GBaud Bit Error Ratio Tester, Bit Error Ratio Tester, Error Ratio Tester, Ratio Tester, Tester

References

- Microsoft – Cloud, Computers, Apps & Gaming
- Download Drivers & Updates for Microsoft, Windows and more - Microsoft Download Center
- AT4039D | MultiLane
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