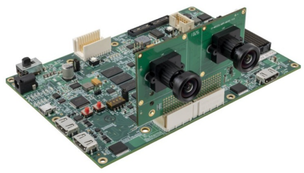

Microsemi UG0649 Display Controller User Guide

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Microsemi UG0649 Display Controller

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Configuration Parameters, page 5 section.
- Updated Resource Utilization, page 8 section.
- Updated display controller testbench waveform. See Figure 12, page 7.

Revision 6.0
The following is a summary of the changes in revision 6.0 of this document.

- Updated the Introduction, page 2 section.
- Updated the Block Diagram and Timing Diagram of Display Controller.
- Updated tables such as Inputs and Outputs of Display Controller, Configuration Parameters, and Resource Utilization Report.
- Updated the testbench configuration parameters and some of the figures of Testbench section.

Revision 5.0
The following is a summary of the changes in revision 5.0 of this document.

- Updated Resource Utilization, page 8 section.

Revision 4.0
The following is a summary of the changes in revision 4.0 of this document.

- Updated Testbench Simulation, page 6 section.

Revision 3.0
The following is a summary of the changes in revision 3.0 of this document.

- Updated section Hardware Implementation, page 3 with ddr_rd_video_resolution input signal.
- Updated the display control resolution to 4096 × 2160. For more information, see Inputs and Outputs, page 4.
- Added section Testbench Simulation, page 6.

Revision 2.0
Updated Table 2, page 5 with g_DEPTH_OF_VIDEO_PIXEL_FROM_DDR signal. For more information see Configuration Parameters, page 5 (SAR 76065).

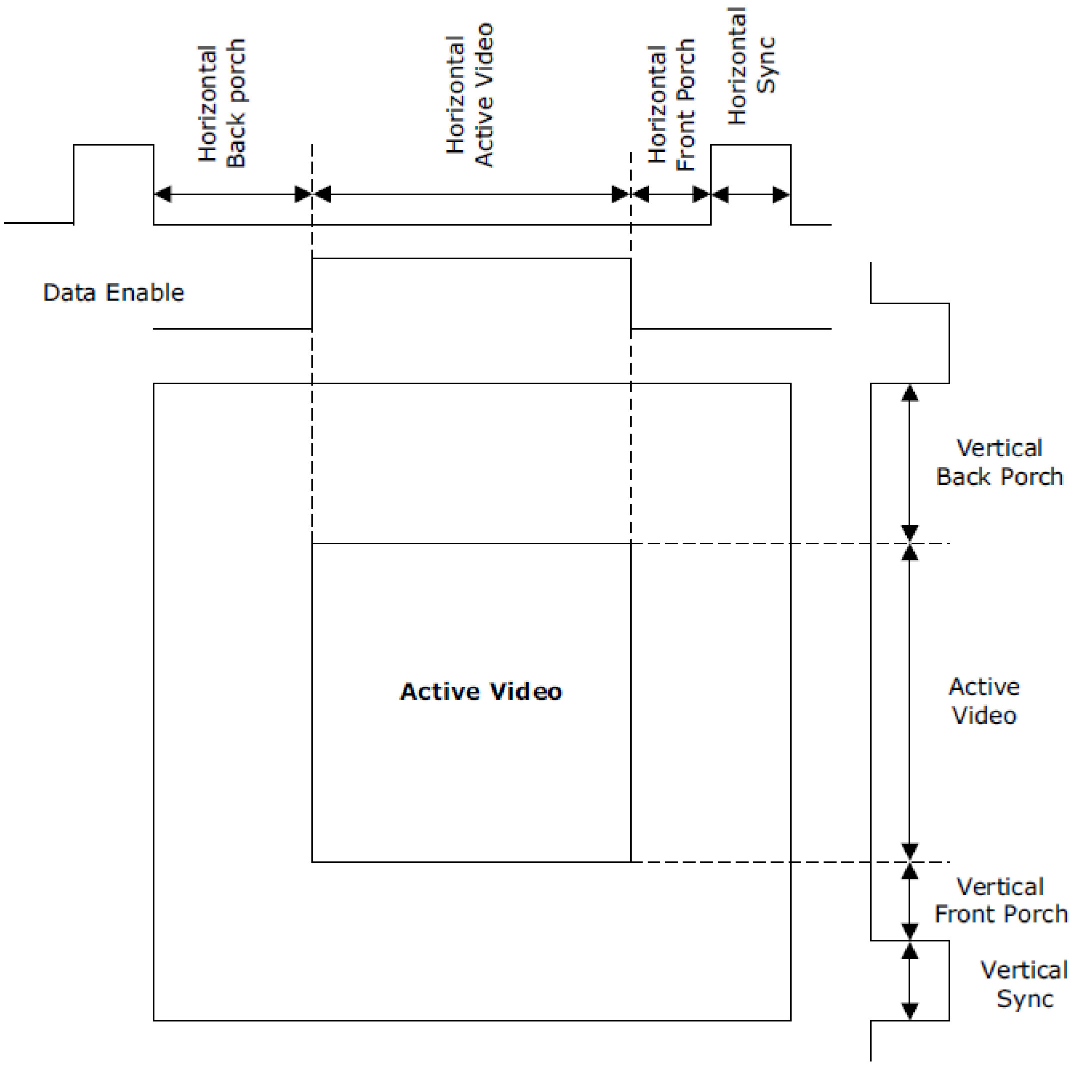
Revision 1.0
Revision 1.0 was the first publication of this document.

Introduction

The display controller generates display synchronization signals based on the display resolution. It generates the horizontal and vertical sync signals, horizontal and vertical active signals, frame end and data enable signals. The input video data is also synchronized with these sync signals. The sync signals along with video data can be fed to a DVI, HDMI, or VGA card that interfaces with the display monitor.

The following figure shows the sync signal waveforms.

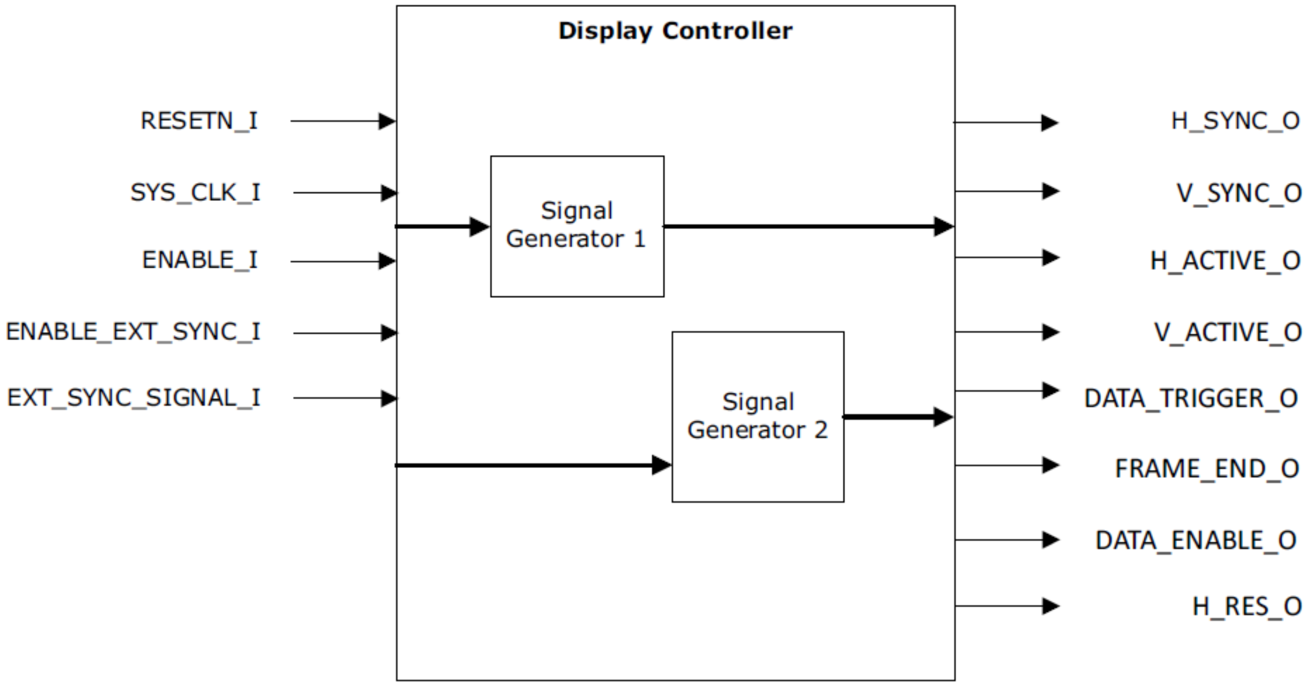
Figure 1 • Sync Signal Waveforms



Hardware Implementation

The following figure shows the display controller block diagram.

Figure 2 • Display Controller Block Diagram



Display controller has following two submodules.

Signal Generator 1

It has one horizontal counter and one vertical counter. The horizontal counter starts counting as soon as the ENABLE_I signal goes high and resets to zero every time when it reaches total horizontal count (Horizontal Resolution + Horizontal Front Porch + Horizontal back porch + Horizontal Sync Width). The vertical counter starts counting after end of first horizontal line and resets to zero when it reaches total vertical count (Vertical Resolution + Vertical Front Porch + Vertical back porch + Vertical Sync Width).

The DATA_TRIGGER_O signal is generated by signal generator1 based on the horizontal and vertical counter values.

Signal Generator 2

It has also one horizontal counter and one vertical counter. The horizontal counter starts counting when EXT_SYNC_SIGNAL_I goes high and resets to zero every time when it reaches total horizontal count (Horizontal Resolution + Horizontal Front Porch + Horizontal back porch + Horizontal Sync Width). The vertical counter starts counting when the horizontal counter reaches the total horizontal count for the first time. The vertical counter resets to zero when it reaches total vertical count (Vertical Resolution + Vertical Front Porch + Vertical back porch + Vertical Sync Width). The H_SYNC_O, V_SYNC_O, H_ACTIVE_O, V_ACTIVE_O and DATA_ENABLE_O signals are generated by signal generator2 based on the horizontal and vertical counter values.

Inputs and Outputs

Ports

The following table lists the description of input and output ports. Table 1 • Inputs and Outputs of Display Controller

Signal Name	Direction	Width	Description
RESETN_I	Input	1 bit	Active low asynchronous reset signal to design
SYS_CLK_I	Input	1 bit	System clock
ENABLE_I	Input	1 bit	Enables display controller
ENABLE_EXT_SYNC_I	Input	1 bit	Enables external syncing
EXT_SYNC_SIGNAL_I	Input	1 bit	External sync reference signal. It is used to compensate the de lay generated by the intermediate blocks. Its timing characteristics should match that of video resolution (set using G_VIDEO_FORMAT) selected.
H_SYNC_O	Output	1 bit	Active horizontal sync pulse
V_SYNC_O	Output	1 bit	Active vertical sync pulse
H_ACTIVE_O	Output	1 bit	Horizontal active video period
V_ACTIVE_O	Output	1 bit	Vertical active video period
DATA_TRIGGER_O	Output	1 bit	Data trigger. It is used to trigger DDR read operation
FRAME_END_O	Output	1 bit	Goes high for one clock after every frame end
DATA_ENABLE_O	Output	1 bit	Data enable for HDMI
H_RES_O	Output	16 bit	Horizontal resolution

Configuration Parameters

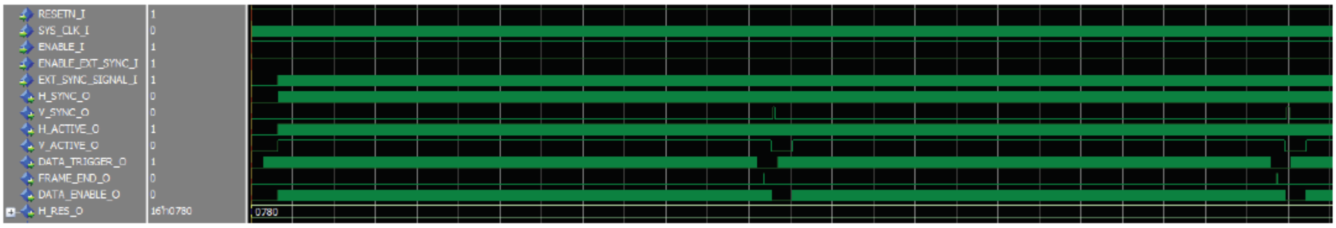
The following table lists the description of the generic configuration parameters used in the hardware implementation of display controller, which can vary based on the application requirements.

Table 2 • **Configuration Parameters**

Name	Description
G_VIDEO_FORMAT	Video format selection—1280x720, 1920x1080, and 3840x2160.
G_PIXELS_PER_CLK	Number of Pixels per clock selection—1 and 4. Selecting 4 changes the horizontal timing to 1/4 of standard definition.

Timing Diagrams

Figure 3 • **Frame End and Vertical Sync Signal**



The following figure shows the timing diagram for video data and data valid input signals received from the memory controller.

Figure 4 • **Frame End and Vertical Sync Detailed View**

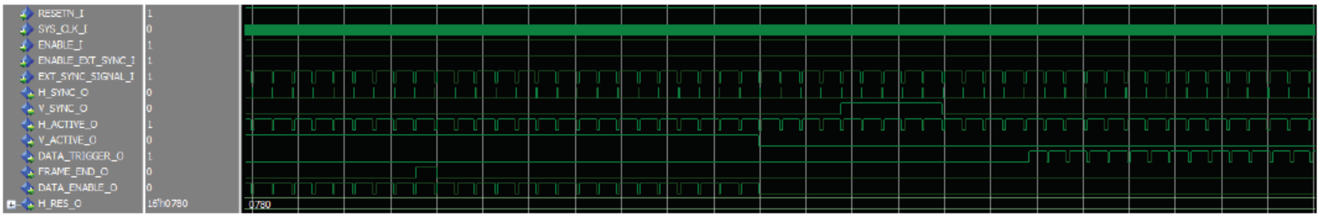
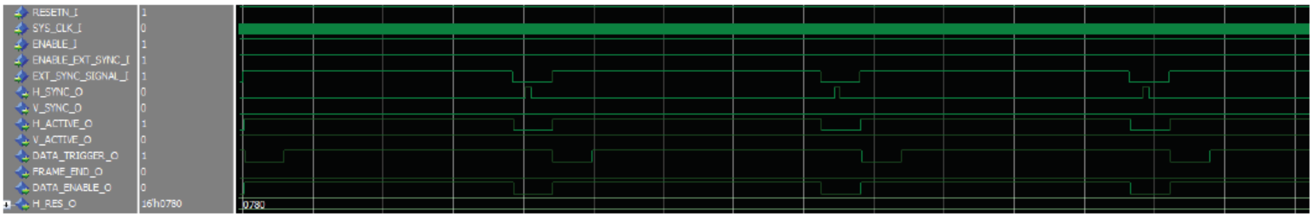


Figure 5 • **External Sync Signal, Horizontal Sync Signal Data Trigger and Data Enable**



Testbench Simulation

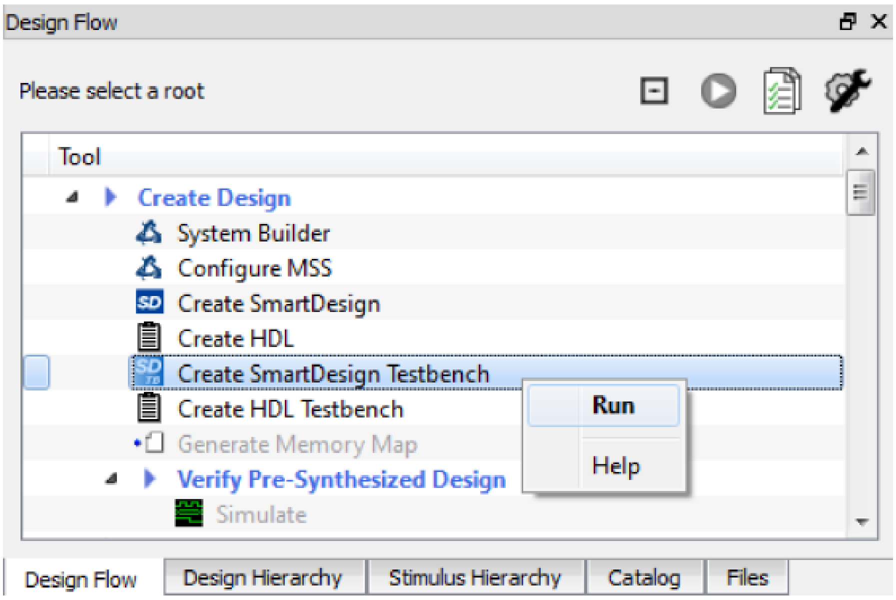
A testbench is provided to check the functionality of the display controller. The following table lists the parameters that can be configured.

Table 3 • **Testbench Configuration Parameters**

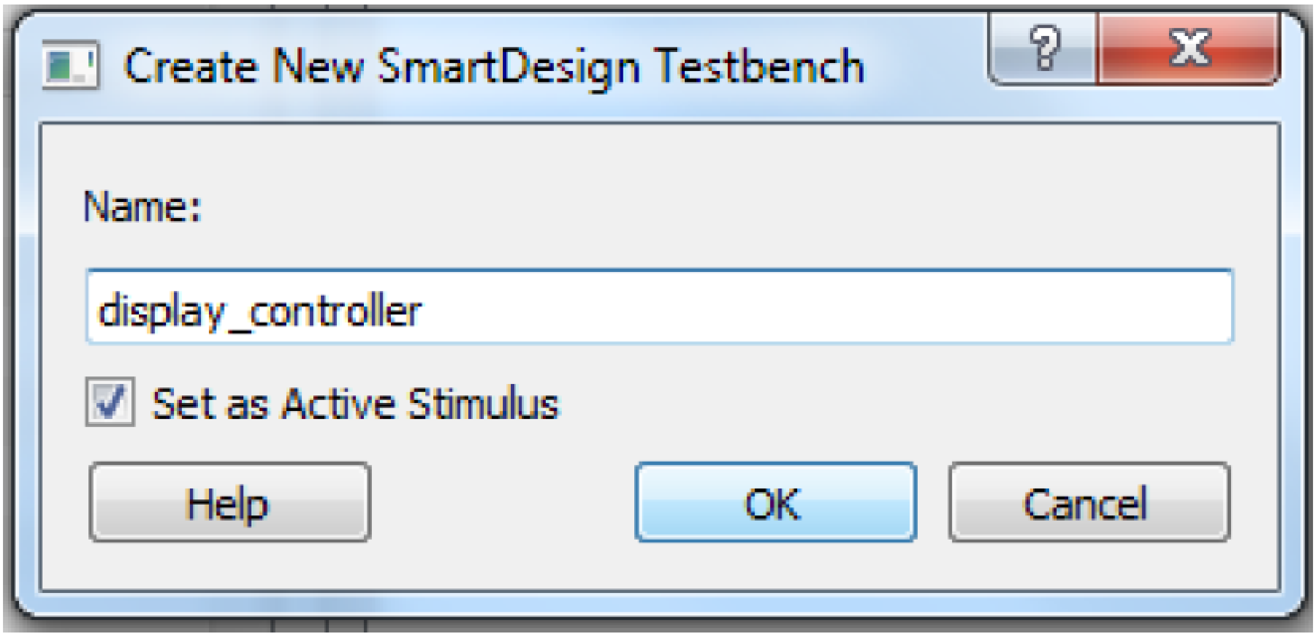
Name	Description
G_VIDEO_FORMAT	Video format selection
G_PIXELS_PER_CLK	Number of pixels per clock selection

The following steps describe how to simulate the core using the testbench.

1. In the Libero SoC Design Flow window, expand Create Design, double-click Create SmartDesign Testbench or right-click Create SmartDesign Testbench and click Run to create a SmartDesign testbench. See the following figure.

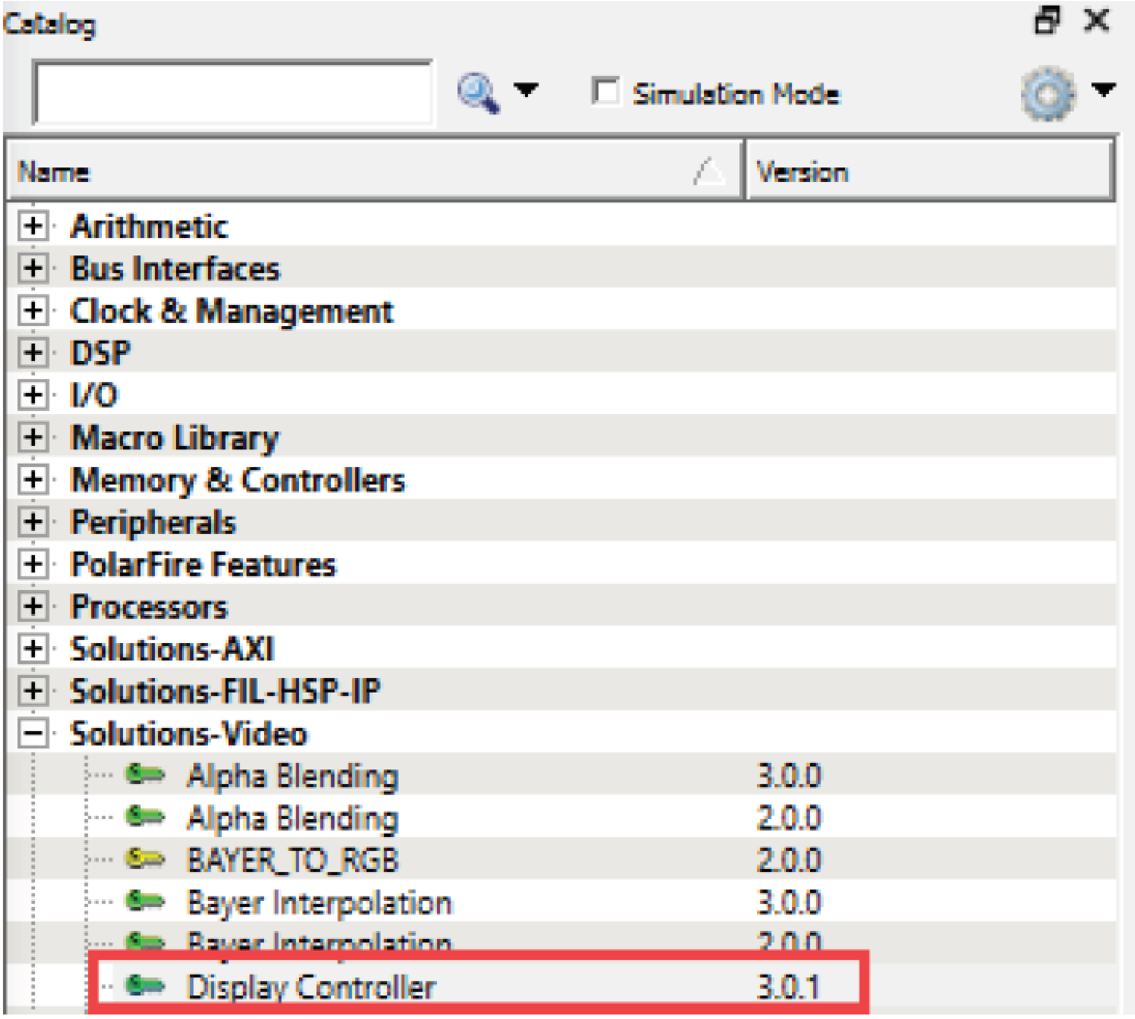


2. Enter a name for the new SmartDesign testbench in the Create New SmartDesign Testbench dialog box and click OK as shown in the following figure.

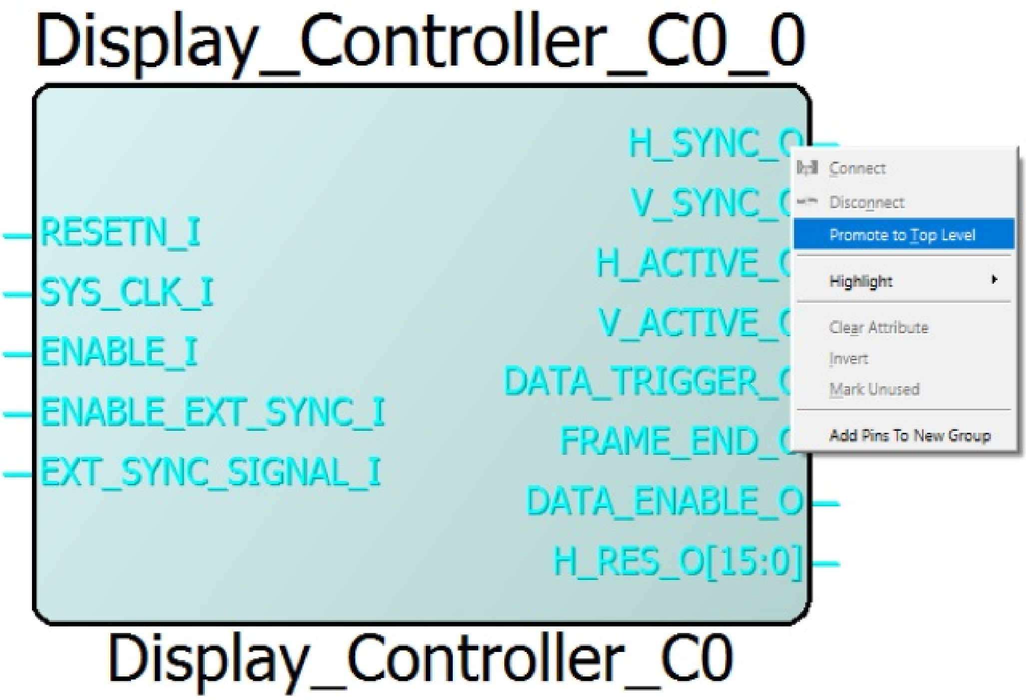


A SmartDesign test bench is created, and a canvas appears to the right of the Design Flow pane.

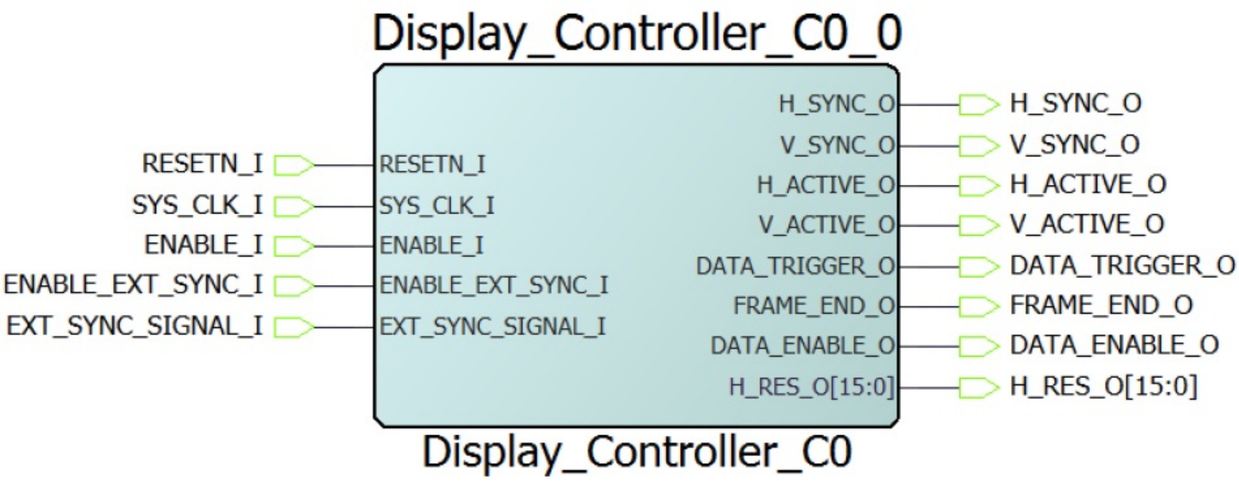
3. In the Libero SoC Catalog (View > Windows > Catalog), expand Solutions-Video and drag-and- drop the Display Controller core onto the SmartDesign testbench canvas, as shown in the following figure.



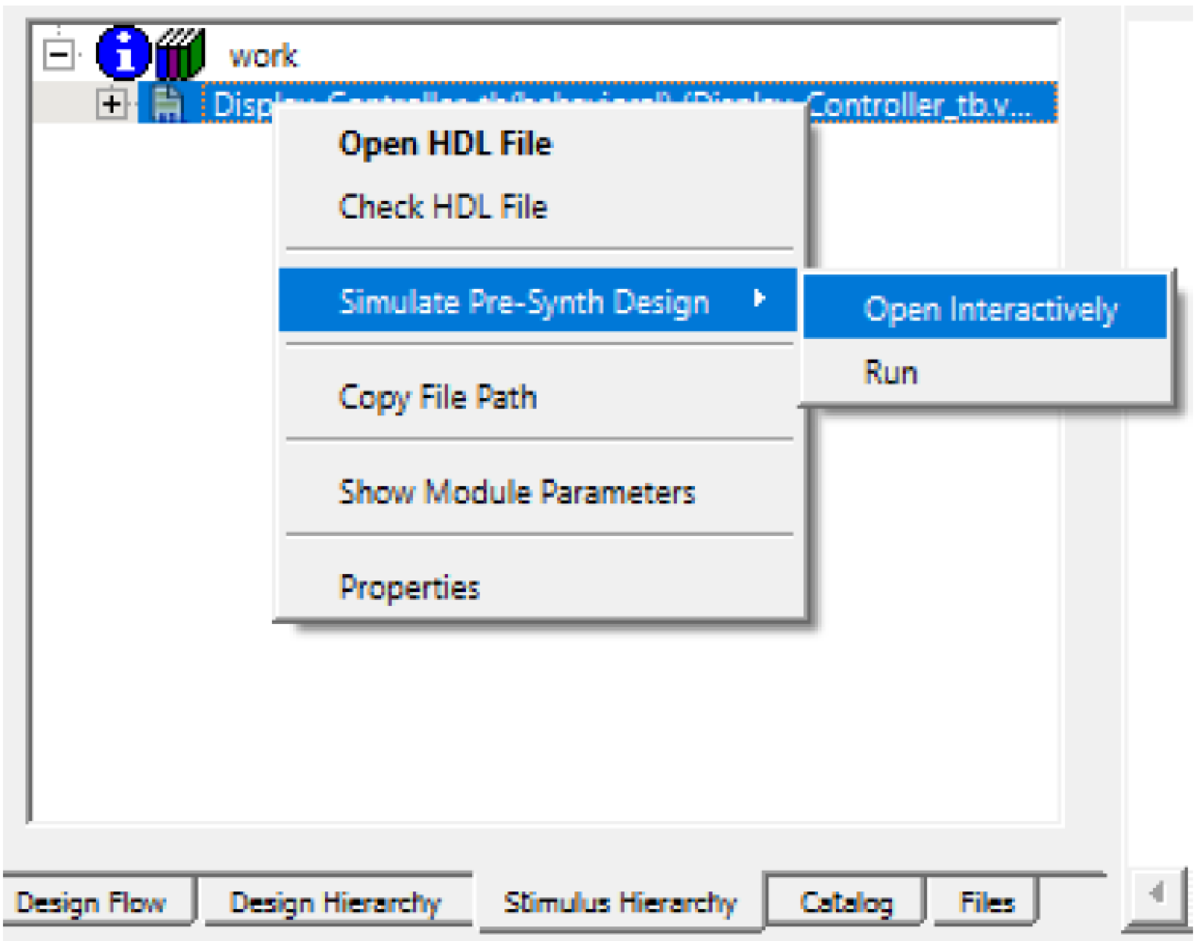
4. Select all the ports, right-click, and select Promote to Top Level, as shown in the following figure.



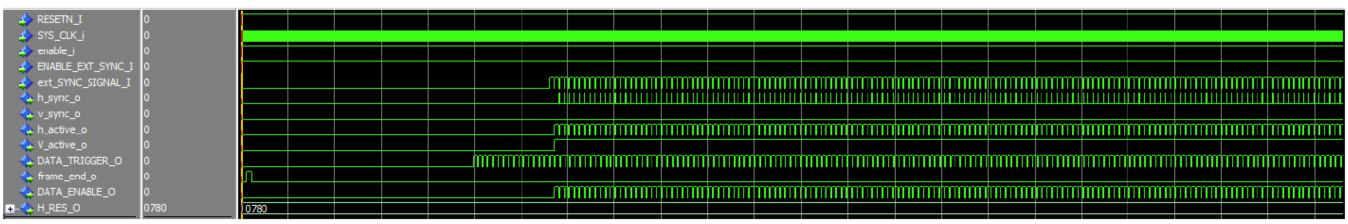
5. Click Generate Component from the SmartDesign toolbar, as shown in the following figure



6. On Stimulus Hierarchy tab, right-click display_controller_test (display_controller_tb.vhd) testbench



The ModelSim tool appears with the test bench file loaded on to it as shown in the following figure



If the simulation is interrupted because of the runtime limit in the DO file, use the run -all command to complete the simulation. After the simulation is completed, the test bench output image file appears in the simulation folder (View > Files > simulation). For more information about updating the testbench parameters, see Table 3, page 6.

Resource Utilization

The display controller is implemented in the SmartFusion2 and IGLOO2 system-on-chip (SoC) FPGA (M2S150T-1FC1152 package) and PolarFire FPGA (MPF300TS – 1FCG1152E Package). The following table lists the resources utilized by the FPGA when G_VIDEO_FORMAT = 1920×1080 and G_PIXELS_PER_CLK = 1.

Resource	Usage
DFFs	79
4LUTs	150
LSRAM	0
MATH	0

Resource	Usage
DFFs	79
4LUTs	149
RAM1Kx18	0
RAM64x18	0
MACC	0

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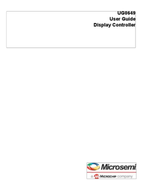
Documents / Resources

	Microsemi UG0649 Display Controller [pdf] User Guide UG0649 Display Controller, UG0649, Display Controller, Controller

References

- Microsemi | Semiconductor & System Solutions | Power Matters