Microsemi UG0596 RTG4 FPGA Power Estimator Software User Guide

UG0596
User Guide
RTG4 FPGA Power Estimator

Contents

UG0596 RTG4 FPGA Power Estimator Software

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to
independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such

information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

About Microsemi
Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets.
Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at **www.microsemi.com**.

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0
Updated for the RTG4 Power Estimator v6a.

1.2 Revision 1.0
This was the first release of this document.

RTG4 FPGA Power Estimator

2.1 Introduction

This user guide describes the RTG4™ Power Estimator for RTG4 Field Programmable Gate Array (FPGA) device families. Early power estimation helps designers to define the architecture within the power budget by applying power saving strategies. It also helps the board designers to design and select the power supplies and heat sink. The Power Estimator workbook is used to estimate the power consumption from early design concept to design implementation. It also provides details about thermal analysis and factors that contribute to power consumption. Device resources, operating frequency, clock resources, toggle rates, and many other parameters are entered into the Power Estimator workbook.
These parameters are then combined with the power models to estimate the power. The power models are based on simulation or characterized device data.
The accuracy of power estimation depends on the data entered into the workbook. Therefore, ensure that realistic data is entered into the design. The actual power depends greatly on actual RTL design, place-and-route, and operating conditions. The Power Estimator result is an early estimation of power consumption rather than measured. Use the SmartPower tool in the Libero® System-on-Chip (SoC) software for accurate and detailed power estimations for designs after place-and-route. Power must be measured during device operation.

2.1.1 Features

The RTG4 Power Estimator has the following features:

- Estimation of power consumption from the design concept phase to implementation.
- Integrated Graphical User Interface (GUI) in a worksheet to initialize the Power Estimator and for I/O Bank voltage settings.
- Power estimation of Active and Standby power modes.
- Power estimation using scenarios.
- Separate worksheet for device features and also a subtotal of power consumed by each device feature.
- Calculation of the Junction temperature and thermal input support.

2.2 Additional Documentation

- RTG4 FPGA Product Brief
- RTG4 FPGA Pin Descriptions
- RTG4 FPGA Fabric User Guide
- RTG4 FPGA High Speed DDR Interfaces User's Guide
- RTG4 FPGA High Speed Serial Interfaces User Guide
- RTG4 FPGA Clocking Resources User Guide
- Libero SoC User Guide

2.3 Launching Power Estimator

This section contains the following sub sections:

2.3.1 System Requirement

- The Power Estimator workbook requires Microsoft Excel. Table 1 shows the supported software.
- Windows operating system.

Table 1 • Supported Software

Supported Software
Microsoft Excel 2003
Microsoft Excel 2007
Microsoft Excel 2010
Microsoft Excel 2013

Note: OpenOffice and Google Docs spreadsheet editors are not supported.

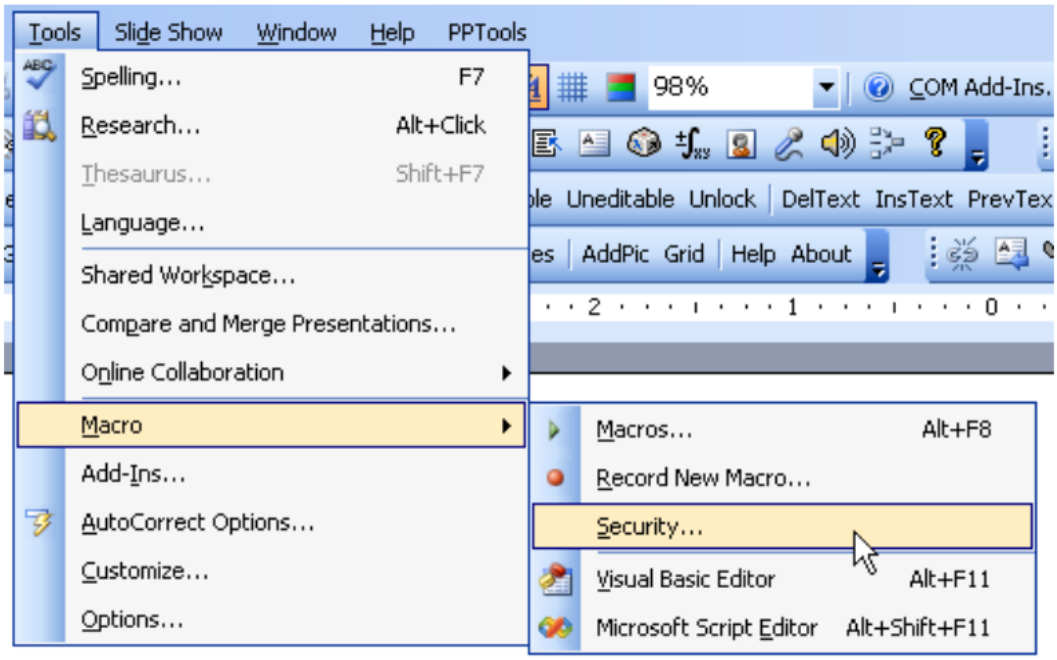
2.3.2 Downloading Power Estimator and Enabling Macros

The Power Estimator workbook for the RTG4 devices latest version can be downloaded from:
https://www.microsemi.com/document-portal/doc_download/1244030-rtg4-power-calculator
The Power Estimator workbook has several built-in macros. By default, the macro security level in Microsoft Excel software is set to High. The macros are automatically disabled if the macro security level is set to High. Ensure that Microsoft Excel settings allow macro executions for the Power Estimator workbook to function properly.
The following sections describe how to change the macro security settings in different versions of Microsoft Excel software:

2.3.2.1 Microsoft Excel 2003

1. Open the Power Estimator Excel file and select Tools > Macro > Security from the main menu.

Figure 1 • Macro Security Level Settings in Microsoft Excel 2003

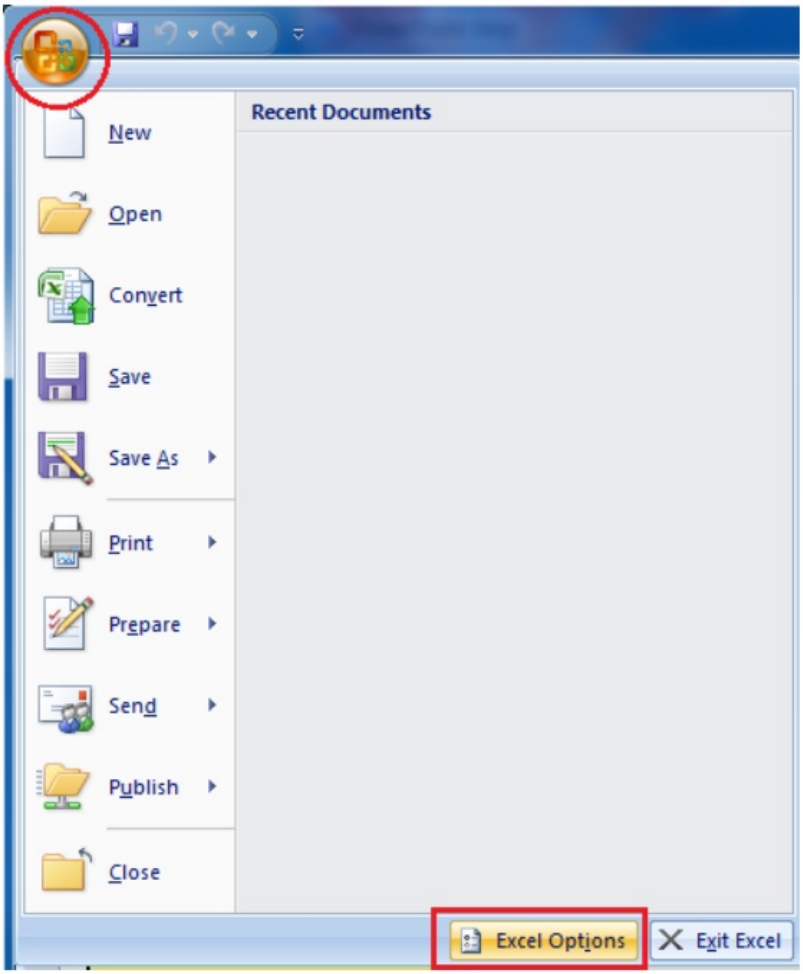


2. From the Macro Security dialogue box, click Security Level tab, and select Medium. Click OK.
3. Close the Power Estimator file and reopen it.
4. Click Enable Macros when prompted to enable macros.

2.3.2.2 Microsoft Excel 2007

1. Open the Power Estimator Excel file and click the Office button at the upper left corner.
2. Click Excel Options.

Figure 2 • Macro Security Level Settings in Microsoft Excel 2007

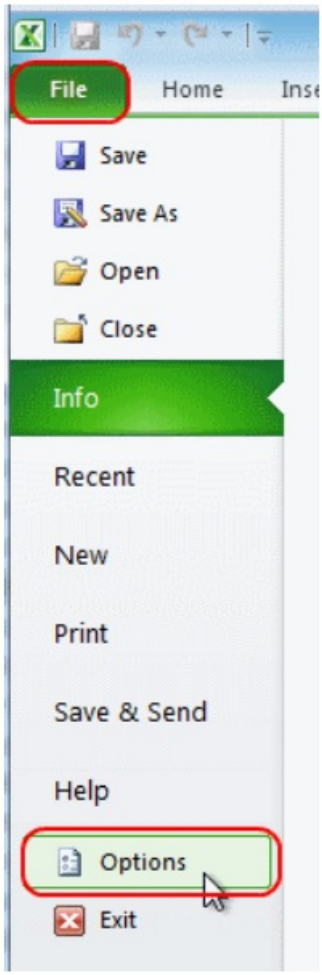


3. Click Trust Center from the left panel.
4. Click Trust Center Settings….
5. From the Trust Center window, click Macro Settings from the left panel. Select Disable all macros with notification and click OK.
6. Close the Power Estimator file and reopen it.
7. A security warning notification appears under the Office ribbon. Click Options.
8. Choose Enable this content in the Microsoft Office Security Options window.

2.3.2.3 Microsoft Excel 2010 and 2013

1. Open the Power Estimator Excel file.
2. Click the File tab and click Options.

Figure 3 • Macro Security Level Settings in Microsoft Excel 2010 and 2013



3. Click Trust Center from the left panel.
4. Click Trust Center Settings….
5. From the Trust Center window, click Macro Settings from the left panel. Select Disable all macros with notification and click OK.
6. Close the Power Estimator file and reopen it.
7. A security warning notification appears under the Office ribbon. Click Options.
8. Choose Enable this content in the Microsoft Office Security Options window.

2.3.3 Minimum Input Requirements

Estimating power for the RTG4 devices is highly dependent on the amount of logic present in the FPGA Fabric. The following are the minimum input requirements for a reasonably accurate power estimation:

- Select a proper device with suitable operating conditions.
- Proper estimation of FPGA Fabric resources (for example, flip-flops, LUTs, LSRAM, uSRAM, MACC, and I/O).
- Proper estimation of high speed serial and DDR interfaces.
- System clock and clock domain.
- Toggle rates of logic and I/Os.
- Enable, write, and read rates for RAMs.

2.4 Power Estimator Excel Workbook

This section describes each worksheet of the RTG4 Power Estimator Excel workbook. Separate worksheets for device features are available. Also, a subtotal of power consumed by each device feature is available. The usage and activity details of the different resources available in the targeted RTG4 device can be entered (for example, flip-flops, LUTs, LSRAM, uSRAM, MACC, I/O, high speed serial and DDR interfaces, system clock and clock domain, toggle rates of logic, and I/Os). The Power Summary section in the Summary worksheet provides the

total power and power breakdown by rail and resource type.

This section contains the following sub sections:

2.4.1 Cell Color-Coding

The RTG4 Power Estimator Excel workbook has several worksheets. The cells of each worksheet are color coded to simplify the data entry and review.
Table 2 lists the cell colors and description.

Table 2 • Cell Color Coding

Cell color	User Action	Description
	Editable	User can enter data
	Non Editable	User cannot enter data
	Read-Only	Calculated values
	Read-Only	Summary values
	Read-Only	Error

2.4.2 Recommended Flow

2.4.2.1 Step – 1: Settings

Select the device, package, temperature grade, operating condition, and thermal inputs settings.

2.4.2.2 Step – 2: Active Mode Configuration

Set up the design specific information that is used to compute the dynamic power.

- FPGA Fabric Components:
- Set up the FPGA Fabric components and their operating frequencies.
- I/Os:
- Set up the I/O technology and their operating frequencies.
- Built-in Blocks (SERDES and FDDR):
- Configure the SERDES and DDR subsystems with appropriate settings.

2.4.2.3 Step – 3: Scenarios

Optional: Update the percentage of time the device must be in a given mode during its operational time (for instance, 50% of the time Active and 50% in Standby).

2.4.2.4 Step – 4: Power Estimation Summary

The power summary section in the Summary worksheet provides the total power and its breakdown based on the power sources and rails. The total power for the scenario is described in Step – 3: Scenarios, page 22.

The following sections describe these steps in detail:

2.5 Step – 1: Settings

Figure 4 shows the Settings section in the Summary worksheet.

Figure 4 • Settings Section in Summary Worksheet

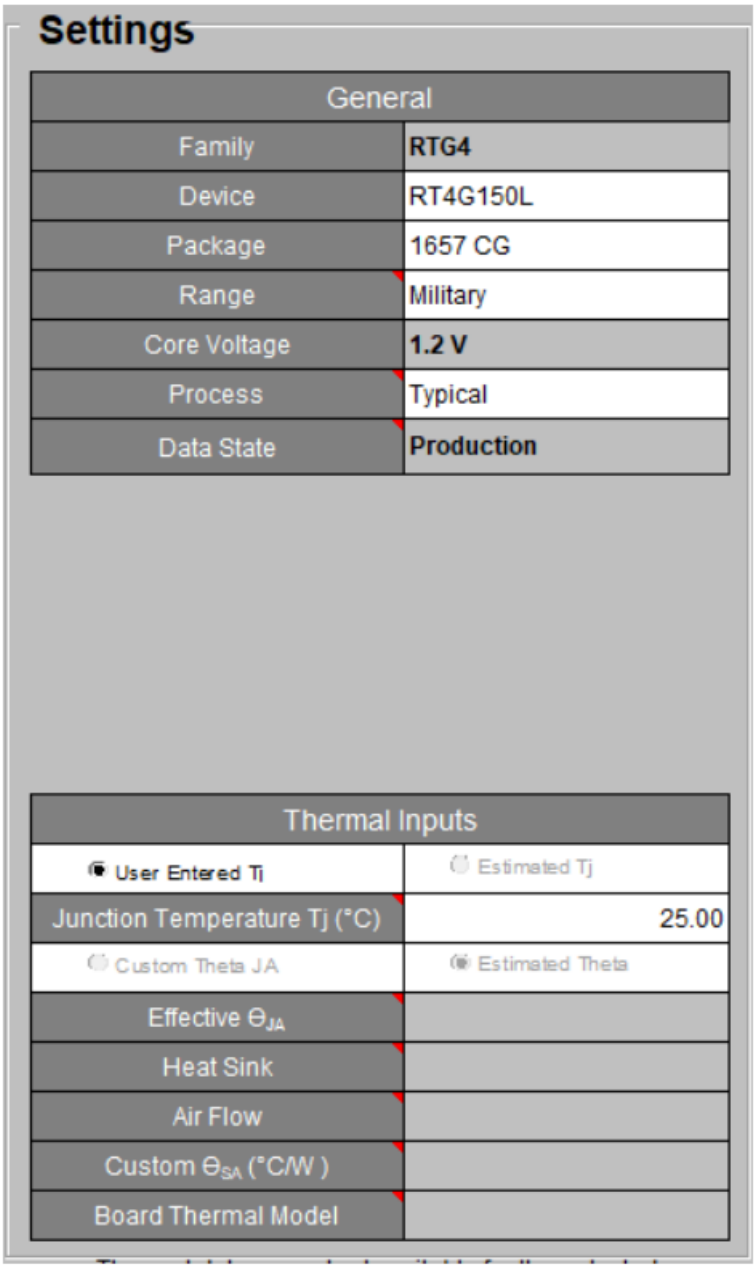


Table 3 shows the General and Thermal Inputs settings in the Settings section of the Summary worksheet. Ensure that you select the device with the appropriate operating conditions.

Parameters	Description
General Settings	

Family	RTG4
Device	Select the device. The following devices are supported: • RT4G150L
Package	Select the package.
Range	Select the product grade. The following grades are available. • E Military Temperature grade for different ranges: • E Military (-55°C to 125°C)
Core Voltage	Core supply voltage (1.2 V)
Process	Select the process. The following conditions are available: • Typical Process accounts for manufacturing process variations that affect power dissipatio n. Typical uses average power dissipation factors for your design. Voltage and Tem perature are controlled independently of the process.
Data State	Advanced: Initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. Preliminary: Information based on simulation and/or initial characterization. The information is b elieved to be correct, but changes are possible. Production: Information that is considered to be final.
Thermal Inputs	
Junction Temperature Tj (°C) **Note:** Thermal data is not yet available. User Entere d TJ option is only support ed.	Enter the Junction Temperature of the device. This field is available only when User Entered TJ option is selected. In this case, ot her thermal input fields are disabled. When Estimated TJ option is selected, the junction temperature is calculated based on the thermal inputs entered.

Ambient Temperature Ta (°C)	Enter the temperature of the air surrounding the device. This field is available only if Estimated TJ option is selected. Valid temperature ranges are: • E Military: -55°C to 125°C When Estimated Theta JA option is selected, this field is used to calculate the junction temperature based on the thermal resistance and power dissipation. When Custom Theta JA option is selected, this field is used to calculate the junction temperature based on the Effective qJA and power dissipation.
Effective qJA	Effective thermal resistance. User selected device, package, airflow, heat sink and board model are used with characterization and simulation data to calculate effective thermal resistance. To enter a custom effective Theta JA, select Custom Theta JA and enter a value, to account for conditions not covered by the available choices or where more extensive thermal modeling has been done. The following fields are disabled when Custom Theta JA is selected and enabled Estimated Theta JA is selected: • E Heat Sink • E Air Flow • E Custom qSA (°C/W) • E Board Thermal Model
Heat Sink	Select one of the following options: • None • Custom • 10 mm-Low Profile • 15 mm-Medium Profile • 20 mm-High Profile This field is enabled only when Estimated TJ and Estimated Theta JA options are selected.
Airflow	Select an ambient airflow in meter per second (m/s): • 1.0 m/s • 2.5 m/s This field is enabled only when Estimated TJ and Estimated Theta JA options are selected. The junction temperature is reduced if the ambient airflow is increased.
Custom qSA (°C/W)	If a custom heat sink is selected, enter the heat sink-to-ambient thermal resistance from the heat sink datasheet. This field is enabled only when Estimated TJ and Estimated Theta JA options are selected.

Board Thermal Model	Select one of the following options: • None (Conservative) • JEDEC (2s2p) This field is enabled only when Estimated TJ and Estimated Theta JA options are s elected. If None (Conservative) option is selected, the thermal model assumes that no heat is dissipated through the board. If JEDEC (2s2p) option is selected, the thermal model assumes that the characteristics is of the JEDEC 2s2p test board specified in standard JESD51-9.

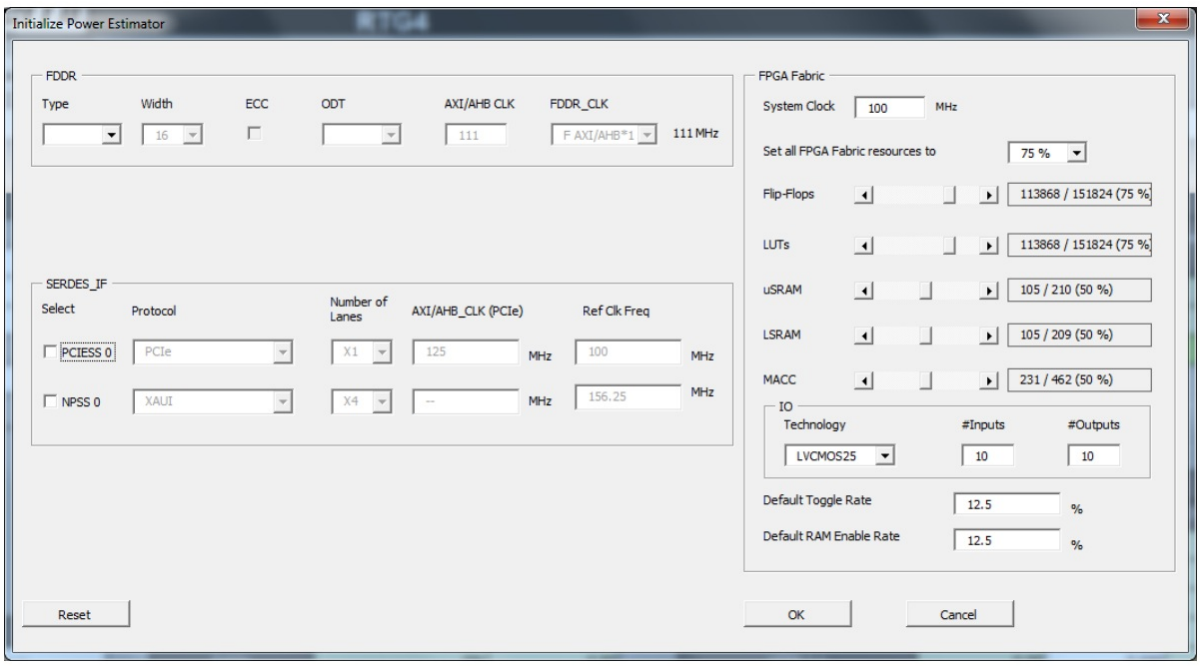
2.6 Step – 2: Active Mode Configuration

In this section, enter design specific information that can be used to compute dynamic power.
It contains the following subsections:

2.6.1 Initialize Power Estimator Wizard

The Summary worksheet has an integrated power estimator wizard. Click Initialize Power Estimator at the top left of the worksheet to invoke the Initialize Power Estimator wizard. This wizard enables the user to select design specific information. Upon running the wizard, it populates the Power Estimator spreadsheet with design specific information and estimates power for the design. Change the wizard populated entries to provide more accurate inputs to the Power Estimator.
Figure 5 shows the Initialize Power Estimator wizard.

Figure 5 • Power Estimator Wizard



The Power Estimator wizard provides following fields depending on the product family selected:

- **FDDR**

Select the memory type, width, ECC, ODT, and FDDR_CLK.

Maximum frequency of FDDR_CLK is 333 MHz.

- **SERDES_IF**

  Select PCIE sub-system (PCIESS), non-PCIE sub-system (NPSS), Protocol, Number of Lanes, AXI/AHB_CLK (PCIe) clock, and Ref Clk Freq.
- **FPGA Fabric**
- **System Clock**

  Specify the Fabric clock frequency. By default, it is set to 100 MHz. Valid entries are between 0 and 300 MHz.
- **Design Utilization**

  Use the drop down menu against Set all FPGA Fabric Resources to set a percentage value for all the resources at one go. A percentage value for each resource to be utilized can be set using the slide bar against the resources.

  The following are the available resources:

  * Flip-Flops

  * LUTs

  * uSRAM

  * LSRAM

  * MACC
- **I/O**

  Select the I/O technology and enter the number of inputs and outputs.
- **Default Toggle Rate**

  Enter a toggle rate in percentage. This toggle rate applies to all logic module and I/Os.
- **Default RAM Enable Rate**

  Enter an enable rate in percentage. This enable rate applies to uSRAM and LSRAM.

Note: When the slider thumb moves between the end points of the slider track, the value is updated in the corresponding text field.
To populate the Power Estimator spreadsheet with the entered values, click OK.

2.6.2 FPGA Fabric Components

This section describes the design of specific information for FPGA Fabric components that are used to calculate dynamic power. The RTG4 Power Estimator workbook provides separate worksheets for each FPGA Fabric component. These worksheets are described in the following subsections:

2.6.2.1 Clock

The RTG4 devices support only global clock networks. Each row in the Clock worksheet represents a separate clock domain.
Enter the following parameters for each clock domain:

- Name
- Clock Frequency (MHz)
- Fanout
- Global Enable Rate

Figure 6 shows the Clock worksheet.
Figure 6 • Clock Worksheet

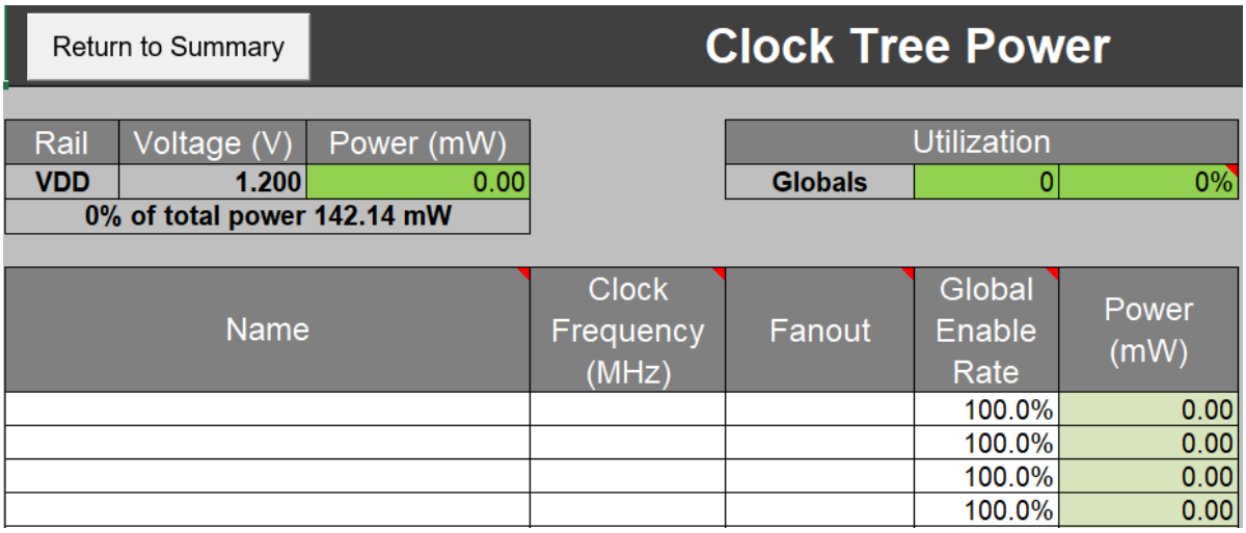


Table 4 shows the parameters to be entered in the Clock worksheet.

Table 4 • Clock Worksheet Parameters

Parameters	Description
Name	Enter a name for each clock domain (optional).
Clock Frequency (MHz)	Enter the clock frequency of the domain. The maximum frequency of the FPGA Fa bric is 300 MHz.
Fanout	Enter the number of registers and other synchronous elements (LSRAM, uSRAM, Math Block, and I/O) clocked.
Global Enable Rate	Enter the average percentage of time that clock enable is high for each clock doma in.

For more information about the clock networks of the supported device families, refer to RTG4 FPGA **Clocking Resources User Guide**.

2.6.2.2 Logic

Each row in the Logic worksheet represents a separate clock domain.
Enter the following parameters for each clock domain:

- Name
- Clock Frequency (MHz)
- Number of Registers
- Number of LUTs

- Fanout
- Toggle Rate

  Figure 7 shows the Logic worksheet.

Figure 7 • Logic Worksheet

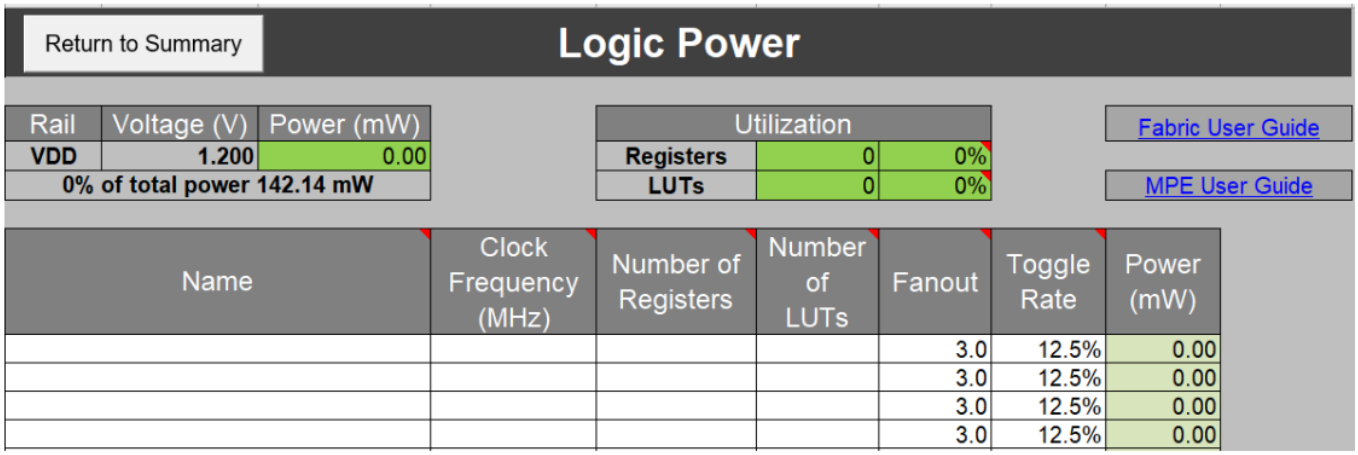


Table 5 shows the parameters to be entered in the Logic worksheet.

Table 5 • Logic Worksheet Parameters

Parameters	Description
Name	Enter a name for each clock domain (optional).
Clock Frequency (MHz)	Enter the clock frequency of the domain. The maximum frequency of the FPGA Fa bric is 300 MHz.
Number of Registers	Enter the number of registers for each clock domain.
Number of LUTs	Enter the number of regular LUT (combinatorial) modules.
Average Fanout	Enter the average fanout of the nets driven by the registers and LUTs.
Toggle Rate	Enter the toggle rate of register and LUTs outputs.

For more information about the Logic Element of the supported device families, refer to RTG4 FPGAFabric User Guide.

2.6.2.3 LSRAM

Each row in the LSRAM worksheet represents a separate clock domain.
Enter the following parameters for each clock domain:

- Name
- Number of LSRAM blocks
- Port A – Clock Frequency (MHz)
- Port A – Write Rate
- Port A – Enable Rate
- Port B – Clock Frequency (MHz)

- Port B – Write Rate
- Port B – Enable Rate

Figure 8 shows the LSRAM worksheet.
Figure 8 • LSRAM Worksheet

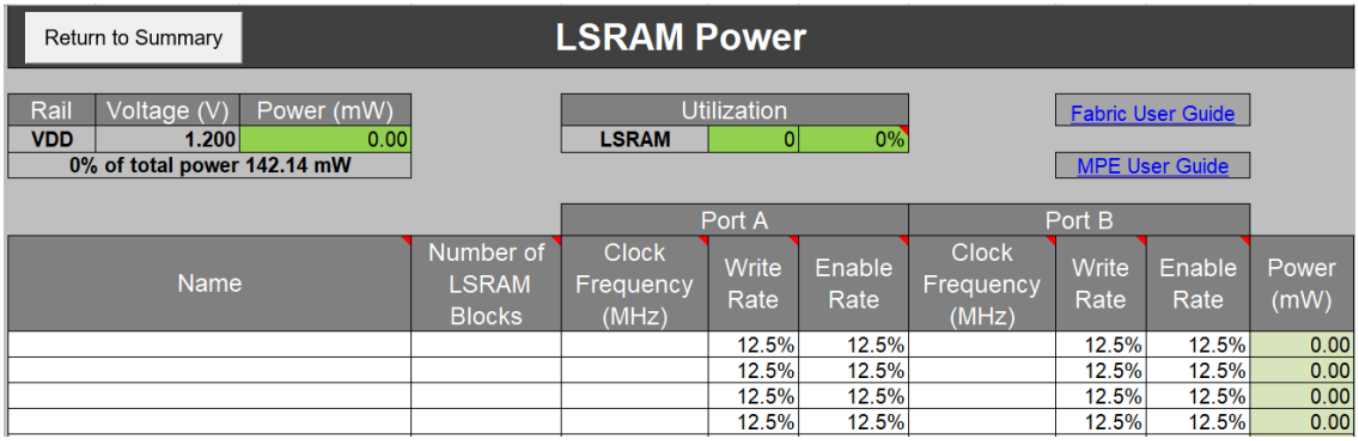


Table 6 shows the parameters to be entered in the LSRAM worksheet.

Table 6 • LSRAM Worksheet Parameters

Parameters	Description
Name	Enter the name of the module or clock domain containing the LSRAM.
Number of LSRAM blocks	Enter the number of LSRAM blocks.
Port A – Clock Frequency (MHz)	Enter the clock frequency for Port A of the LSRAM blocks. It supports a maximum f requency of up to 300 MHz.
Port A – Write Rate	Enter the percentage of time that Port A is used for write operations. The remainin g time is used for read operations.
Port A – Enable Rate	Enter the percentage of time that Port A is enabled.
Port B – Clock Frequency (MHz)	Enter the clock frequency for Port B of the LSRAM blocks. It supports a maximum f requency of up to 300 MHz.
Port B – Write Rate	Enter the percentage of time that Port B is used for write operations. The remainin g time is used for read operations.
Port B – Enable Rate	Enter the percentage of time that Port B is enabled.

For more information about the LSRAM of the supported device families, refer to RTG4 FPGA Fabric User Guide.

2.6.2.4 uSRAM

Each row in the uSRAM worksheet represents a separate clock domain.
Enter the following parameters for each clock domain:

- Name
- Number of uSRAM blocks
- Port A – Read Clock Frequency (MHz)

- Port A – Enable Rate
- Port B – Read Clock Frequency (MHz)
- Port B – Enable Rate
- Port C – Write Clock Frequency (MHz)
- Port C – Enable Rate

Figure 9 shows the uSRAM worksheet.

Figure 9 • uSRAM Worksheet

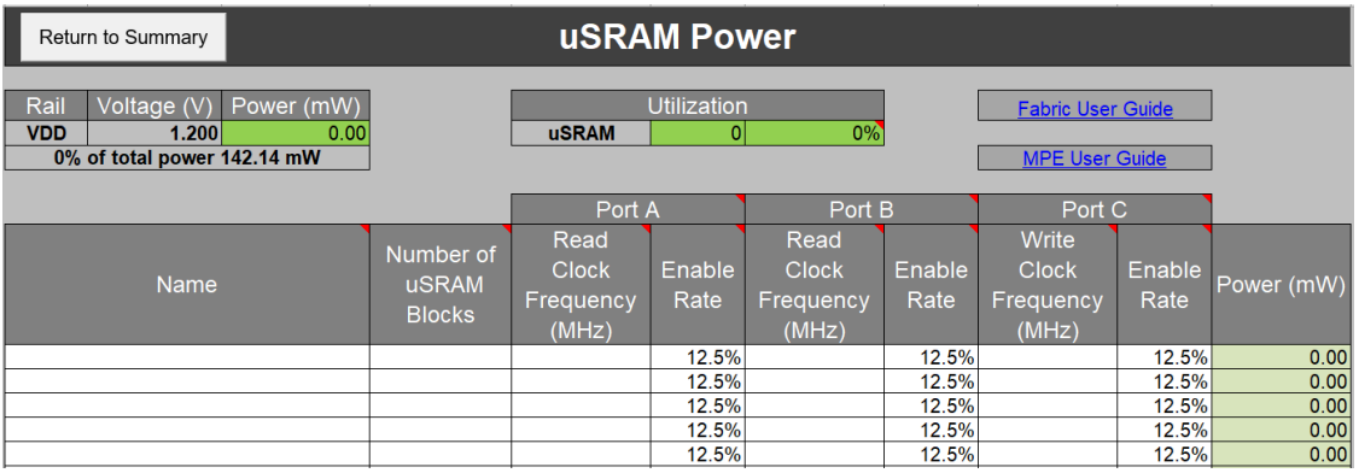


Table 7 shows the parameters to be entered in the uSRAM worksheet.

Table 7 • uSRAM Worksheet Parameters

Parameters	Description
Name	Enter the name of the module or clock domain containing the uSRAM.
Number of uSRAM blocks	Enter the number of uSRAM blocks.
Port A – Read Clock Frequency (MHz)	Enter the read clock frequency for Port A of the uSRAM blocks. It supports a maximum frequency of up to 300 MHz.
Port A – Enable Rate	Enter the percentage of time that Port A is enabled.
Port B – Read Clock Frequency (MHz)	Enter the read clock frequency for Port B of the uSRAM blocks. It supports a maximum frequency of up to 300 MHz.
Port B – Enable Rate	Enter the percentage of time Port B is enabled.
Port C – Write Clock Frequency (MHz)	Enter the write clock frequency for Port C of the uSRAM blocks. It supports a maximum frequency of up to 300 MHz.
Port C – Enable Rate	Enter the percentage of time that Port C is enabled.

For more information about the uSRAM of the supported device families, refer to RTG4 FPGA Fabric User Guide.

2.6.2.5 Math Block

Each row in the Math Block worksheet represents a separate clock domain.
Enter the following parameters for each clock domain:

- Name
- Clock Frequency (MHz)
- Number of Math Blocks
- Data Toggle Rate

Figure 10 shows the Math Block worksheet.
Figure 10 • Math Block Worksheet

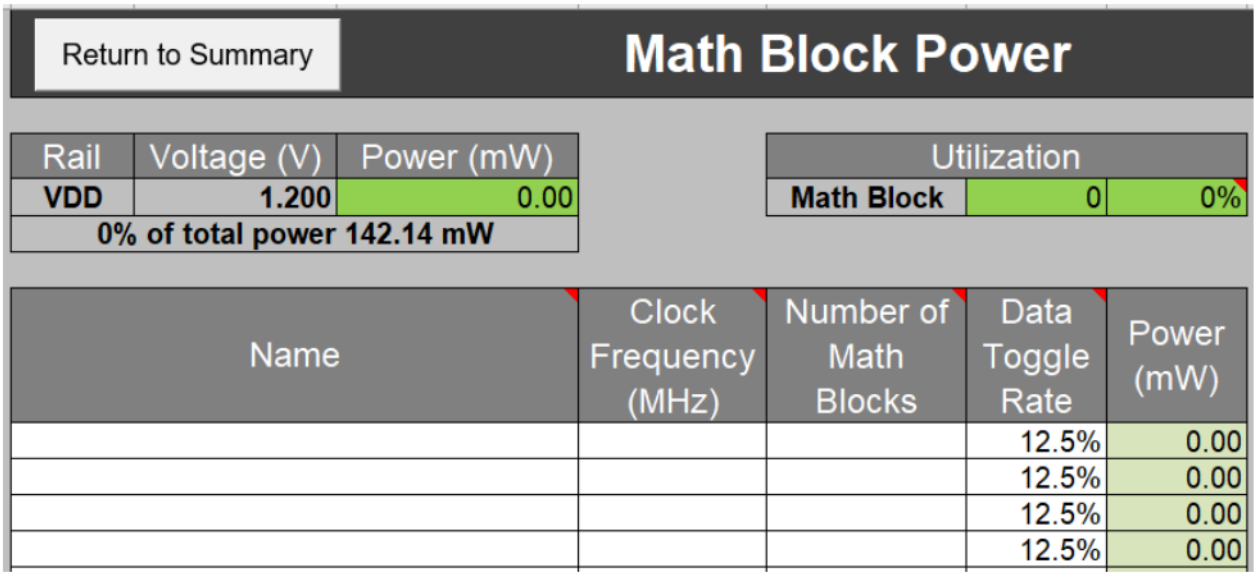


Table 8 lists the parameters to be entered in the Math Block worksheet.

Table 8 • Math Block Worksheet Parameters

Parameters	Description
Name	Enter the name of the module or clock domain containing Math Block.
Clock Frequency (MHz)	Enter the clock frequency of the domain. The maximum frequency of the Math Block is 300 MHz.
Number of Math Blocks	Enter the number of math blocks for each clock domain.
Data Toggle Rate	Enter the average data bus toggle rate.

For more information about the Math Block of the supported device families, refer to RTG4 FPGA Fabric User Guide.

2.6.2.6 CCC

The RTG4 devices have eight CCCs. Each CCC enables flexible clocking schemes for the logic implemented in the FPGA Fabric and can provide the base clock for on-chip hard IP blocks such as FDDR and SERDESIF.
Enter the following parameters for each CCC:

- Name
- Reference Clock Frequency (MHz)
- PLL Output Frequency (MHz)
- Output1 Frequency (MHz)
- Output2 Frequency (MHz)

- Output3 Frequency (MHz)
- Output4 Frequency (MHz)

Figure 11 shows the CCC Power section in the CCC worksheet.
Figure 11 • CCC Power Section

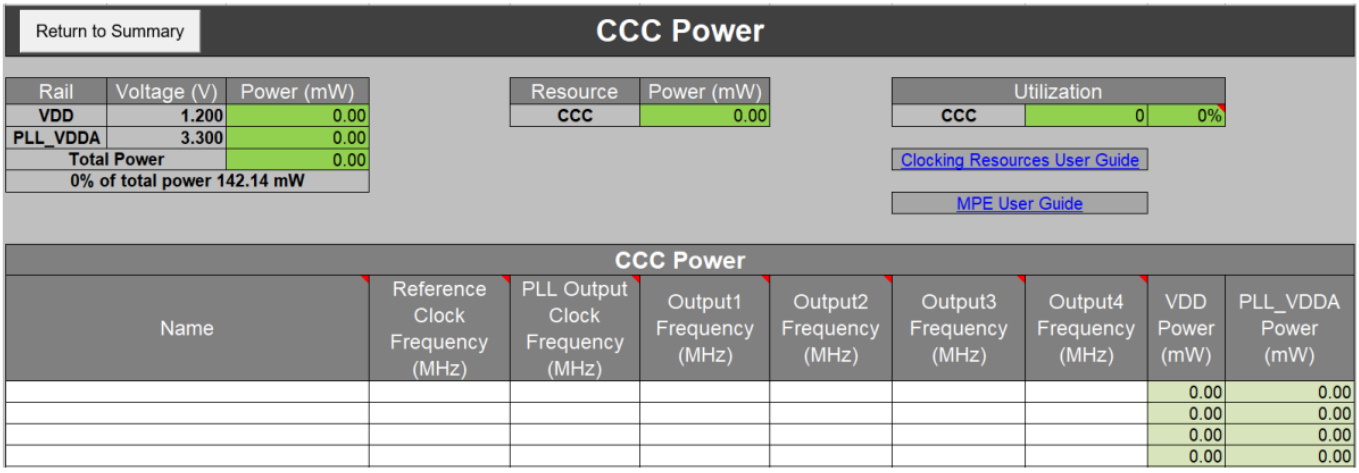


Table 9 shows the parameters to be entered in the CCC Power section of the CCC worksheet.
Table 9 • CCC Section Parameters

Parameters	**Description**
Name	Enter the name of the CCC module.
Reference Clock Frequency (MHz)	Enter the reference clock frequency.
PLL Output Frequency (MHz)	Enter the PLL output frequency.
Output1 Frequency (MHz)	Enter the output1 (GL0/Y0) frequency.
Output2 Frequency (MHz)	Enter the output2 (GL1/Y1) frequency.
Output3 Frequency (MHz)	Enter the output3 (GL2/Y2) frequency.
Output4 Frequency (MHz)	Enter the output4 (GL3/Y3) frequency.

For more information about the CCC of the supported device families, refer to RTG4 FPGA Clocking Resources User Guide.

2.6.3 I/O

Design specific information is entered in the I/O worksheet for the I/Os used to calculate dynamic power.
Each row represents a clock frequency and an I/O domain.
Enter the following parameters for each row:

- Name
- Bank Type
- I/O standard
- I/P Pins
- O/P Pins
- Bidir Pins

- ODT
- Output Drive (mA)
- Output Load (pF)
- Clock (MHz)
- Data Rate
- Toggle Rate
- Output Enable
- ODT Enable

Figure 12 shows the I/O worksheet.

Figure 12 • I/O Worksheet

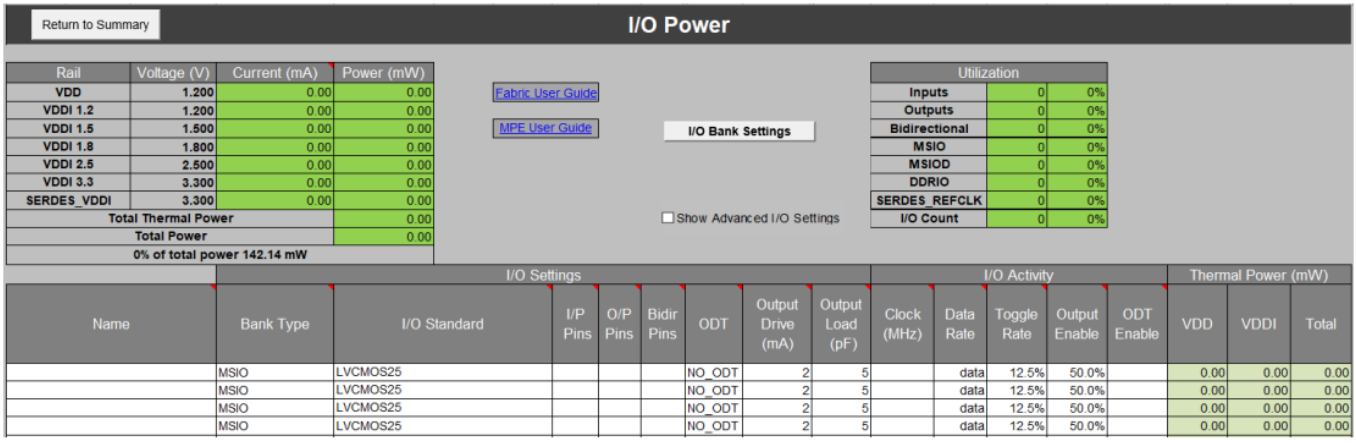


Table 10 shows the parameters to be entered in the I/O worksheet. The advanced I/O settings, Schmitt trigger, Pre-emphasis, and Slew are not visible by default. Select Show Advanced I/O Settings to unhide these columns.

Table 10 • I/O Worksheet Parameters

Parameters	Description	
Name	Enter a name for each I/O, bus or module.	
I/O Settings	Bank Type	Select the bank type. Supports the followings types of banks: •MSIO •MSIOD •DDRIO
	I/O standard	Select the appropriate I/O standard.
	UP Pins	Enter the number of input pins or differential pair used for each I/O, bus or module. The differential pair must be considered as a single pin.
	0/P Pins	Enter the number of output pins or differential pair used for each I/O, bus or module. The differential pair must be considered as a single pin.
	Bidir Pins	Enter the number of bidirectional pins or differential pair used for each I/O, bus or module. The differential pair must be considered as single pin.
	ODT	Select the Input On-die termination impedance.
	Output Drive (mA)	Select the output drive current.
	Output Load (p F)	Enter the board and other external capacitance.

Table 10 • I/O Worksheet Parameters (continued)

Parameters	Description	
I/O Activity	Clock (MHz)	Enter the clock frequency of the domain. It supports a maximum frequency of up to 300 MHz.
	Data Rate	For I/0s used as clocks, select clock as Data Rate. For others, select data.
	Toggle Rate	Enter the average percentage of input, output, and bidirectional pins toggling.
	Output Enable	Enter the percentage of time output pins are enabled. For bidirectional I/Os the input pins are active when the output pins are disabled.
	ODT Enable	ODT Enable is applicable only: •For DDRIO Inputs and Bidirectional pins (if they are connected for FDDR or MDDR) •For the standards: LPDDR, SSTL18, and SSTL15 •If ODT is enabled

For more information about the I/Os of the supported device families, refer to RTG4 FPGA Fabric User Guide.

2.6.4 Built-in Blocks

Design specific information for built-in blocks (SERDES and FDDR) are entered to calculate the dynamic power. This section contains the following subsections:

- SERDES, page 19
- FDDR, page 21

2.6.4.1 SERDES

The RTG4 devices have up to 6 SERDES blocks (2 PCIESS and 4 NPSS). It depends on the device selected. Each row in the SERDES worksheet represents a single (X1) or multiple (X2/X4) SERDES lane.
Enter the following parameters for each SERDES block:

- Name
- Location
- Protocol
- Number of Lanes
- Speed (Gbps)
- PCIe F AXI/AHB (MHz)
- Data Rate (Mbps)

Figure 13 shows the SERDES worksheet.

Figure 13 • SERDES Worksheet

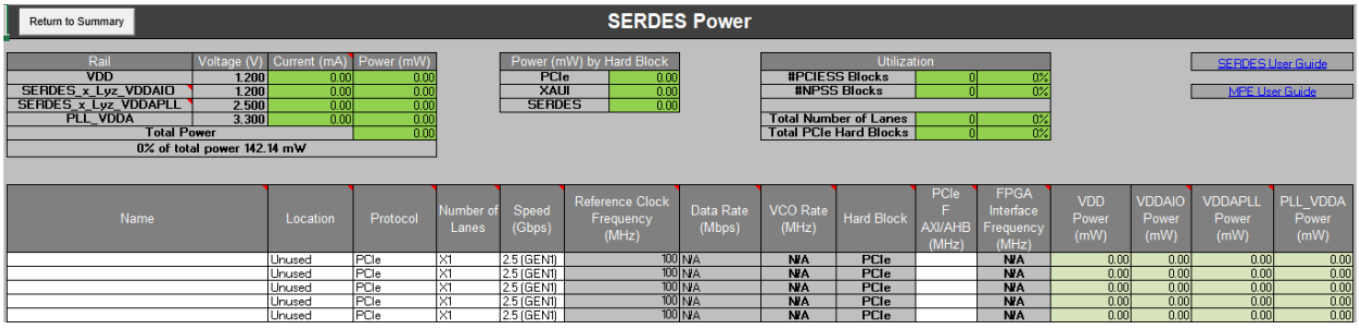


Table 11 shows the parameters to be entered in the SERDES worksheet.

Table 11 • SERDES Worksheet Parameters

Parameters	Description
Name	Enter a name for each SERDES block. Name is optional. Each SERDES block can be configured as X1, X2, or X4 lanes. Configurations can be: •Four X1s •two X2s, or •single X4 Depending on the configuration of lanes in SERDES block, the number of rows varies.
Location	Select the SERDES location. Each SERDES can use up to 4 lanes and it depends on the device selected. When NPSS is selected, only non PCIe protocols (XAUI and EPCS) are available in the protocol column. When PCIESS is selected, all protocols (PCIe, XAUI, and EPCS) are available.
Protocol	Select the protocol. It supports PCIe, XAUI, and EPCS protocols. Figure 14 shows the supported speed list when EPCS protocol is chosen. Custom speed and data width can be selected from the Data Rate (Mbps) drop-down list. VCO Rate and FPGA Interface Frequencies are populated based on the data rate selected.
Number of Lanes	Select the number of lanes. It supports X1, X2, and X4.
Speed (Gbps)	Select the data rate for the selected protocol.
PCIe F AXI/AHB (MHz)	Enter the clock frequency of the AXI/AHB interface. It supports a maximum frequency of up to 200 MHz.
Data Rate (Mbps)	Select the custom speed and data width. This field is enabled only when EPCS protocol is selected.
Reference Clock Frequency (MHz)	This is a fixed value for all protocols except EPCS custom speed. In this case, enter any value between 100 MHz and 160 MHz.
VCO Rate (MHz)	Read-only fixed value for all protocols except EPCS custom speed. The displayed values are computed and updated based on the Reference Clock Frequency and Data Rate.

Figure 14 • Custom EPCS Speed

Location	Protocol	Number of Lanes	Speed (Gbps)	Reference Clock Frequency (MHz)	Data Rate (Mbps)	VCO Rate (MHz)
Unused	PCIe	X1	2.5 (GEN1)	100	N/A	**N/A**
Unused	PCIe	X1	2.5 (GEN1)	100	N/A	**N/A**
Unused	PCIe	X1	2.5 (GEN1)	100	N/A	**N/A**
Unused	PCIe	X1	2.5 (GEN1)	100	N/A	**N/A**
Unused	PCIe	X1	2.5 (GEN1)	100	N/A	**N/A**

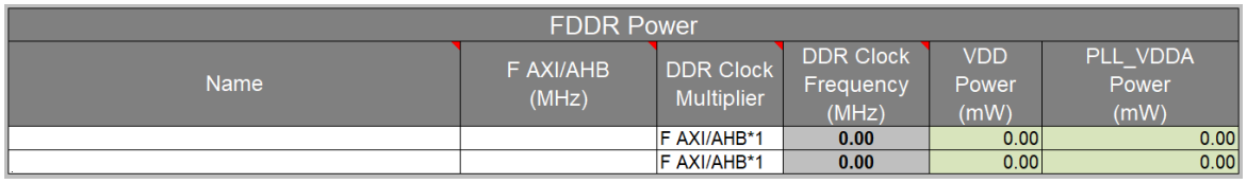
For more information about the SERDES of the supported device families, refer to RTG4 FPGA High Speed Serial Interfaces User Guide.

2.6.4.2 FDDR

Figure 15 shows the FDDR Power section in the FDDR worksheet. Enter the following parameters for FDDR:

- Name
- F AXI/AHB (MHz)
- DDR Clock Multiplier

Figure 15 • FDDR Power Section



FDDR Power					
Name	F AXI/AHB (MHz)	DDR Clock Multiplier	DDR Clock Frequency (MHz)	VDD Power (mW)	PLL_VDDA Power (mW)
		F AXI/AHB*1	0.00	0.00	0.00
		F AXI/AHB*1	0.00	0.00	0.00

Table 12 shows the parameters to be entered in the FDDR Power section of the FDDR worksheet.

Table 12 • FDDR Power Section Parameters

Parameters	Description
Name	Enter the name of the module containing FDDR.
F AXI/AHB (MHz)	Enter the clock frequency of AXI/AHB interface. It supports a maximum frequen cy of up to 200 MHz.
DDR Clock Multiplier	Select the frequency multiplication factor of DDR. DDR clock frequency (FDDR_CLK) must be less than 334 MHz (for example, if F AXI/AHB is 167, DDR clock multiplier must not be more than F AXI/AHB*2).

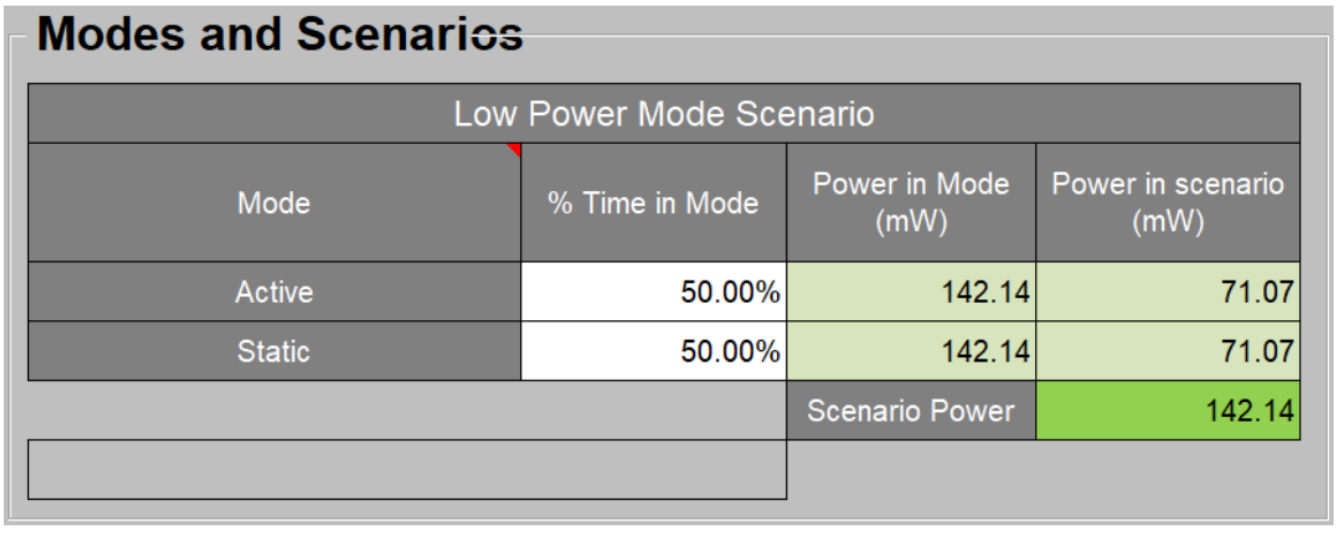
For more information about FDDR, refer to RTG4 FPGA High Speed DDR Interfaces User Guide.

2.7 Step – 3: Scenarios

In this section, enter the device operational modes during its operational time, for instance, 50% of the time Active and 50% in Standby. Enter the percentage of time the device is expected to be in Active and Standby modes. This section is available in the Summary worksheet. It is optional to provide these details.

Figure 16 shows the Modes and Scenarios section in the Summary worksheet.

Figure 16 • Modes and Scenarios Section



Modes and Scenarios

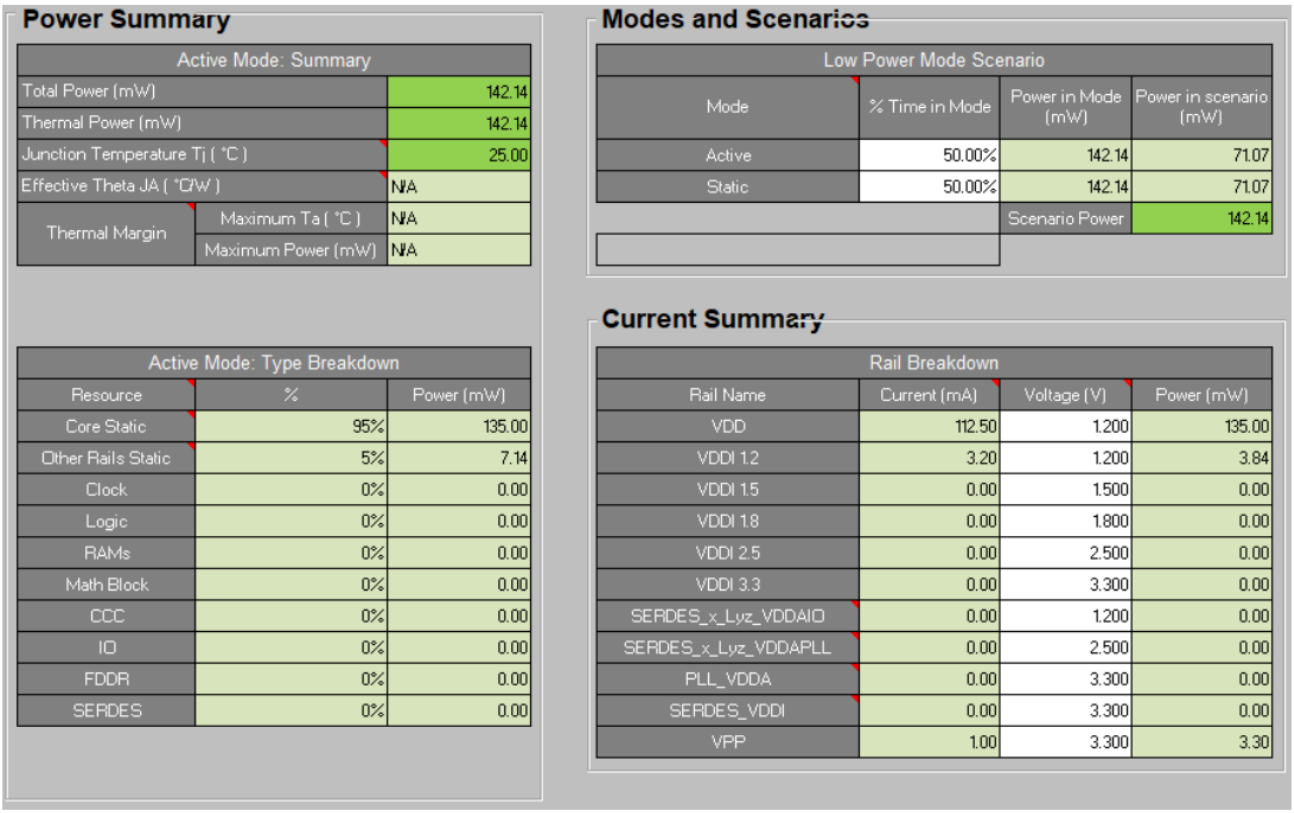
Low Power Mode Scenario			
Mode	% Time in Mode	Power in Mode (mW)	Power in scenario (mW)
Active	50.00%	142.14	71.07
Static	50.00%	142.14	71.07
		Scenario Power	142.14

2.8 Step – 4: Power Estimation Summary

The Power Summary section provides the total power and power breakdown based on the power sources and rails. It also provides the Thermal Margin (Maximum Ta and Maximum Power) summary.

Figure 17 shows Current Summary, Power Summary, and Modes and Scenarios sections in the Summary worksheet.

Figure 17 • Summary Worksheet



Power Summary

Active Mode: Summary		
Total Power (mW)		142.14
Thermal Power (mW)		142.14
Junction Temperature Tj (°C)		25.00
Effective Theta JA (°C/W)		N/A
Thermal Margin	Maximum Ta (°C)	N/A
	Maximum Power (mW)	N/A

Active Mode: Type Breakdown		
Resource	%	Power (mW)
Core Static	95%	135.00
Other Rails Static	5%	7.14
Clock	0%	0.00
Logic	0%	0.00
RAMs	0%	0.00
Math Block	0%	0.00
CCC	0%	0.00
IO	0%	0.00
FDDR	0%	0.00
SERDES	0%	0.00

Modes and Scenarios

Low Power Mode Scenario			
Mode	% Time in Mode	Power in Mode (mW)	Power in scenario (mW)
Active	50.00%	142.14	71.07
Static	50.00%	142.14	71.07
		Scenario Power	142.14

Current Summary

Rail Breakdown			
Rail Name	Current (mA)	Voltage (V)	Power (mW)
VDD	112.50	1.200	135.00
VDDI 1.2	3.20	1.200	3.84
VDDI 1.5	0.00	1.500	0.00
VDDI 1.8	0.00	1.800	0.00
VDDI 2.5	0.00	2.500	0.00
VDDI 3.3	0.00	3.300	0.00
SERDES_x_Lyz_VDDAIO	0.00	1.200	0.00
SERDES_x_Lyz_VDDAPLL	0.00	2.500	0.00
PLL_VDDA	0.00	3.300	0.00
SERDES_VDDI	0.00	3.300	0.00
VPP	1.00	3.300	3.30

Note: Table 13 shows the acceptable rail voltage range.

Table 13 • Acceptable Rail Voltage Range

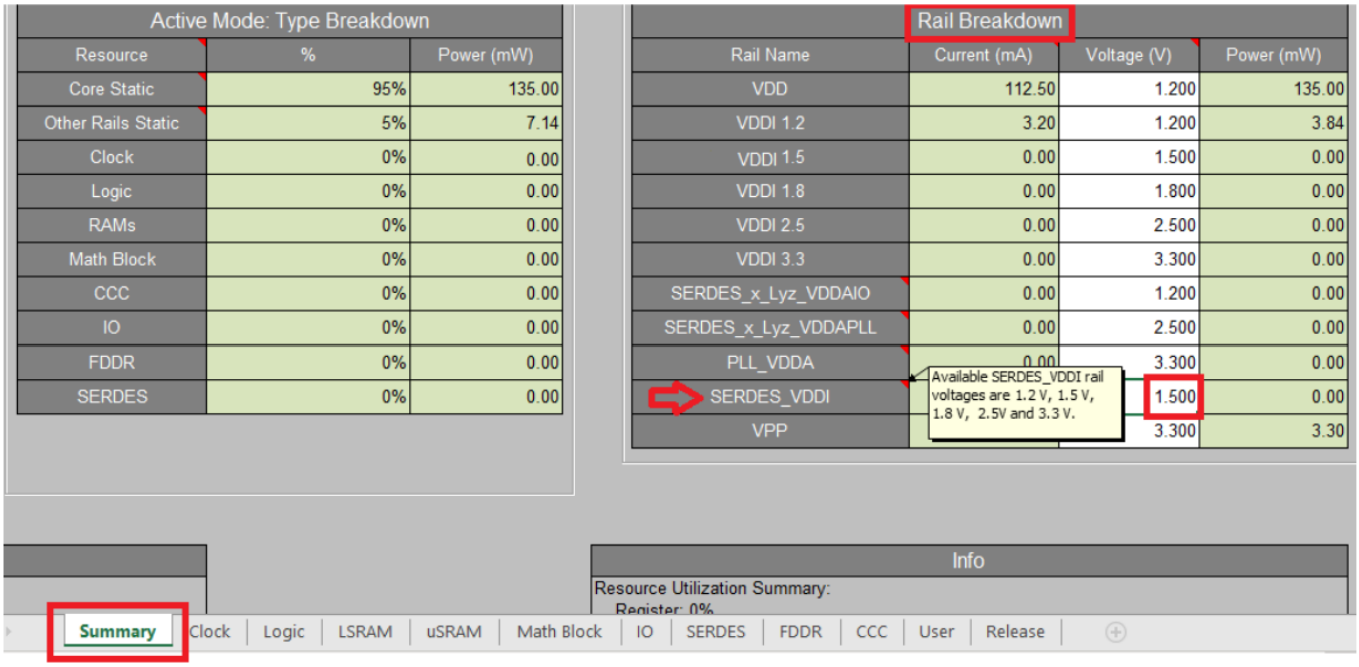
Rail Name	Voltage Range (V)	
	Min	Max
VDD	1.14	1.26
VDDI 1.2	1.14	1.26
VDDI 1.5	1.425	1.575
VDDI 1.8	1.71	1.89
VDDI 2.5	2.375	2.625
VDDI 3.3	3.15	3.45
SERDES J011_L[0123LVDDA10	1.14	1.26
SERDES JOILL[0123]_VDDAPLL	2.375	2.625
PLL_VDDA (3.3 V)1	3.135	3.465
SERDES VDDI	1.14	3.45
VPP	3.135	3.465

1. PLL Analog Supply includes SERDES_x_PLL_VDDA (x: 0 to 6), FDDR_x_PLL_VDDA (x: 0 to 2) and CCC_x_PLL_VDDA (x = NE0, NE1, NW0, NW1, SW0, SW1, SE0, SE1).

The SERDES_REFCLK (Bank Type) and IO standards selection in the IO tab depends on the SERDES_VDDI rail Voltage in the Summary tab.
Note: You can change the SERDES_VDDI rail voltage from the Rail Breakdown table in the Summary tab. The following are the applicable ranges:

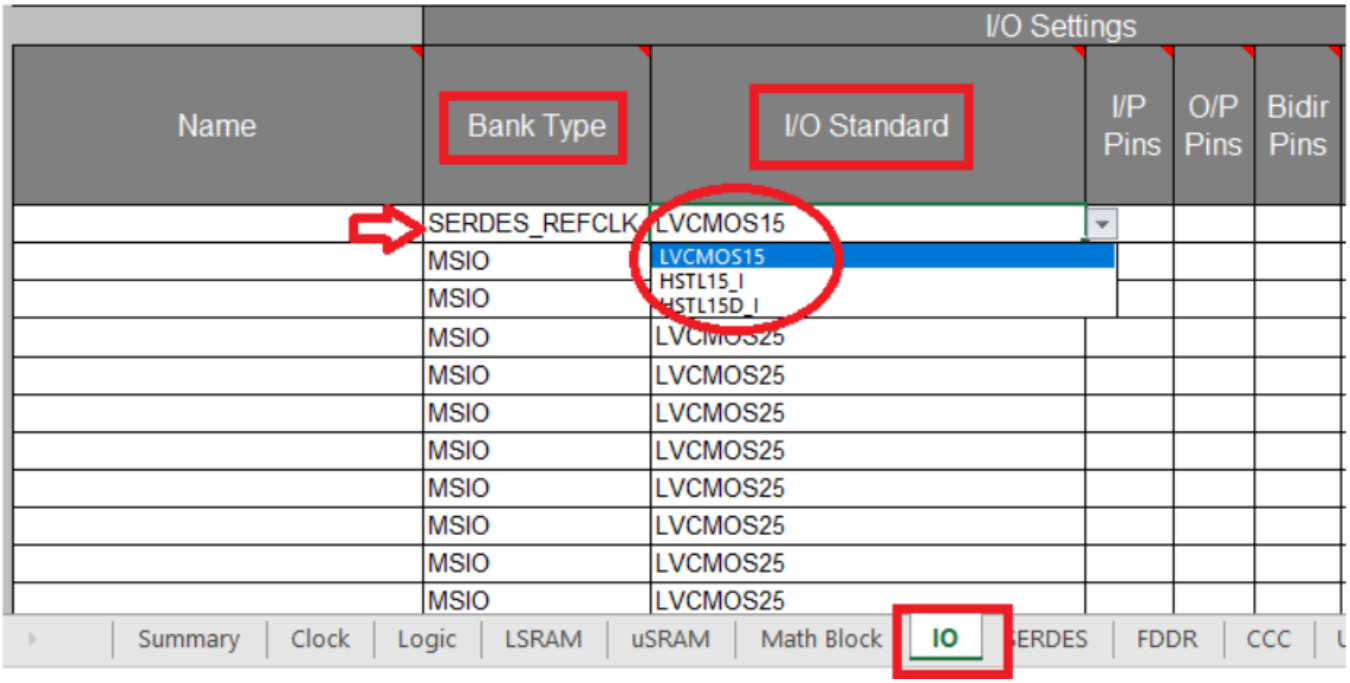
- [1.14, 1.26] for 1.2 V
- [1.425, 1.575] for 1.5 V
- [1.710, 1890] for 1.8 V
- [2.375, 2.625] for 2.5 V
- [3.15, 3.45] for 3.3. V

Figure 18 • Summary Tab



Note: Type in one of the available SERDES_VDDI rail voltage as shown in tool tip in the cell (Voltage column).

Figure 19 • IO Tab



Note: Since SERDES_VDDI rail voltage is selected 1.5v (Figure 18), I/O standards for SERDES_REFCLK can now be selected from the drop down matching the rail voltage.
Figure 20 shows the Device Utilization section displayed at the bottom of the Summary worksheet.

Figure 20 • Device Utilization Section

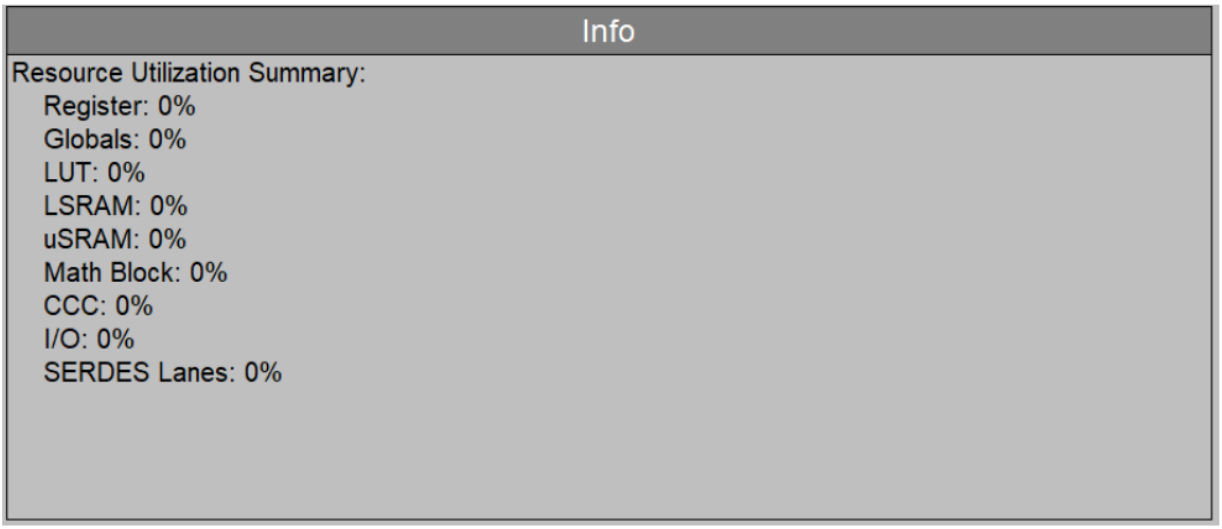


Figure 21 shows the Errors section in the Summary worksheet.

Figure 21 • Errors Section

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

Documents / Resources

	Microsemi UG0596 RTG4 FPGA Power Estimator Software [pdf] User Guide UG0596, UG0596 RTG4 FPGA Power Estimator Software, RTG4 FPGA Power Estimator Soft ware, FPGA Power Estimator Software, Power Estimator Software, Estimator Software

References

- Microsemi | Semiconductor & System Solutions | Power Matters
- microsemi.com/index.php?option=com_docman&task=doc_download&gid=130850
- microsemi.com/index.php?option=com_docman&task=doc_download&gid=134406
- microsemi.com/index.php?option=com_docman&task=doc_download&gid=134407
- Downloads | Silicon User's Guides | SoC | Internal Documents | Microsemi
- UG0XXX: RTG4 SERDES Block Handbook
- microsemi.com/index.php?option=com_docman&task=doc_download&gid=134410
- microsemi.com/index.php?option=com_docman&task=doc_download&gid=134430
- microsemi.com/document-portal/doc_download/1244030-rtg4-power-calculator