Microsemi SmartFusion2 MSS GPIO Configuration User Manual

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Contents

Introduction

The SmartFusion2 Microcontroller Subsystem (MSS) provides one GPIO hard peripheral (APB_1 sub bus) supporting 32 General Purpose I/Os.
On the MSS canvas, you must enable (default) or disable the GPIO instance based on whether it is being used in your current application. If disabled, the GPIO instance is held in reset (lowest power state). By default, no GPIO is used when you enabled the GPIO instance the first time. Note that MSIOs allocated to the GPIO instance are shared with other MSS peripherals. These shared I/Os are available to connect other peripherals when the GPIO instance is disabled or if the GPIO instance ports are connected to the FPGA fabric. Note that GPIOs are

configured individually in the GPIO peripheral configurator. The functional behavior of each GPIO (i.e. interrupt behavior) must be defined at the application level using the SmartFusion2 MSS MMUART Driver provided by Microsemi. In this document, we describe how you to configure the MSS GPIO instances and define how the peripheral signals are connected. For more details about the MSS GPIO hard peripherals, please refer to the SmartFusion2 User Guide

Configuration Options

Set/Reset Definition – There are four equal groups of eight GPIOs each for a total of 32. You can define a common source and state (Set or Reset) for the eight GPIOs in a group. There are two choices for the source of Set/Reset:

- System Registers – Each group has a unique system register for this purpose. The system registers can be accessed via firmware. Setting the MSS_GPIO_<range>_SOFT_RESET system register will reset all GPIOs in that range to the value defined by the reset state.
- FPGA Fabric – The signal is called MSS_GPIO_RESET_N.

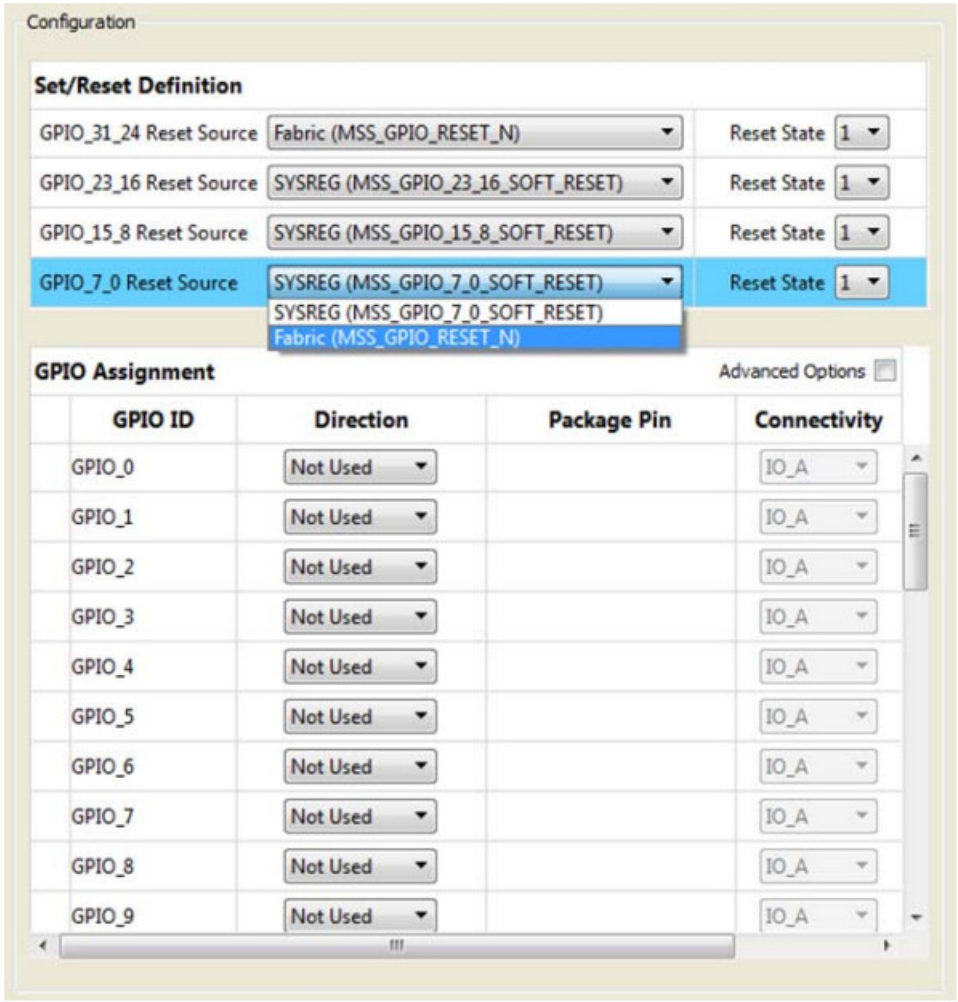

Figure 1-1 SmartFusion2 MSS GPIO Configuration Options

GPIO Signals Assignment Table

The SmartFusion2 architecture provides a very flexible schema for connecting peripherals' signals to either MSIOs or the FPGA fabric. Use the signal assignment configuration table to define what your peripheral is connected to in your application. This assignment table has the following columns:

GPIO ID – Identifies the GPIO identifier – 0 to 31 – for each row.
Direction – Indicates if the GPIO is configured as Input, Output, Tristate or Bidirectional. Use the pulldown to set the GPIO direction.
Package Pin – Shows the package pin associated with the MSIO when the signal is connected to an MSIO.

Connectivity – Use the drop-down list to select whether the signal is connected to an MSIO or the FPGA fabric. There are two options – A and B -, in each case, that you can choose from.
MSIO – There are two different I/O assignments possible for each
GPIO: IO_A and IO_B. You can select either and check the package pin. A tooltip over the package pin indicates which other peripherals could also use the same MSIO. You can use the IO_A and IO_B options to resolve conflicts. For instance, in IO_A is already used by another peripheral, you can chose IO_B. In some device/package combinations, both IO_A and/or IO_B options may not be available.
FPGA Fabric – There are two different assignments possible for each GPIO to the FPGA fabric: – Fabric_A and Fabric_B. You can use the Fabric_A and Fabric_B options to resolve conflicts. For instance, in Fabric_A is already used by another peripheral, you can choose Fabric_B. In some devices, both Fabric_A and/or Fabric_B options may not be available. Extra Connections – Use the Advanced Options check-box to view the extra connection options:

- Check the Fabric option to observe into the FPGA fabric a signal that is connected to an MSIO.

Connectivity Preview

The Connectivity Preview panel in the MSS GPIO Configurator dialog shows a graphical view of the current connections for the highlighted signal row (Figure 3-1).

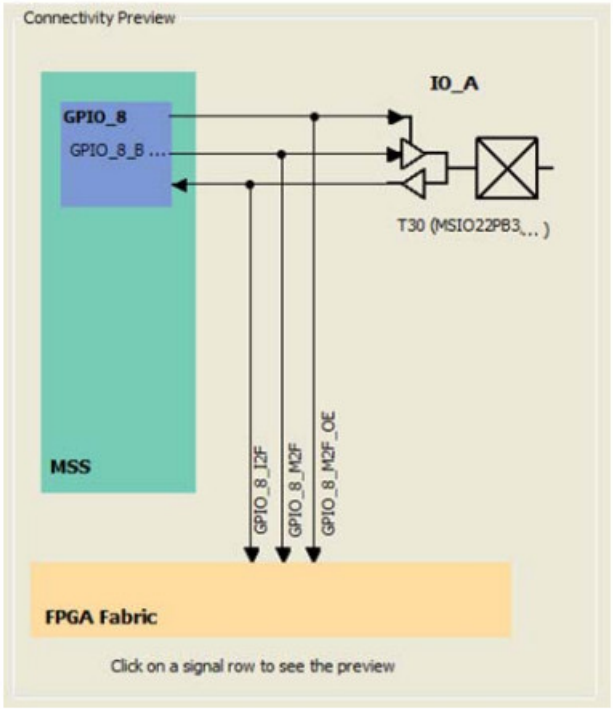

Figure 3-1 Connectivity Preview Panel

Resource Conflicts

Because MSS peripherals – MMUART, I2C, SPI, CAN, GPIO, USB and the Ethernet MAC – share MSIO and FPGA fabric access resources, the configuration of any of these peripherals may result in a resource conflict when you configure an instance of the current peripheral. Peripheral configurators provide clear indicators when such a conflict arises.

Resources used by a previously configured peripheral result in three types of feedback in the current peripheral configurator:

Information – If a resource used by another peripheral does not conflict with the current configuration, an information icon is displayed, in the Connectivity Preview panel, on that resource. A tooltip on the icon provides details about which peripheral uses that resource.

Warning/Error – If a resource used by another peripheral does conflict with the current configuration, a warning or error icon appears, in the Connectivity Preview panel, on that resource. A tooltip on the icon provides details about which peripheral uses that resource. When errors are displayed you cannot commit the current configuration. Y

ou can either resolve the conflict by using a different configuration or cancel the current configuration using the Cancel button. When warnings are displayed (and there are no errors), you can commit the current configuration. However, you cannot generate the overall MSS; you will see generation errors in the Libero SoC log window. You must resolve the conflict that you created when you committed the configuration by reconfiguring either of the peripherals causing the conflict. The peripheral configurators implement the following rules to determine if a conflict should be reported as an error or a warning.

1. If the peripheral being configured is the GPIO peripheral then all conflicts are errors.
2. If the peripheral being configured is not the GPIO peripheral then all conflicts are errors unless the conflict is with a GPIO resource in which case conflicts will be treated as warnings.

Error Feedback Example

The I2C_1 peripheral is used and uses the device PAD bounded to package pin V23. Configuring the GPIO peripheral (GPIO_0) such that the GPIO_0 port is connected to an MSIO results in an error. Figure 4-1 shows the error icon displayed in the connectivity assignment table for the GPIO_0 port.

Figure 4-1 Error Displayed in the Connectivity Assignment Table

Figure 4-2 shows the error icon displayed in the preview panel on the PAD resource for the GPIO_0 port.

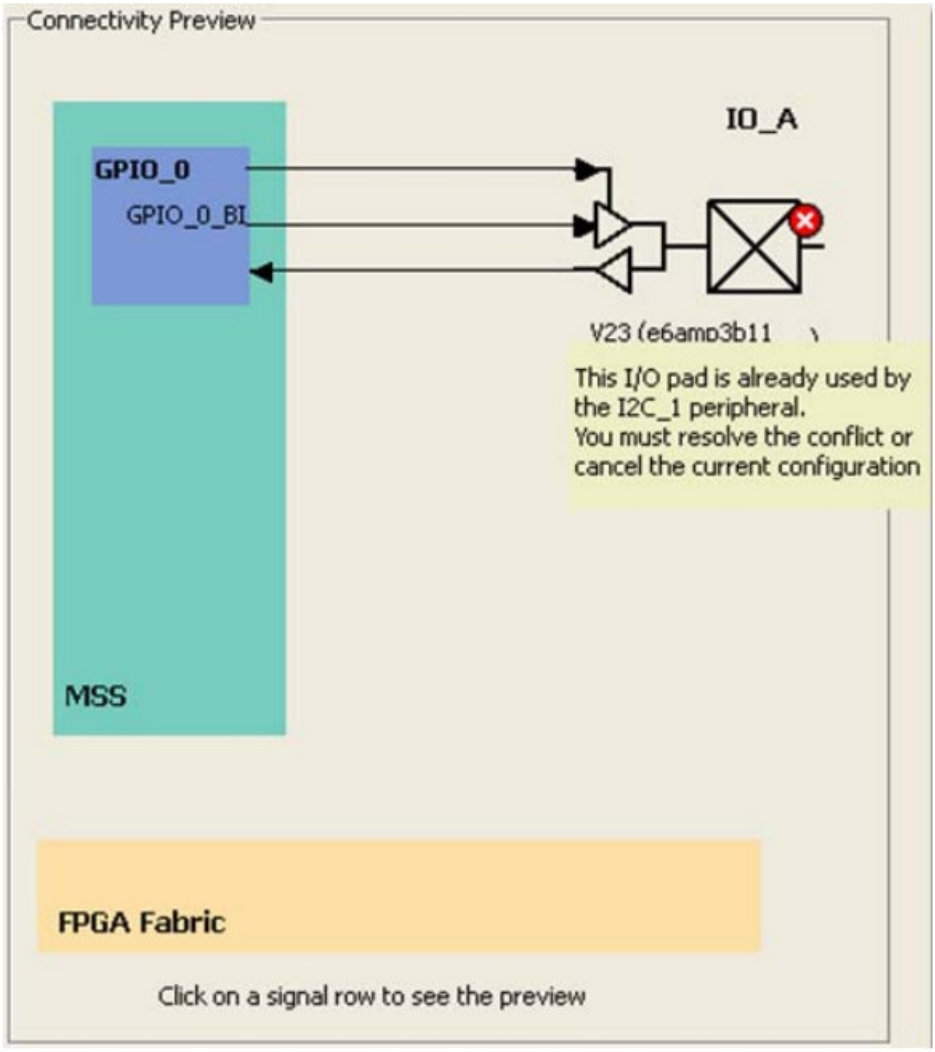

Figure 4-2 Error Displayed in the Preview Panel

Information Feedback Example

The I2C_1 peripheral is used and uses the device PAD bounded to package pin V23. Configuring the GPIO peripheral such that the GPIO_0 port is connected to the FPGA fabric does not result in a conflict. However, to indicate that he PAD associated with the GPIO_0 port (but not used in this case), the Information icon is displayed in the preview panel (Figure 4-3). A tooltip associated with the icon provides a description of how the resource is used (I2C_1 in this case).

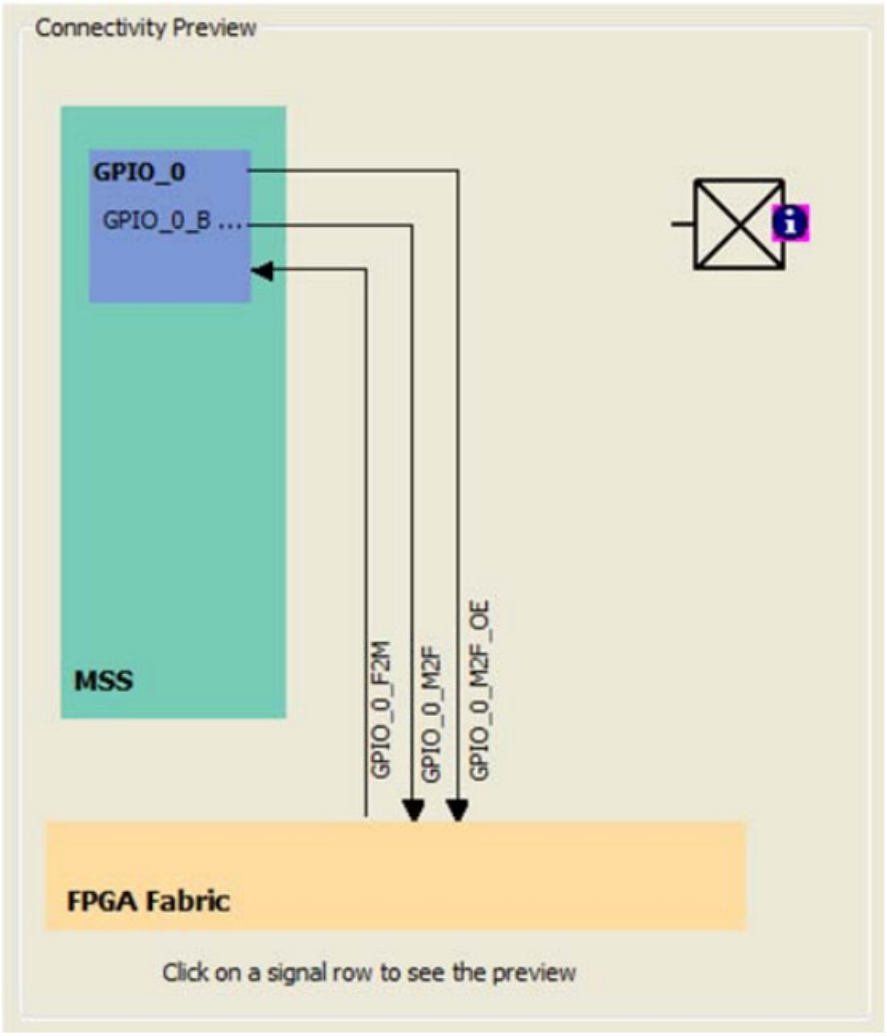

Figure 4-3 Information Icon in the Preview Panel

Port Description

Table 5-1 GPIO Port Description

Port Name	Port Group	Description
GPIO_<n>	GPIO_PADS/GPIO_FABRIC	GPIO signal

Note:

- I/O ‘main connection’ ports names have IN, OUT, TRI or BI as a suffix based on the selected direction, e.g. GPIO_0_IN.
- Fabric ‘main connection’ input ports names have “F2M” as a suffix, e.g. GPIO _8_F2M. • Fabric ‘extra connection’ input ports names have “I2F” as a suffix, e.g. GPIO_8_I2F.
- Fabric output and output-enable ports names have “M2F” and “M2F_OE” as a suffix, e.g. GPIO_8_M2F and GPIO_ 8_M2F_OE. • PAD ports are automatically promoted to top throughout the design hierarchy.

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contains information about contacting Microsemi SoC Products Group and using these support services.

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From the rest of the world, call 650.318.4460

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Website

You can browse a variety of technical and non-technical information on the SoC home page, at **www.microsemi.com/soc**.

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Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

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Documents / Resources

	Microsemi SmartFusion2 MSS GPIO Configuration [pdf] User Manual SmartFusion2 MSS GPIO Configuration, SmartFusion2 MSS, GPIO Configuration, Configuration

References

- Microsemi | Semiconductor & System Solutions | Power Matters
- Libero® SoC Design Suite Versions 2023.1 to 12.0 | Microchip Technology
- Libero® SoC Design Suite Versions 2023.1 to 12.0 | Microchip Technology
- Libero® SoC Design Suite Versions 2022.3 to 12.0 | Microchip Technology
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