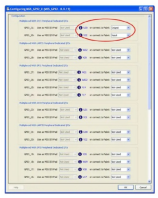
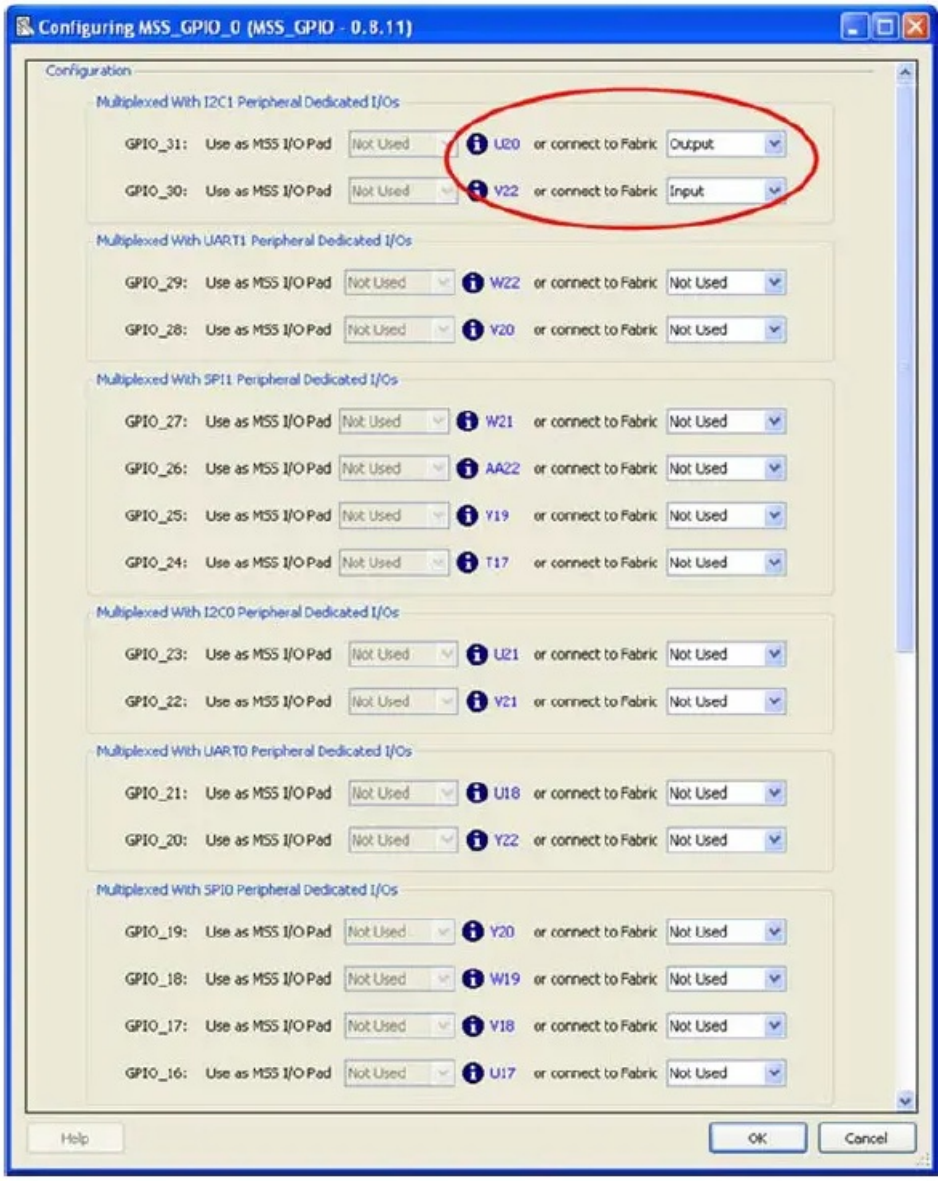


Microsemi SmartDesign MSS GPIO Configuration User Manual

Contents

Microsemi SmartDesign MSS GPIO Configuration



The SmartFusion Microcontroller Subsystem (MSS) provides a GPIO hard peripheral (APB_1 sub bus) with 32 configurable GPIOs. The actual behavior of each GPIO (input, output and output enable register controls, interrupt modes, etc.) can be defined at the application level using the SmartFusion MSS GPIO Driver provided by Actel. However, you must define whether a GPIO is directly connected to an external pad (MSS I/O) or to the FPGA fabric. This portion of the device configuration is done using the MSS GPIO configurator and is described in this document.
For more details about the MSS GPIO hard peripheral, please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.

Connectivity Options

MSS I/O Pad – Select this option to indicate that the selected GPIO will be connected to an external dedicated pad (MSS I/O). You must select the type of I/O buffer – INBUF, OUTBUF, TRIBUFF and BIBUF – that will define how the MSS I/O pad is being configured. Note that this option may not be available if the MSS I/O is already used by another peripheral or the fabric (see the MSS I/O Sharing section for more details)

Fabric – Select this option to indicate that the selected GPIO will be connected to the FPGA fabric. You must select whether you want the GPI (Input), GPO (Output) or both GPI and GPO (Input/Output) connection(s) to be brought out to connect to the fabric. Note that the GPIO output enable register cannot be brought out to the fabric when this option is selected. Also, GPI's connected to the fabric can trigger interrupts from user logic if the appropriate interrupt enable bits are set properly by your application (MSS GPIO driver initialization functions).

MSS I/O Sharing

In the SmartFusion architecture MSS I/Os are shared between two MSS peripherals or between a MSS peripheral and the FPGA fabric. MSS GPIOs may not be able to connect to a particular MSS I/O if this I/Os is already connected to a MSS peripheral or to the FPGA fabric. The GPIO configurator provides direct feedback regarding whether a GPIO can be connected to a MSS I/O or not.

GPIO[31:16]

GPIO[31:16] are organized in groups that indicate which MSS peripheral they are sharing MSS I/Os with. If a peripheral is used (enabled on the MSS canvas), then the MSS I/O Pad pull-down menu is grayed-out for the corresponding shared GPIOs and an Info icon is displayed next to the pull-down menu. The Info icon indicates that the MSS I/O option cannot be selected because it is already used by a MSS peripheral or, based on the package selected, not bonded.

Example 1

SPI_0, SPI_1, I2C_0, I2C_1, UART_0 and UART_1 are enabled in the MSS canvas.

- GPIO[31:16] cannot be connected to an MSS I/O. Note the grayed-out menus and the Info icons (Figure 1-1).
- GPIO[31:15] can still be connected to the FPGA fabric. In this example, GPIO[31] is connected to the fabric as an Output and GPIO[30] as an Input.

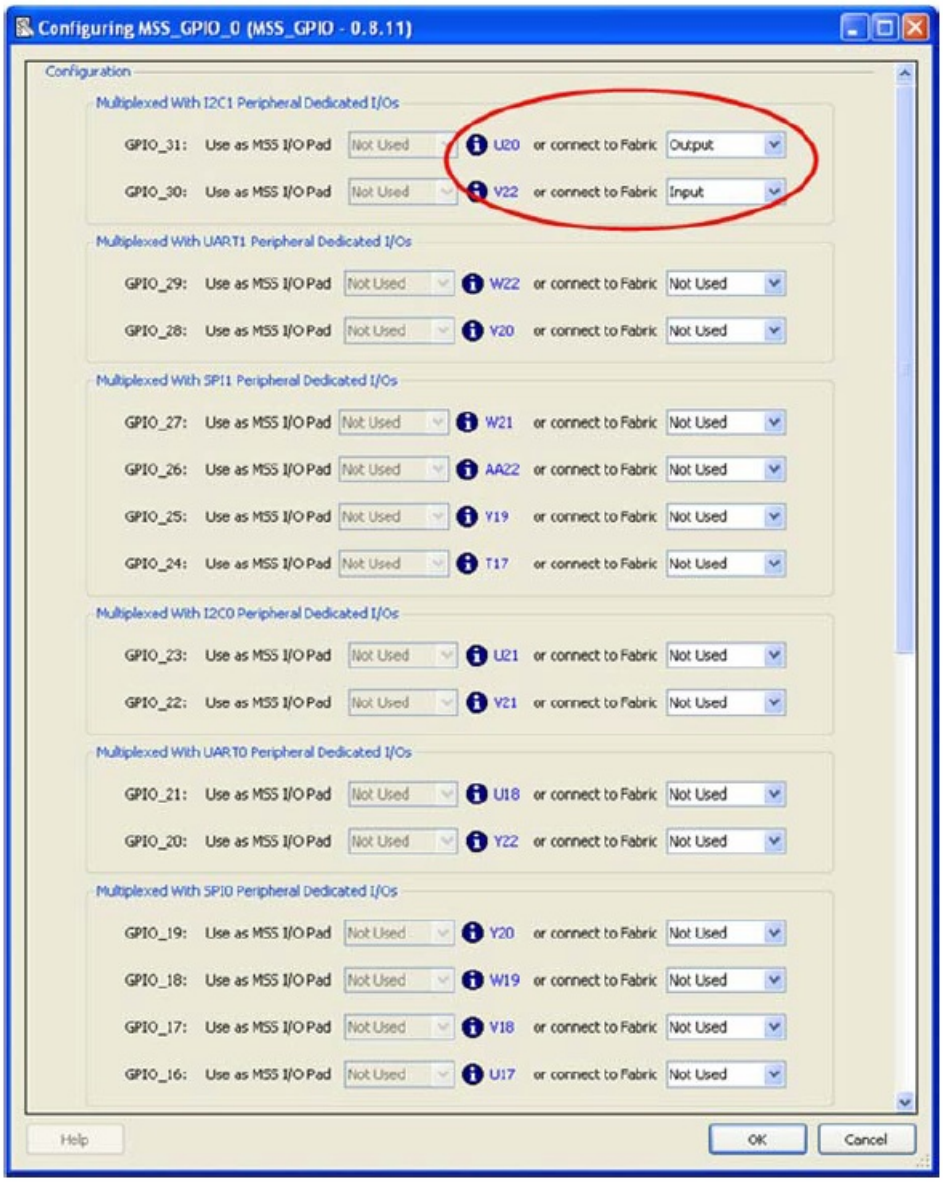


***Figure 1-1* • GPIO Configuration Example 1**

Example 2
I2C_0 and I2C_1 are disabled in the MSS canvas.

- GPIO[31:30] and GPIO[23:22] can be connected to an MSS I/O (as shown in Figure 1-2).
- In this example, both GPIO[31] and GPIO[30] are connected to a MSS I/O as Output ports.
- In this example, GPIO[23] is connected to a MSS I/O as an Input port and GPIO[22] is connected to an MSS I/O as a Bidirectional port.
- GPIO[29:24,21:16] cannot be connected to an MSS I/O. Note the grayed-out menus and the Info icons.
- GPIO[29:24,21:16] can still be connected to the FPGA fabric. In this example, both GPIO[29] and GPIO[28] are connected to the fabric as Input ports.

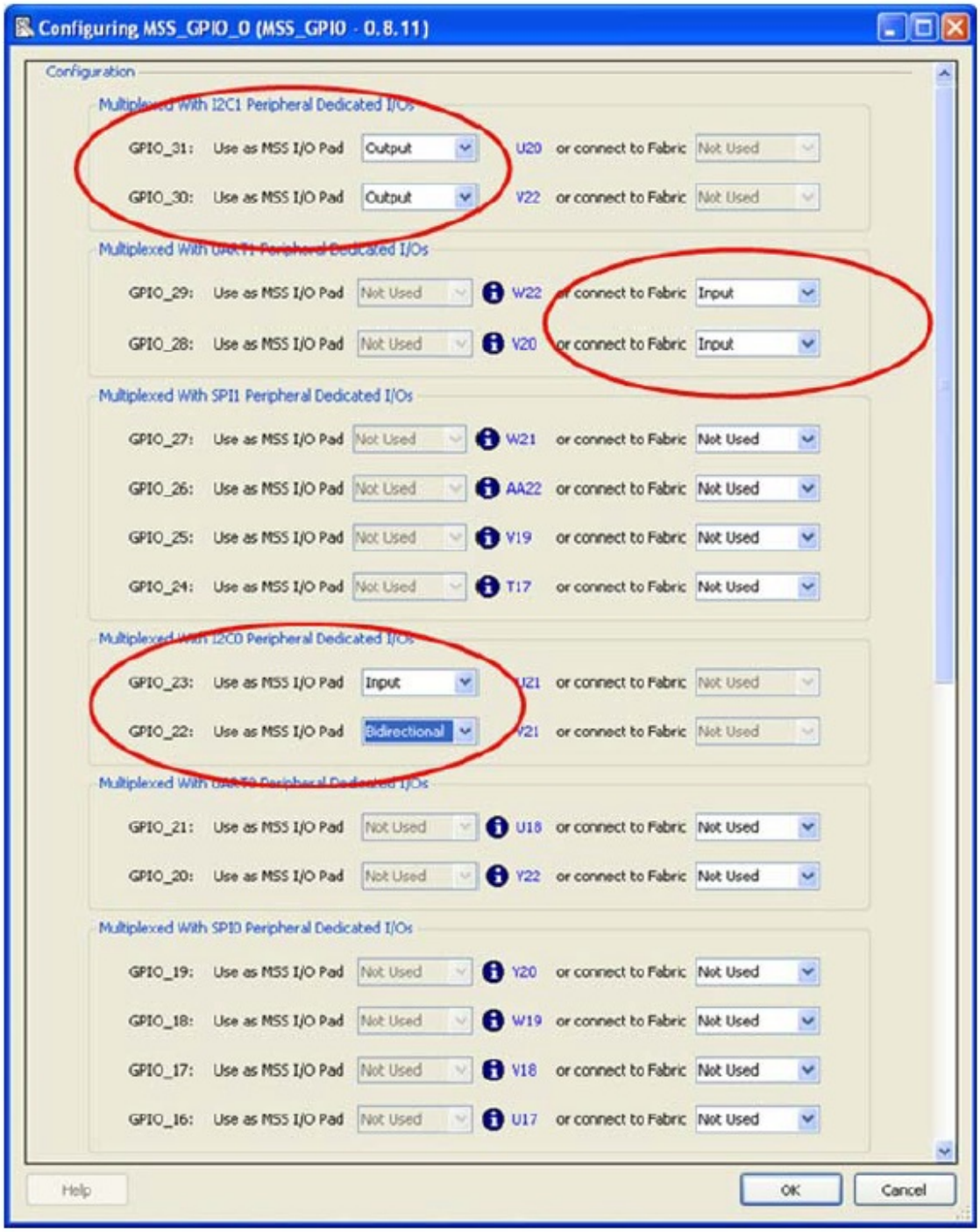


***Figure 1-2* • GPIO Configuration Example 2**

GPIO[15:0]

GPIO[15:0] share MSS I/Os that can be configured to connect to the FPGA fabric (this later configuration can be done using MSS I/O Configurator). If an MSS I/O is configured to connect to the FPGA fabric, then the MSS I/O Pad pull-down menu is grayed-out for the corresponding shared GPIOs and an Info icon is displayed next to the pull-down menu. The Info icon indicates that the MSS I/O option cannot be selected because it is already used or, based on the package selected, not bonded.

Note that the blue text in the configurator highlights the package pin name for each MSS I/O associated with a GPIO. This information is useful for planning board layout.

Example

To properly demonstrate how the MSS I/O configurations and the GPIO[15:0] configurations are coupled, Figure 1-3 shows both configurators side by side with the following configuration:

- MSS I/O[15] is used as an INBUF port connected to the FPGA fabric. Consequently, GPIO[15] cannot be

connected to an MSS I/O.

- GPIO[5] is connected to an MSS I/O as an Input. Consequently MSS I/O[5] cannot be used to connect to the FPGA fabric.
- GPIO[3] is connected to the FPGA fabric as an Output. Consequently MSS I/O[3] cannot be used to connect to the FPGA fabric.

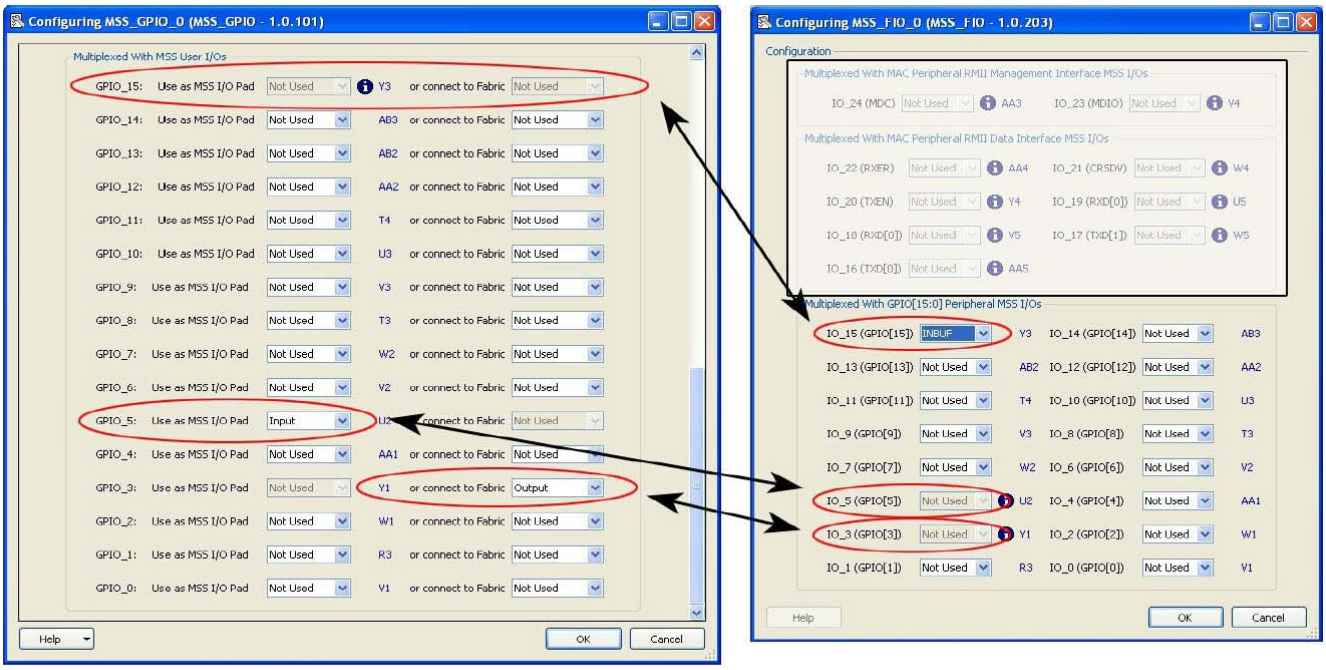


Figure 1-3 • **MSSIO and GPIO Configuration Example**

Port Description

Table 2-1 • GPIO Port Description

Port Name	Direction	PAD ?	Description
GPIO_<index>_IN	In	Yes	GPIO port name when GPIO[index] is configured as an MSS I/O **Input** port
GPIO_<index>_OUT	Out	Yes	GPIO port name when GPIO[index] is configured as an MSS I/O **Output** port
GPIO_<index>_TRI	Out	Yes	GPIO port name when GPIO[index] is configured as an MSS I/O **Tristate** port
GPIO_<index>_BI	Inout	Yes	GPIO port name when GPIO[index] is configured as an MSS **I/O Bidirectional** port
F2M_GPI_<index>	In	No	GPIO port name when GPIO[index] is configured to connect to the FPGA fabric as an **Input** port (F2M indicates that the signal is going from the fabric to the MSS)
M2F_GPO_<index>	In	No	GPIO port name when GPIO[index] is configured to connect to the FPGA fabric as an **Output** port (M2F indicates that the signal is going from the MSS to the fabric)

Note:

- PAD ports are automatically promoted to top throughout the design hierarchy.
- Non-PAD ports must be promoted manually to the top level from the MSS configurator canvas to be available as the next level of hierarchy.

Product Support

The Microsemi SoC Products Group backs its products with various support services including a Customer Technical Support Center and Non-Technical Customer Service. This appendix contains information about contacting the SoC Products Group and using these support services.

Contacting the Customer Technical Support Center
Microsemi staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

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Microsemi customers can receive technical support on Microsemi SoC products by calling Technical Support Hotline anytime Monday through Friday. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week.
Web: **www.actel.com/mycases**
Phone (North America): 1.800.262.1060
Phone (International): +1 650.318.4460
Email: **soc_tech@microsemi.com**

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Phone (North America): 1.888.988.ITAR
Phone (International): +1 650.318.4900
Email: **soc_tech_itar@microsemi.com**

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Corporate Headquarters Microsemi Corporation 2381 Morse Avenue Irvine, CA
92614-6233
USA
Phone 949-221-7100 Fax 949-756-0308

SoC Products Group 2061 Stierlin Court Mountain View, CA 94043-4655
USA
Phone 650.318.4200 Fax 650.318.4600 **www.actel.com**

SoC Products Group (Europe) River Court, Meadows Business Park Station Approach, Blackwatery Camberley Surrey GU17 9AB United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

SoC Products Group (Japan) EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku Tokyo 150 Japan
Phone +81.03.3445.7671 Fax +81.03.3445.7668

SoC Products Group (Hong Kong) Room 2107, China Resources Building 26 Harbour Road
Wanchai, Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488

Documents / Resources

	**Microsemi SmartDesign MSS GPIO Configuration** [pdf] User Manual SmartDesign MSS GPIO, Configuration, SmartDesign MSS GPIO Configuration, SmartDesign MSS

References

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- FPGAs and PLDs | Microchip Technology
- FPGAs and PLDs | Microchip Technology
- Microsemi | Semiconductor & System Solutions | Power Matters