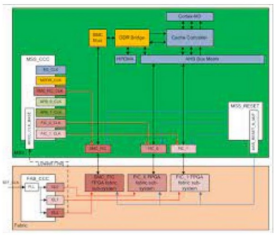
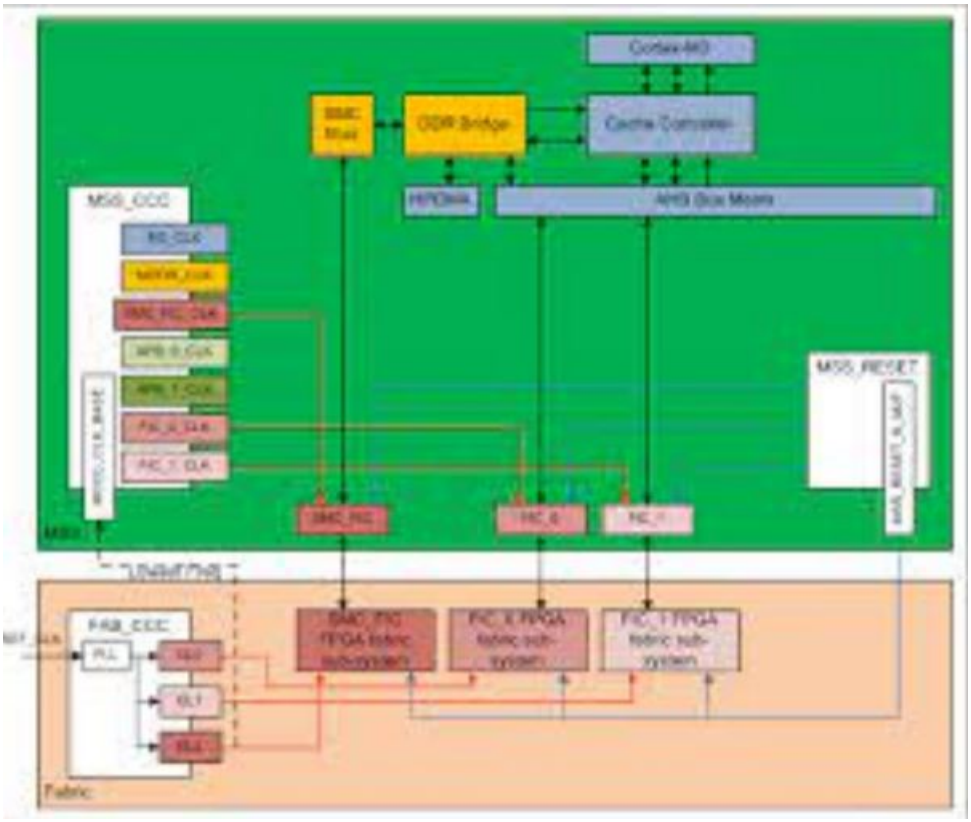


Microsemi SmartDesign MSS Fabric Interface Instruction Manual

Contents

Microsemi SmartDesign MSS Fabric Interface



SmartDesign MSS Fabric Interface Controller

The SmartDesign MSS Fabric Interface Controller (FIC) is a part of the microcontroller subsystem (MSS) that performs a bridging function between the AHB bus matrix and an AHB or APB bus in the FPGA fabric. The FIC provides two bus interfaces between the MSS and the fabric, with one being mastered by the MSS and having slaves in the fabric, and the other having a master in the fabric and slaves in the MSS. The address and data buses between the FIC and the FPGA fabric are common to both the AHB and APB interfaces.

The Fabric Interface Controller (FIC) provides several configuration options related to clock frequencies and pipelining of transactions. In pipelined mode, the ratio between the MSS FCLK frequency and the frequency of the AHB/APB circuitry in the FPGA fabric can be 1:1, 2:1, or 4:1. If the interfaces are configured as AHB and the clock ratio is 1:1, it is possible to select a bypass mode in which signals to and from the fabric are not registered. However, fewer clock cycles are required to complete each transaction in bypass mode, but the overall system frequency may be lower than in pipelined mode.

Configuration Options

The following configuration options are available:

- Clock Configuration
- Interface Configuration

The fabric interface controller (FIC) is part of the microcontroller subsystem (MSS) and performs an AHB to AHB or AHB to APB bridging function between the AHB bus matrix and an AHB or APB bus in the FPGA fabric. The FIC consumes no FPGA resources. It provides two bus interfaces between the MSS and the fabric. The first is mastered by the MSS and has slaves in the fabric and the second has a master in the fabric and slaves in the MSS.
The address and data buses between the FIC and the FPGA fabric are common to both the AHB and APB interfaces; hence only one type of interface can be enabled at any time. However, separate groups of signals are used for the AHB and APB control signals.
In addition to the choice of AHB or APB interfaces between the MSS and the fabric, a number of options related to

relative clock frequencies and pipelining of transactions are available. In pipelined mode, the ratio between the MSS FCLK frequency and the frequency of the AHB/APB circuitry in the FPGA fabric can be 1:1, 2:1, or 4:1. If the interfaces are configured as AHB and the clock ratio is 1:1, it is possible to select a bypass mode in which signals to and from the fabric are not registered. In bypass mode, fewer clock cycles are required to complete each transaction but the overall system frequency may be lower than is possible in pipelined mode.
The Fabric Interface configurator enables you to define how the MSS to fabric sub-system should be configured. Use the MSS Clock Configurator to configure the fabric clock.
For more details about the Fabric Interface Controller (FIC), please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.

Port Description

The Fabric Interface Controller (FIC) provides two bus interfaces between the MSS and the fabric:

- Mastered by MSS with slaves in the fabric
- Mastered by fabric with slaves in MSS

Product Support

If you require further support, please use the following:

- Customer Service
- Customer Technical Support Center
- Technical Support
- Website
- Contacting the Customer Technical Support Center
- ITAR Technical Support

Product Usage Instructions

To configure the Fabric Interface Controller (FIC):

1. Use the MSS Clock Configurator to configure the fabric clock.
2. Use the Fabric Interface configurator to define how the MSS to fabric sub-system should be configured.
3. Choose between AHB or APB interfaces between the MSS and the fabric.
4. Select a clock ratio of 1:1, 2:1, or 4:1 in pipelined mode.
5. Select bypass mode in AHB interface and 1:1 clock ratio configuration to reduce the number of clock cycles required to complete each transaction.

Please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide for more details about the Fabric Interface Controller (FIC).

Clock Configuration

- **MSS Clock Frequency –** Displays the MSS clock (FCLK) frequency as defined in the MSS Clock Management configurator (as shown in Figure 1-1). It is updated automatically when FCLK is updated in the clock management configurator.

- **Fabric Clock Frequency –** Displays the fabric clock (FAB_CLK) frequency as defined in the MSS Clock Management configurator. It is updated automatically when FAB_CLK is updated in the clock management configurator. You should verify that the design meets all the timing constraints using SmartTime. You may have to change FCLK or FAB_CLK or both for the design to meet all timing constraints.

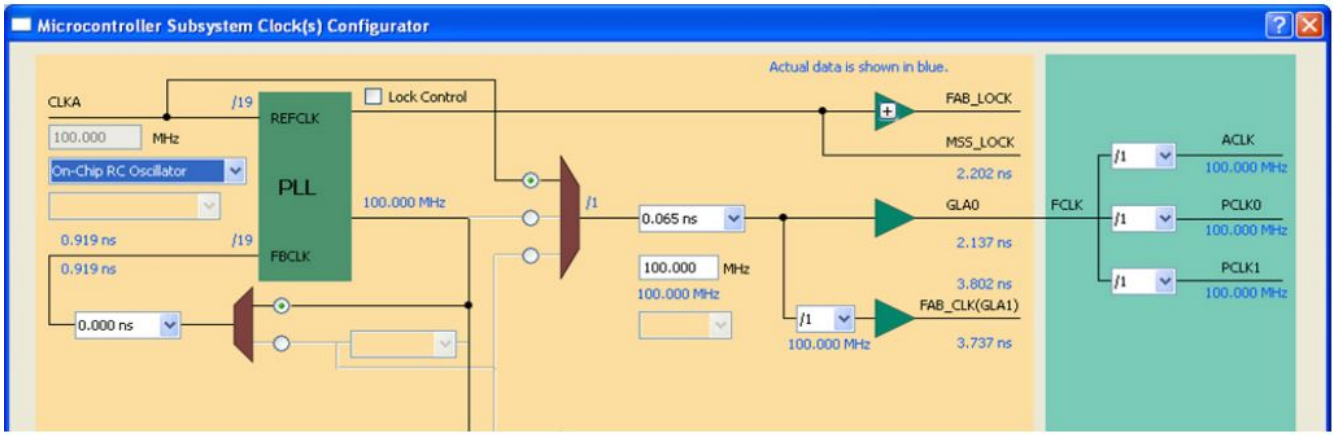


Figure 1-1 • MSS Clock(s) Configurator

Interface Configuration

- **Interface Type –** Use this option to select between the AMBA APB3 (AHB to APB bridge) and AHBLite (AHB to AHB bridge) FIC modes (Figure 1-2).
- **Bypass Mode –** Use this option to enable the FIC bypass mode, in which signals to and from the fabric are not registered. In bypass mode, fewer clock cycles are required to complete each transaction but the overall system frequency may be lower than is possible in pipelined mode.
- **Master Interface –** Use this option to expose the master Bus Interface (BIF) port. You must use this option when a master in the MSS addresses a peripheral in the FPGA fabric. Select this mode if you want the MSS to be a MASTER or if you want the FABRIC to be the MASTER.
- **Slave Interface –** Use this option to expose the slave Bus Interface (BIF) port. You must use this option when a master in the FPGA fabric addresses a peripheral in the MSS. Select this mode if you want the MSS to be a SLAVE or if you want the FABRIC to be the SLAVE.

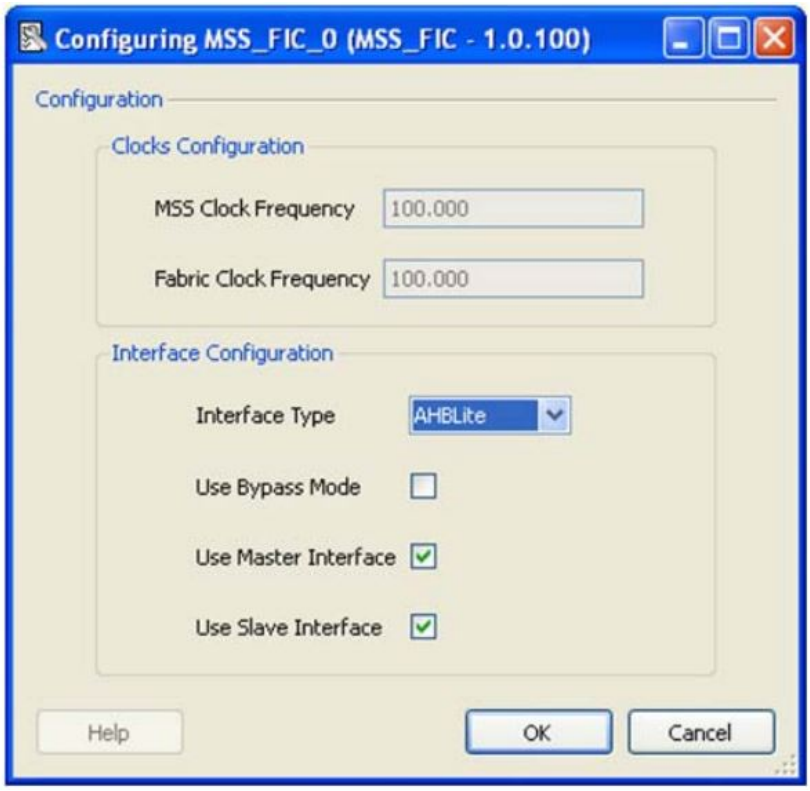


Figure 1-2 • Fabric Interface Configurator

Port Description

Table 2-1 • MSS Hard Master AHBLite Bus Interface (BIF)

Port Name	Direction	Description
MSSHADDR[19:0]	Out	Address bus – byte address on the bus interface
MSSHWDATA[31:0]	Out	Write data from the hard master to the fabric slave.
MSSHRDATA[31:0]	In	Read data from the fabric slave to the hard master.
MSSHLOCK	Out	Lock. When asserted, the current transfer is part of a locked transaction.
MSSHSIZE[1:0]	Out	Indicates the size of the current transfer (8/16/32 byte transactions) 00: byte (8-bit) 01: halfword (16-bit) 10: word (32-bit)
MSSHTRANS[1:0]	Out	Indicates the transfer type of the current transaction. 00 – Idle 01 – Busy 10 – Non-Sequential 11 – Sequential
MSSHWRITE	Out	When high, indicates that the current transaction is a write. When low, indicates that the current transaction is a read.
MSSHREADY	In	When high, indicates that the bus is ready to accept a new transaction.
MSSHRESP	In	Response status – When driven high at the end of a transaction indicates that the transaction has completed with errors. When driven low at the end of a transaction indicates that the transaction has completed successfully.

Table 2-2 • MSS Hard Master APB Bus Interface (BIF)

Port Name	Direction	Description
MSSPADDR[19:0]	Out	Address bus – byte address on the bus interface
MSSPWDATA[31:0]	Out	Write data from the hard master to the fabric slave.
MSSPRDATA[31:0]	In	Read data from the fabric slave to the hard master.
MSSPSEL	Out	Select. The AHB bus matrix to APB bridge unit generates a single select to the fabric.
MSSPENABLE	Out	Enable. This signal indicates the second and subsequent cycles of an APB transfer.

Table 2-2 • MSS Hard Master APB Bus Interface (BIF)

Port Name	Direction	Description
MSSPWRITE	Out	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
MSSPREADY	In	Ready. The slave uses this signal to extend an APB transfer.
MSSPSLVERR	In	This signal indicates a transfer failure.

Table 2-3 • MSS Hard Slave AHBLite Bus Interface (BIF)

Port Name	Direction	Description
FABHADDR[31:0]	In	Address bus from fabric master.
FABWDATA[31:0]	In	Write data from a fabric master to a MSS slave.
FABRDATA[31:0]	Out	Read read data from the selected MSS slave to the fabric master.
FABHMASTLOCK	In	Lock. When asserted the current transfer is part of a locked transaction.
FABHSIZE[1:0]	In	Indicates the size of the current transfer (8/16/32 byte transactions) 00: byte (8-bit) 01: halfword (16-bit) 10: word (32-bit)
FABHTRANS[1:0]	In	Indicates the transfer type of the current transaction. 00 – Idle 01 – Busy 10 – Non-Sequential 11 – Sequential
FABHSEL	In	Slave select. When asserted the MSS is being accessed by the fabric master.
FABHWRITE	In	When high indicates that the current transaction is a write. When low indicates that the current transaction is a read.
FABHREADY	In	When high, indicates that the bus is ready to accept a new transaction.
FABHREADYOUT	Out	Slave ready. When high for a write indicates the selected MSS subsystem slav e is ready to accept data and when high for a read indicates that data is valid.
FABHRESP	Out	Response status. When driven high at the end of a transaction indicates that t he transaction has completed with errors. When driven low at the end of a tran saction indicates that the transaction has completed successfully.

Table 2-4 • MSS Hard Slave APB Bus Interface (BIF)

Port Name	Direction	Description
FABADDR[31:0]	In	Address bus from fabric master.
FABWDATA[31:0]	In	Write data from a fabric master to a MSS slave.

Table 2-4 • MSS Hard Slave APB Bus Interface (BIF)

Port Name	Direction	Description
FABRDATA[31:0]	Out	Read data from the selected MSS slave to the fabric master.
FABPSEL	In	Select. The AHB bus matrix to APB bridge unit generates a single select to the fabric.
FABPENABLE	In	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
FABPWRITE	In	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
FABPREADY	Out	Ready. The slave uses this signal to extend an APB transfer.
FABPSLVERR	Out	This signal indicates a transfer failure.

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.
From North America, call 800.262.1060
From the rest of the world, call 650.318.4460 Fax, from anywhere in the world, 650.318.8044

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (**www.microsemi.com/soc/support/search/default.aspx**) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.
The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select Yes in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at www.microsemi.com.

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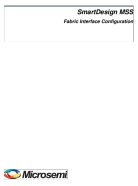
Documents / Resources

	Microsemi SmartDesign MSS Fabric Interface [pdf] Instruction Manual SmartDesign MSS Fabric Interface, MSS Fabric Interface, Fabric Interface, Interface

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- Libero® SoC Design Suite Versions 2023.1 to 12.0 | Microchip Technology
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