

# Microsemi SmartDesign MSS AHB Bus Matrix Configuration User Guide

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SmartDesign MSS  
AHB Bus Matrix Configuration  
Libero® IDE Software

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## Configuration Options

The SmartFusion Microcontroller Subsystem AHB Bus Matrix is highly configurable.

The MSS AHB Bus Matrix configurator enables you to define only a sub-set of the bus matrix configurations. The options defined in the configurator are likely to be static for a given application and – when set in the configurator – will be automatically configured in the SmartFusion device by the Actel System Boot. Other configurable options such as eNVM and eSRAM remapping are more likely to be run-time configurations and are not available in this configurator.

In this document we provide a brief description of these options. For more details please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.

## Configuration Options

### Arbitration

Slave Arbitration Algorithm. Each of the slave interfaces contains an arbiter. The arbiter has two modes of

operation: (pure) round robin and weighted round robin (as shown in Figure 1). The arbitration scheme selected is applied to all slave interfaces. It should be noted that the user can override the arbitration scheme dynamically in their run-time code on the fly.

### Security – Port Access

Each of the non-Cortex-M3 masters connected to the AHB bus matrix can be blocked from accessing any of the slave ports connected to the bus matrix. The Fabric Master, Ethernet MAC and Peripheral DMA ports can be blocked by checking the corresponding check-box in this configurator. **Note** that in the case of the fabric master, access is further qualified by the restricted region options described below.

### Security – Soft Processor Memory Access

#### Restrict Memory Access

- Disabling this option allows any soft processor (or fabric master) to access any location in the Cortex-M3 memory map.
- Enabling this option prevents any soft processor (or fabric master) to access any location in the Cortex-M3 memory map defined by the Restricted Memory Region.

Restricted Memory Region Size – This option defines the size of the restricted memory region to the fabric master.

Restricted Memory Region Address – This option defines the base address of the restricted memoregion. This address should be aligned with the chosen restricted memory region size.

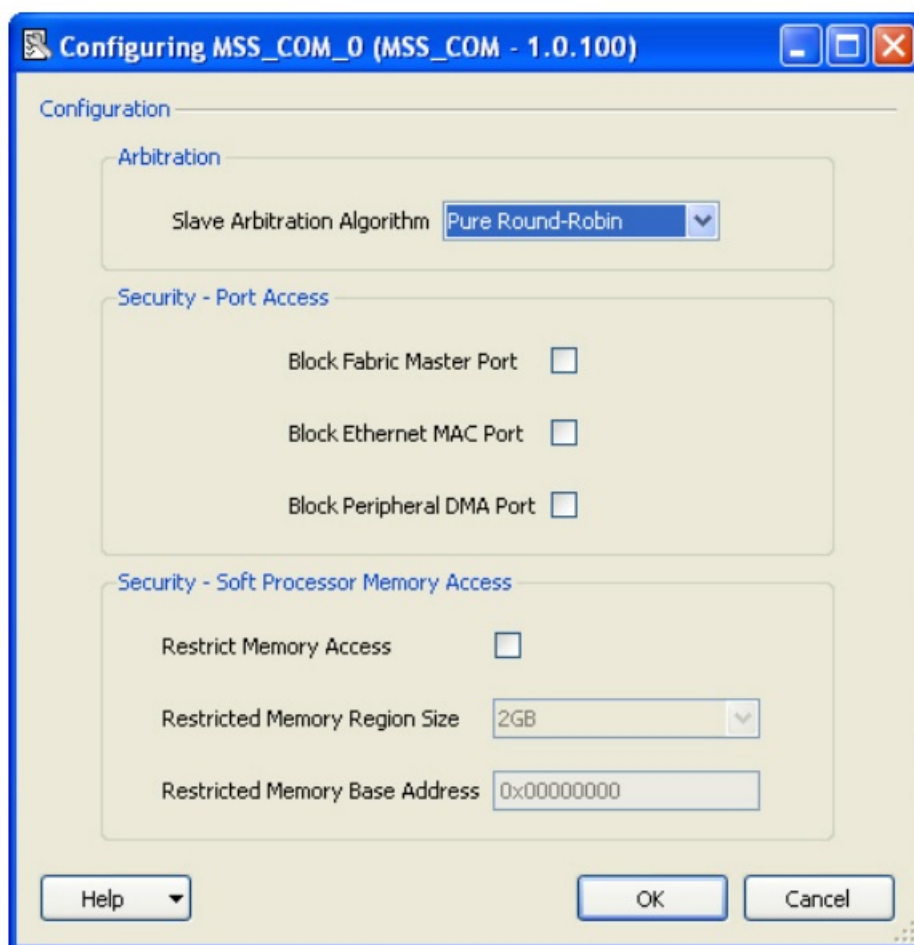


Figure 1 • MSS AHB Bus Matrix Configurator

### Port Description

**Table 1 • Cortex-M3 Port Description**

| Port Name | Direction | PAD? | Description  |
|-----------|-----------|------|--|
| RXEV      | IN        | No   | Causes the Cortex-M3 to wake up from a WFE (wait for event) instruction. The event input, RXEV, is registered even when not waiting for an event, and so affects the next WFE. |
| TXEV      | OUT       | No   | Event transmitted as a result of a Cortex-M3 SEV (send event) instruction. This is a single-cycle pulse equal to 1 FCLK period.  |
| SLEEP     | OUT       | No   | This signal is asserted when the Cortex-M3 is in sleep now or sleep-on-exit mode, and indicates that the clock to the processor can be stopped.                                |
| DEEPSLEEP | OUT       | No   | This signal is asserted when the Cortex-M3 is in sleep now or sleep-on-exit mode when the SLEEPDEEP bit of the System Control Register is set.                                 |

## A – Product Support

The Microsemi SoC Products Group backs its products with various support services including a Customer Technical Support Center and Non-Technical Customer Service. This appendix contains information about contacting the SoC Products Group and using these support services.

### Contacting the Customer Technical Support Center

Microsemi staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

#### Technical Support

Microsemi customers can receive technical support on Microsemi SoC products by calling Technical Support Hotline anytime Monday through Friday. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week. Web: [www.actel.com/mycases](http://www.actel.com/mycases)

Phone (North America): 1.800.262.1060

Phone (International): +1 650.318.4460

Email: [soc\\_tech@microsemi.com](mailto:soc_tech@microsemi.com)

#### ITAR Technical Support

Microsemi customers can receive ITAR technical support on Microsemi SoC products by calling ITAR Technical Support Hotline: Monday through Friday, from 9 AM to 6 PM Pacific Time. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week.

Web: [www.actel.com/mycases](http://www.actel.com/mycases)

Phone (North America): 1.888.988.ITAR

Phone (International): +1 650.318.4900

Email: [soc\\_tech\\_itar@microsemi.com](mailto:soc_tech_itar@microsemi.com)

#### Non-Technical Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

Microsemi's customer service representatives are available Monday through Friday, from 8 AM to 5 PM Pacific Time, to answer non-technical questions.

Phone: +1 650.318.2470





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## Documents / Resources

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| <br><br> | <a href="#">Microsemi SmartDesign MSS AHB Bus Matrix Configuration</a> [pdf] User Guide<br>SmartDesign MSS AHB Bus Matrix Configuration, SmartDesign MSS, AHB Bus Matrix Configuration, Matrix Configuration, Configuration |
|--|---|

## References

-  [FPGAs and PLDs | Microchip Technology](#)
-  [FPGAs and PLDs | Microchip Technology](#)
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-  [Microsemi | Semiconductor & System Solutions | Power Matters](#)