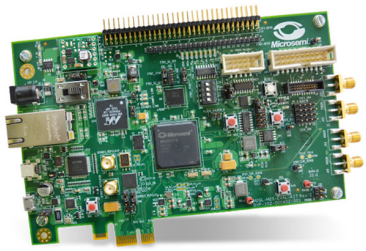

Microsemi IGLOO2 HPMS AHB Bus Matrix Configuration User Guide

IGLOO2 HPMS
AHB Bus Matrix Configuration

Contents

Introduction

The IGLOO2 System Builder automatically configures the memory mapping for you based on your selections of the memory to be used in the design. No user configuration of memory mapping is necessary.
You can use the HPMS AHB Bus Matrix configurator to configure the arbitration schemes. To configure the AHB Bus Matrix access options, use the Security tab in the System Builder (as shown in Figure 1).

***Figure 1* • Security Tab in IGLOO2 System Builder**

The values entered in the configurator will be loaded in the SYSREG block at power up or when the DEVRST_N external pad is asserted/de-asserted.
In this document we provide a brief description of these options. For more details please refer to the **Microsemi IGLOO2 Silicon User's Guides**.

Configuration Options

Arbitration

Each of the slave devices on the AHB bus matrix contains an arbiter. Arbitration is done at two levels. At the first level, the fixed higher priority masters are evaluated for any access request to the slave. At the second level, the remaining busses are evaluated in round robin fashion for any access request to the slave.
Note that you can override the arbitration scheme dynamically in their run-time code on the fly. The following slave arbitration configuration parameters are user programmable registers in the SYSREG block.
You can configure the following parameters from the HPMS AHB Bus Matrix tab of HPMS Options.

- Programmable weight – MASTER_WEIGHT0_CR and MASTER_WEIGHT1_CR are 5-bit programmable registers located in the SYSREG block that define the number of consecutive transfers the weighted master can perform without being interrupted by a fixed priority master, or before moving onto the next master in the WRR cycle. The Round Robin Weight for each of the Masters is user-configurable for values between 1 and 32. The Default is 1 (Figure 1-1).

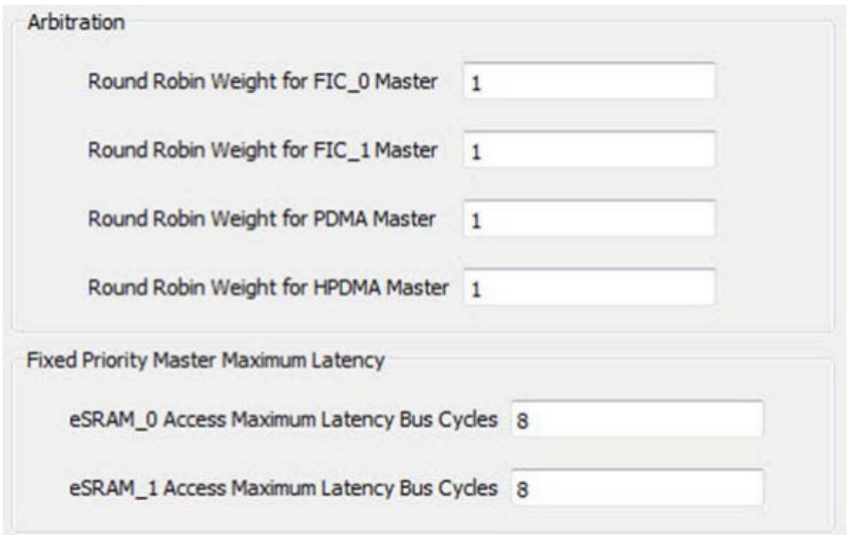

***Figure 1-1* • Programmable Weight Configuration**

- Programmable slave maximum latency – Slave maximum latency, ESRAM_MAX_LAT are 3-bit programmable registers located in the SYSREG block that decides the peak wait time for a fixed priority master arbitrating for eSRAM access while the WRR master is accessing the slave. After the defined latency period, the WRR master must re-arbitrate for slave access. Slave maximum latency can be configurable from 1 to 8 clock cycles (8 by default). ESRAM_MAX_LAT is only supported for fixed priority masters addressing eSRAM slaves; it has no effect on WRR masters. The system designer can use this feature to ensure the processor latency for accesses to eSRAM is limited to a defined number of clock cycles. This is to facilitate limiting the ISR latency for real- time-critical functions (Figure 1-2).

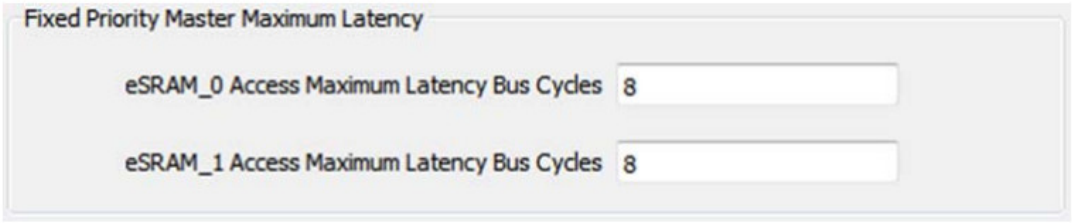

***Figure 1-2* • Programmable Slave Maximum Latency Configuration**

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

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Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

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From the rest of the world, call 650.318.4460

Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (**www.microsemi.com/soc/support/search/default.aspx**) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at **www.microsemi.com/soc**.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

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You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance.

We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

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Documents / Resources

	Microsemi IGLOO2 HPMS AHB Bus Matrix Configuration [pdf] User Guide IGLOO2 HPMS AHB Bus Matrix Configuration, IGLOO2, HPMS AHB Bus Matrix Configuration, Matrix Configuration

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