Microsemi HB0794 CoreReset_PF v2.3 Instructions

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Contents

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 3.0
Added PolarFire® SoC support.

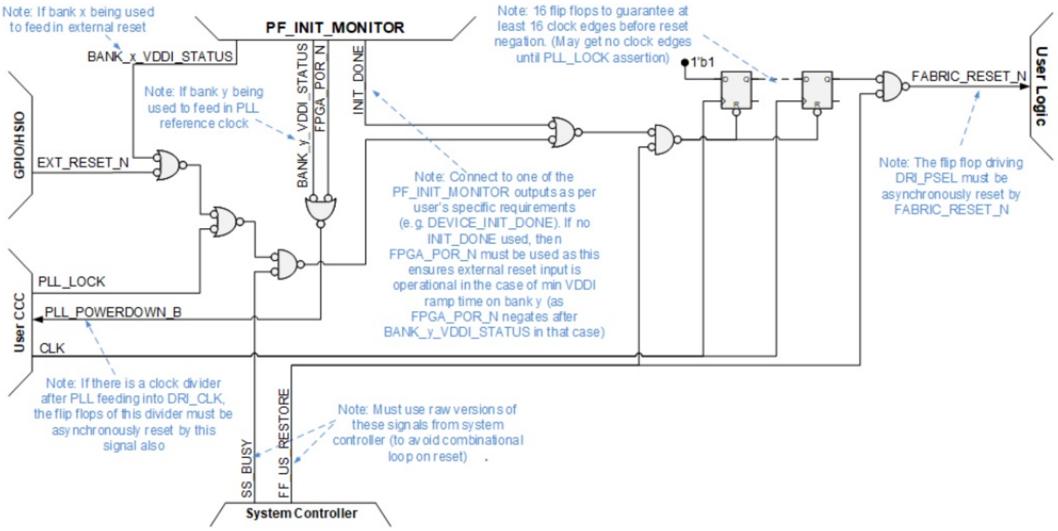
Revision 2.0
Updated for CoreReset_PF v2.2.

Revision 1.0
Revision 1.0 was the first publication of this document. Created for CoreReset_PF v2.1

Introduction

CoreReset_PF allows synchronization of the resets to the user-specified clock domain to which each reset is feeded, so that, when assertion is asynchronous, negation is synchronous to the clock. CoreReset_PF block diagram is as shown in Figure 1, page 2.

Figure 1 • CoreReset_PF Block Diagram



Note: If bank x being used to feed in external reset

Note: If bank y being used to feed in PLL reference clock

Note: 16 flip flops to guarantee at least 16 clock edges before reset negation. (May get no clock edges until PLL_LOCK assertion)

Note: Connect to one of the PF_INIT_MONITOR outputs as per user's specific requirements (e.g. DEVICE_INIT_DONE). If no INIT_DONE used, then FPGA_POR_N must be used as this ensures external reset input is operational in the case of min VDDI ramp time on bank y (as FPGA_POR_N negates after BANK_y_VDDI_STATUS in that case)

Note: The flip flop driving DRI_PSEL must be asynchronously reset by FABRIC_RESET_N

Note: If there is a clock divider after PLL feeding into DRI_CLK, the flip flops of this divider must be asynchronously reset by this signal also

Note: Must use raw versions of these signals from system controller (to avoid combinational loop on reset) .

Key Features

- Generates a reset, which is asserted asynchronously by one of multiple potential sources and which negates synchronously to a specified clock. This ensures that the recovery time of downstream logic is met and that all flip flops come out of reset in the same clock period.
- Multiple reset can be used such as external gpio, phase lock loop lock or init done in conjunction with the master reset from the system controller (through CORESYSSERVICES_PF).

Core Version

This handbook is for CoreReset_PF version 2.3.

Supported Families

- PolarFire® SoC
- PolarFire®

Utilization and Performance

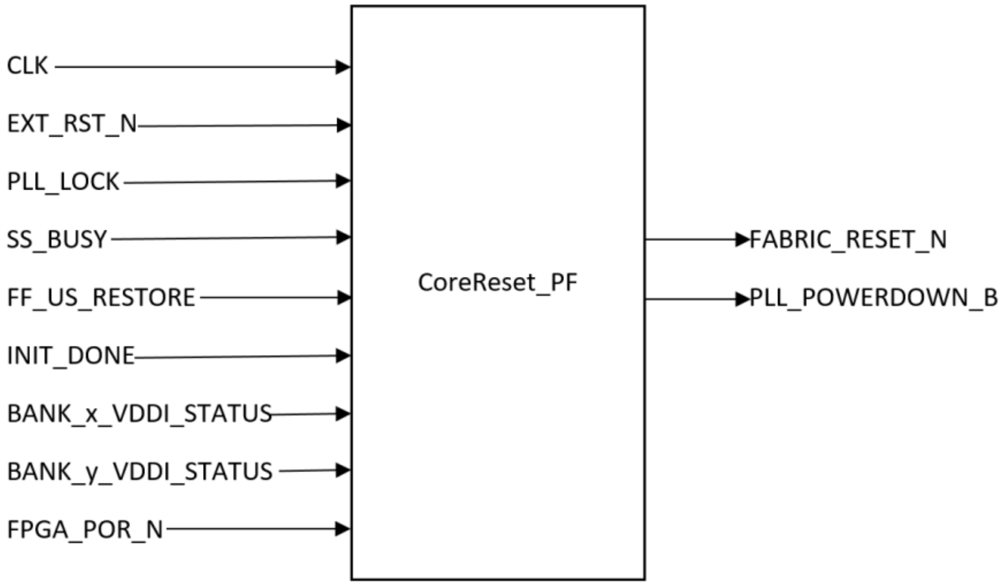
CoreReset_PF has been implemented for the PolarFire and PolarFire SoC device families. A summary of the implementation data for CoreReset_PF is listed in Table 1,

Design Description

I/O Signals

The port signals for the CoreReset_PF macro are as shown in Figure 2, page 4 and defined in Table 2,

Figure 2 • CoreReset_PF I/O Signal Diagram



Tool Flow

Licensing

CoreReset_PF is license free.

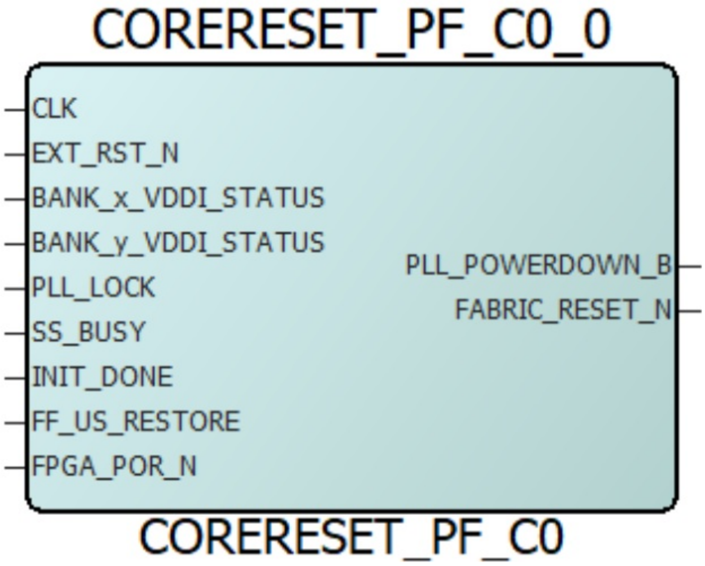
RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreReset_PF is preinstalled in the SmartDesign IP Deployment design environment. The core should be configured using the configuration GUI within SmartDesign, as shown in Figure 3, page 6. To know how to create SmartDesign project using the IP cores, refer to Libero SoC documents page and use the latest SmartDesign user guide.

Figure 3 • CoreReset_PF Full I/O View



Simulation Flows

The user testbench for CoreReset_PF is included in all releases. To run simulations, select the User Testbench flow within the SmartDesign CoreReset_PF configuration GUI, right-click the canvas, and select Generate Design. When SmartDesign generates the design files, it will install the user testbench files. To run the user testbench, Set the design root to the CoreReset_PF instantiation in the LiberoSoC design hierarchy pane and click the Simulation icon in the Libero SoC Design Flow window. This will invoke ModelSim® and automatically run the simulation.

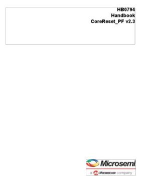
Synthesis in Libero SoC

After setting the design root appropriately for your design, click the Synthesis icon in the Libero SoC. The Synthesis window appears, displaying the Synplicity® project. Set Synplicity to use the Verilog 2001 standard if Verilog is being used. To run Synthesis, click the Run icon.

Place-and-Route in Libero SoC

After setting the design root appropriately for the design, and after running Synthesis, click the Layout icon in the Libero SoC software to invoke Designer. CoreReset_PF requires no special place-and-route settings.

Documents / Resources

 HB0794 Handbook CoreReset_PF v2.3 Microsemi	Microsemi HB0794 CoreReset_PF v2.3 [pdf] Instructions HB0794 CoreReset_PF v2.3, HB0794, CoreReset_PF v2.3, v2.3

References

- Microsemi | Semiconductor & System Solutions | Power Matters